

10 bit ADC with Serial Control

PRODUCT DESCRIPTION

The MS1549/MS1549I is a 10bit, switched-capacitor and SAR analog-to-digital converter. It has two digital input terminals and one tri-state output terminal (\overline{CS} , I/O CLOCK and DATA OUT) which can complete the data communication from three-wire interface to controller.

The MS1549/MS1549I has automatic sample-and-hold, proportional scale calibrating conversion range, anti-noise-interference functions. Therefore, the MS1549/MS1549I can be widely used in the analog-to-digital conversion.



SOP8

FEATURES

- 10bit ADC
- Internal Sample-and-Hold Function
- INL: 1LSB
- On-chip System Clock
- Pin Compatible with TLC1549 and TLV1549

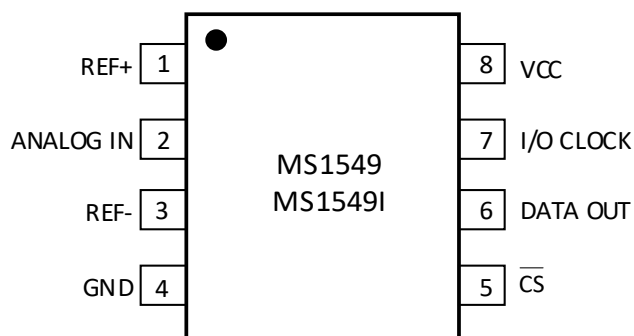
APPLICATIONS

- Analog-to-Digital Conversion like Sensor

PRODUCT SPECIFICATION

Part Number	Operating Temperature	Package	Marking
MS1549	0°C ~ 70°C	SOP8	MS1549
MS1549I	-30°C ~ 85°C	SOP8	MS1549

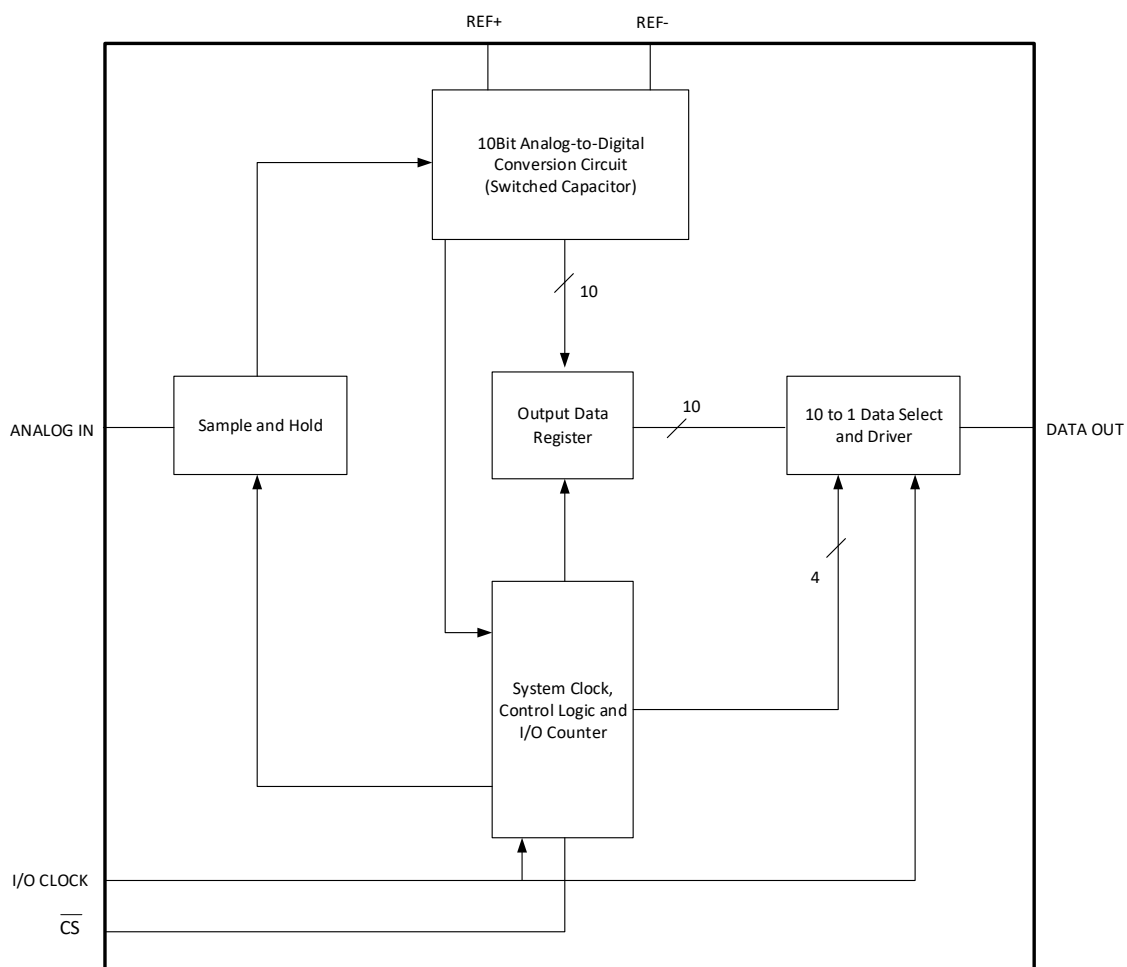
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Typ	Description
1	REF+	I	Positive Reference Voltage. The input voltage range is the differential value of REF+ and REF- voltage.
2	ANALOG IN	I	Analog Signal Input. Power impedance should be less than 1kΩ.
3	REF-	I	Negative Reference Voltage
4	GND	-	Ground
5	\overline{CS}	I	Chip Select
6	DATA OUT	O	When \overline{CS} is high, AD conversion result is high-impedance. When \overline{CS} is low, AD conversion result is valid.
7	I/O CLOCK	IO	Input/Output Clock
8	VCC	-	Positive Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Range	Unit
Power Supply	-0.5 ~ 6.5	V
Input Range	-0.3 ~ $V_{CC}+0.3$	V
Output Range	-0.3 ~ $V_{CC}+0.3$	V
Positive Reference Voltage	$V_{CC}+0.1$	V
Negative Reference Voltage	-0.1	V
Input Peak Current	± 20	mA
Total Peak Current	± 30	mA
Storage Temperature	-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	2.7	5	5.5	V
Positive Reference Voltage	V_{REF+}		V_{CC}		V
Negative Reference Voltage	V_{REF-}		0		V
Differential Reference Voltage	$V_{REF+} - V_{REF-}$	2.5	V_{CC}	$V_{CC}+0.2$	V
Analog Input Voltage		0		V_{CC}	V
Digital High-level Input Voltage ($V_{CC}=2.7V$ to $5.5V$)		$0.8 \times V_{CC}$			V
Digital Low-level Input Voltage ($V_{CC}=2.7V$ to $5.5V$)				$0.2 \times V_{CC}$	V
I/O CLOCK Frequency		0		2.1	MHz
Setup Time, \overline{CS} Falling Edge to I/O CLOCK Rising Edge	$t_{SU(CS)}$	1.425			μs
Hold Time, \overline{CS} Rising Edge to I/O CLOCK Falling Edge	$t_{H(CS)}$	0			ns
I/O CLOCK High-level Time	$t_{WH(I/O)}$	190			ns
I/O CLOCK Low-level Time	$t_{WL(I/O)}$	190			ns
I/O CLOCK Level Transition Time	$t_{t(I/O)}$			1	μs
\overline{CS} Transition Time	$t_{t(CS)}$			10	μs

ELECTRICAL CHARACTERISTICS

$V_{CC}=5V$, $V_{REF}=2.5V$, I/O CLOCK frequency 2MHz.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Output Voltage	V_{OH}	$V_{CC}=2.7V$, $I_{OH}=-1.6mA$	2.4			V
		$V_{CC}=2.7V\sim 5.5V$, $I_{OH}=-20\mu A$	$V_{CC}-0.1$			
Low-level Output Voltage	V_{OL}	$V_{CC}=2.7V$, $I_{OL}=-1.6mA$			0.4	V
		$V_{CC}=2.7V\sim 5.5V$, $I_{OH}=20\mu A$			0.1	
High-impedance Output Current	I_{OZ}	$V_O=V_{CC}$, \overline{CS} at VCC			10	μA
		$V_O=0$, \overline{CS} at VCC			-10	
High-level Input Current	I_{IH}	$V_I=V_{CC}$		0.05	2.5	μA
Low-level Input Current	I_{IL}	$V_I=0$		-0.05	-2.5	μA
Operating Current	I_{CC}	$\overline{CS}=0$		0.35	0.7	mA
Analog Input Leakage Current		$V_I=0\sim V_{CC}$		± 1		μA
REF+ Input Current		$V_{REF+}=V_{CC}$, $V_{REF-}=0$			10	μA
Input Capacitance	C_i	In sample period		30		pF
INL ²					± 1	LSB
EZS Zero-scale Error ³		See Note 1			± 1	LSB
EFS Full-scale Error ³		See Note 1			± 1	LSB
Total Unadjusted Error ⁴					± 1	LSB

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Conversion Time	t_{CONV}				21	μs
Conversion Time (Sample, Hold and Convert)	t_c				21+10 I/O CLOCK Period ⁵	μs
DATA OUT Valid Time after the I/O CLOCK Falling Edge	t_v	See Figure 3	10			ns
Delay Time, I/O CLOCK Falling Edge to DATA OUT Valid	$t_{D(I/O-DATA)}$	See Figure 3			240	ns
Enable Time, \overline{CS} Falling Edge to DATA OUT	t_{PZH}, t_{PZL}	See Figure 1			1.3	μs
Disable Time, \overline{CS} Rising Edge to DATA OUT	t_{PHZ}, t_{PLZ}	See Figure 1			180	ns
Rise Time for Data Bus	$t_{R(BUS)}$	See Figure 3			300	ns
Fall Time for Data Bus	$t_{F(BUS)}$	See Figure 3			300	ns
Delay Time, Tenth I/O CLOCK Falling Edge to \overline{CS} Falling Edge ⁶	$t_{D(I/O-\overline{CS})}$				9	μs

Note:

1. When analog input voltage is higher than REF+, conversion output is all 1. When analog input voltage is lower than REF-, conversion output is all 0. The input voltage range of the MS1549/MS1549I can be low to 1V ($V_{REF+} - V_{REF-}$). At this time, recommended electrical parameters are not applicable.
2. INL is that the actual conversion output deviating from the best input/output characteristic straight line.
3. Zero-scale error is the difference between all 0 and the output for zero input voltage. Full-scale error is the difference between all 1 and the output for full-scale input voltage.
4. Total unadjusted error consists of linearity error, zero-scale error and full-scale error.
5. I/O CLOCK Period=1/(I/O CLOCK Frequency). Sample starts from the third I/O CLOCK falling edge and lasts seven I/O CLOCK periods and finishes on the tenth I/O CLOCK falling edge.
6. \overline{CS} transition is only valid only when the level maintains for a minimum setup time plus two fall time of internal clock after the tenth I/O CLOCK.

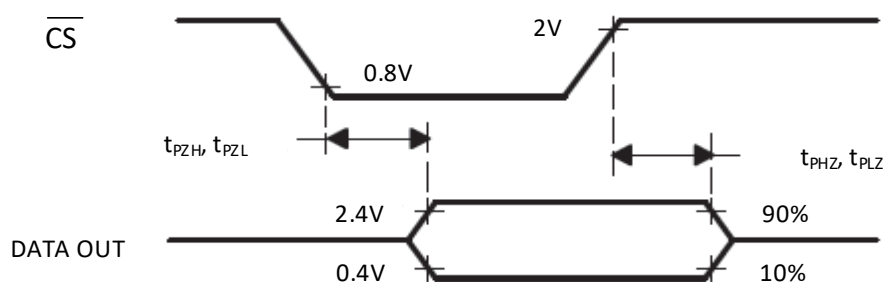


Figure 1. DATA OUT to Hi-Z Waveform

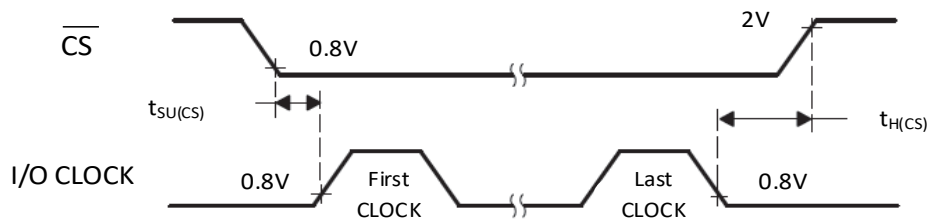


Figure 2. $\overline{\text{CS}}$ to I/O CLOCK Waveform

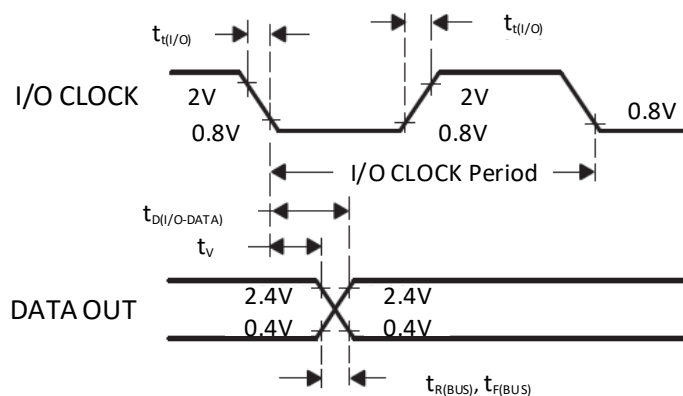


Figure 3. I/O CLOCK and DATA OUT Waveform

FUNCTION DESCRIPTION

When \overline{CS} is high-level, I/O CLOCK is disabled and DATA OUT is high-impedance state. When \overline{CS} is pulled low, the data conversion begins with CLOCK. After conversion finishes, output result on DATA OUT. Set 10 and 16 clocks periods for CLOCK by serial interface. Sampling the analog signal is completed within the first ten clocks periods.

The MS1549/MS1549I has six basic serial interface time modes that depend on clock speed and \overline{CS} operation. These modes include:

Mode 1: (Fast Mode) 10 clock periods for conversion time and \overline{CS} high.

Mode 2: (Fast Mode) 10 clock periods for conversion time and \overline{CS} low.

Mode 3: (Fast Mode) 11~16 clock periods for conversion time and \overline{CS} high.

Mode 4: (Fast Mode) 16 clock periods for conversion time and \overline{CS} low.

Mode 5: (Slow Mode) 11~16 clock periods for conversion time and \overline{CS} high.

Mode 6: (Slow Mode) 16 clock periods for conversion time and \overline{CS} low.

In the mode 1, 3, 5, after \overline{CS} falling edge, DATA OUT pin starts to output the MSB of conversion.

In the mode 2 and 4, within 21 μ s after the tenth clock falling edge, DATA OUT starts to output the MSB of conversion.

In the mode 6, after the sixteenth clock falling edge, DATA OUT starts to output the MSB of conversion. In following nine clock falling edges, remaining 9bits are bit-by-bit output. The number of clock pulse is decided by selected operation mode. But for conversion startup, the minimum 10 clock pulses are needed. If more than 10 clock pulses, internal logic would pull DATA OUT low to ensure the remaining bits are cleared on the tenth clock falling edge.

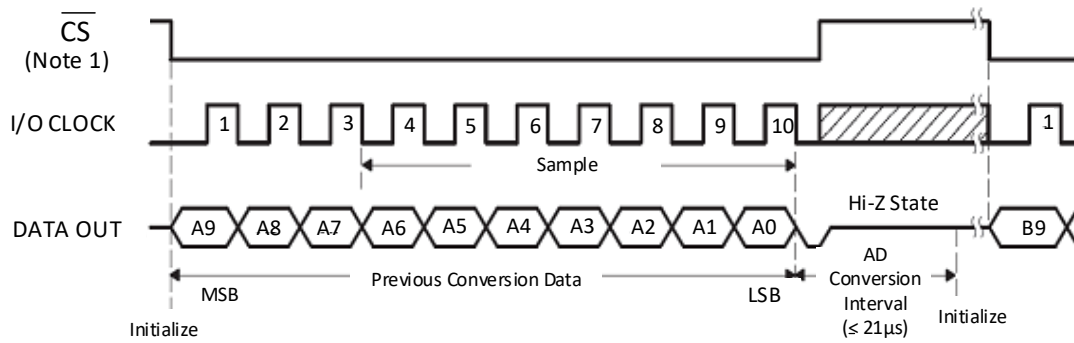
All modes need a minimum 21 μ s delay time after the tenth clock falling edge before next conversion begins. During serial data transmission, \overline{CS} must be low to ensure enabling I/O CLOCK. \overline{CS} state is latched when data transmission in the modes 1, 3, and 5. \overline{CS} transition is thank as valid only when the level maintains for at least 1.425 μ s after the transition. In the modes 3, 4, 5, and 6, If the transmission time is more than ten clock period, the eleventh clock rising edge must occur within 9.5 μ s after the tenth falling edge. Otherwise host serial interface may not synchronize. \overline{CS} would toggle to recovery correct operation mode.

Fast Mode

In fast mode, serial clock transmission would be completed within 21 μ s after the tenth clock falling edge. In a 10-clock-period serial transmission, can only operate fast mode.

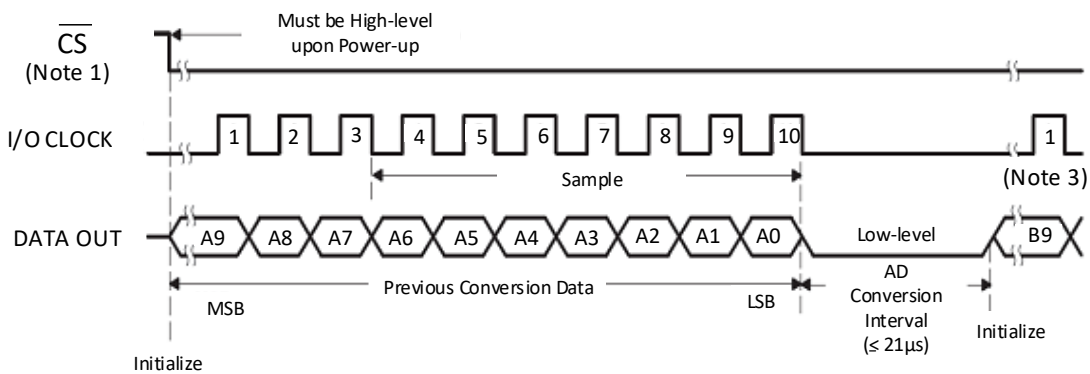
Mode 1: Fast mode, \overline{CS} high between data transmission, 10-clock period.

In this mode, each data transmission is ten-clock period and \overline{CS} becomes high during this time. When the falling edge of \overline{CS} starts, DATA OUT removes high-impedance state. When the rising edge of \overline{CS} ends, DATA OUT returns to high-impedance state within the specified time. In addition, the rising edge of \overline{CS} disables I/O CLOCK within a startup time plus two falling edges of the internal system clock. The timing is as follows:


Mode 1 : 10-Clock Transmission Period with \overline{CS} High

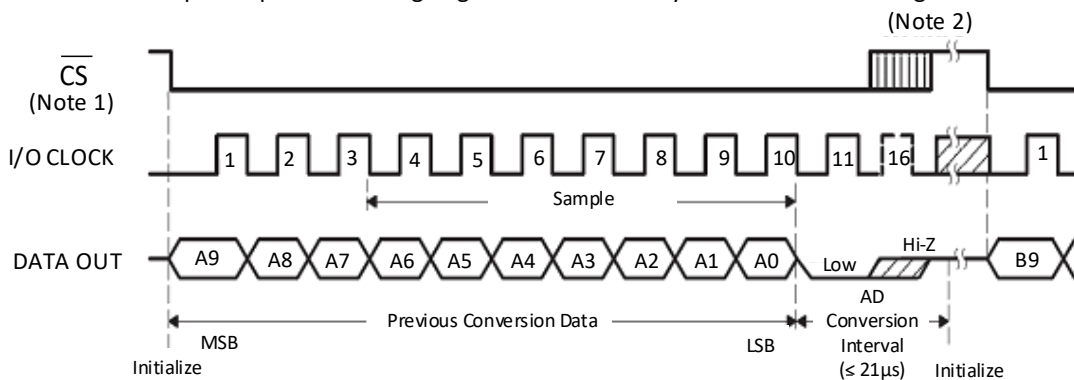
Mode 2: Fast mode, \overline{CS} low between data transmission, 10-clock period.

In this mode, each data transmission is ten-clock period and \overline{CS} becomes low during this time. After initializing the conversion period, \overline{CS} remains low-level for subsequent conversions. Within 21μs after the tenth falling edge, DATA OUT outputs the MSB of the previous conversion. The timing is as follows:


Mode 2 : 10-Clock Transmission Period with \overline{CS} Low

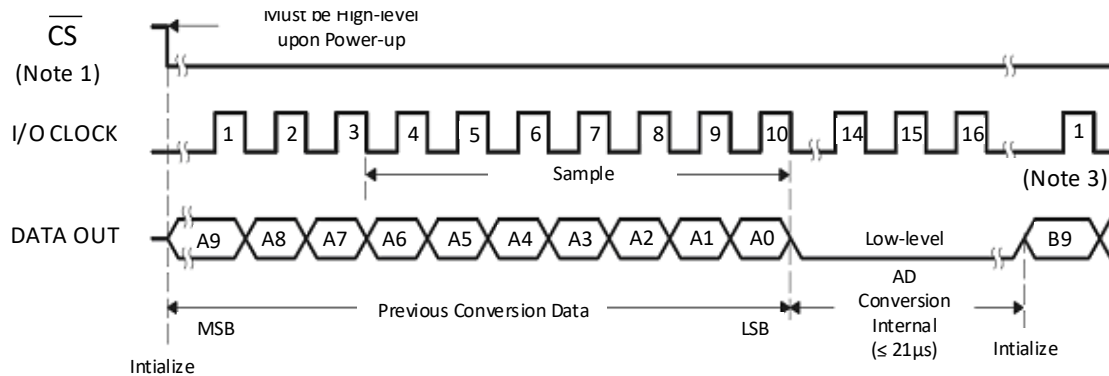
Mode 3: Fast mode, \overline{CS} high between data transmission, 11~16 clock period.

In this mode, each data transmission is 11 to 16 period and \overline{CS} becomes high during this time. When the falling edge of \overline{CS} starts, DATA OUT removes high-impedance state. When the rising edge of \overline{CS} ends, DATA OUT returns to high-impedance state within the specified time. In addition, the rising edge of \overline{CS} disables I/O CLOCK within a startup time plus two falling edges of the internal system clock. The timing is as follows:


Mode 3 : 11 to 16 Clock Transmission Period with \overline{CS} High (Completed within 21μs)

Mode 4: Fast mode, \overline{CS} low between data transmission, 16-clock period.

In this mode, each data transmission is sixteen-clock period and \overline{CS} becomes low during this time. After initializing the conversion period, \overline{CS} remains low-level for subsequent conversions. Within 21 μ s after the tenth falling edge, DATA OUT outputs the MSB of the previous conversion. The timing is as follows:



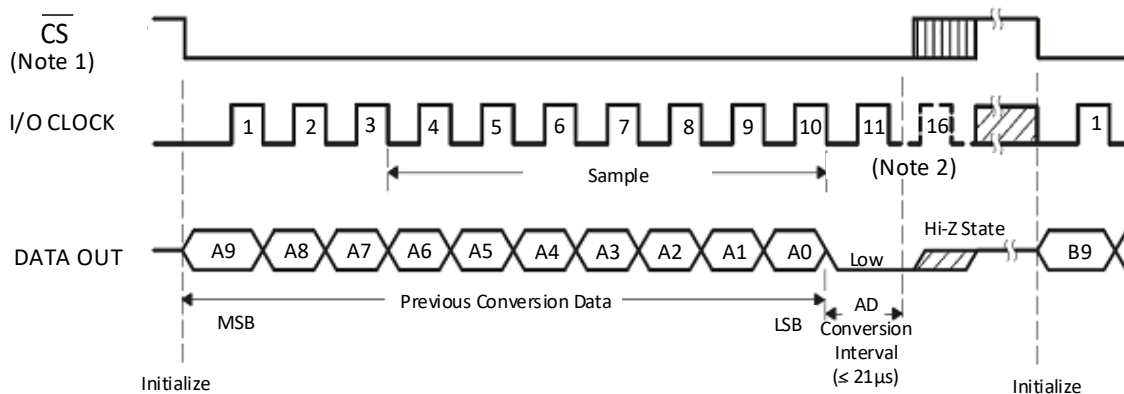
Mode 4 : 16-Clock Transmission Period with \overline{CS} Low (Completed within 21 μ s)

Slow Mode

In slow mode, the serial clock data transmission is completed within 21 μ s after the tenth clock falling edge.

Mode 5: Slow mode, \overline{CS} high between data transmission, 11~16 clock period.

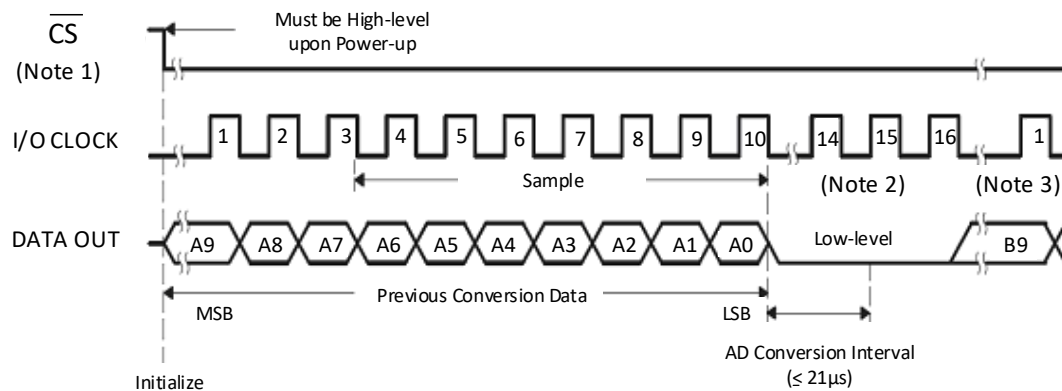
In this mode, each data transmission is 11 to 16 period and \overline{CS} becomes high during this time. When the falling edge of \overline{CS} starts, DATA OUT removes high-impedance state. When the rising edge of \overline{CS} ends, DATA OUT returns to high-impedance state within the specified time. In addition, the rising edge of \overline{CS} disables I/O CLOCK within a startup time plus two falling edges of the internal system clock. The timing is as follows:



Mode 5 : 11 to 16 Clock Transmission Period with \overline{CS} High (Completed after 21 μ s)

Mode 6: Slow mode, \overline{CS} low between data transmission, 16-clock period.

In this mode, each data transmission is sixteen-clock period and \overline{CS} becomes low during this time. After initializing the conversion period, \overline{CS} remains low-level for subsequent conversions. After the sixteen clock falling edges, DATA OUT removes low-level state and starts new conversion period, allowing DATA OUT pin to output the MSB of the previous conversion. Then the device is ready for the next 16-clock conversion initiated by the serial interface. The timing is as follows:



Mode 6 : 16-Clock Transmission Period with \overline{CS} Low (Completed after $21\mu s$)

Note:

1. To reduce errors caused by \overline{CS} noise, the internal circuit needs the wait time for a startup time plus two falling edges of the internal system clock after the falling edge of \overline{CS} . Then respond to I/O CLOCK. The data is output until the minimum \overline{CS} setup time has elapsed.
2. The rising edge of \overline{CS} disables I/O CLOCK within a startup time plus two falling edges of the internal system clock.
3. The first I/O CLOCK must occur at the end of the previous conversion.

Analog Input Sample

Analog input sample starts after the third clock falling edge, and lasts for seven clock periods. The sample value is held on the tenth falling edge.

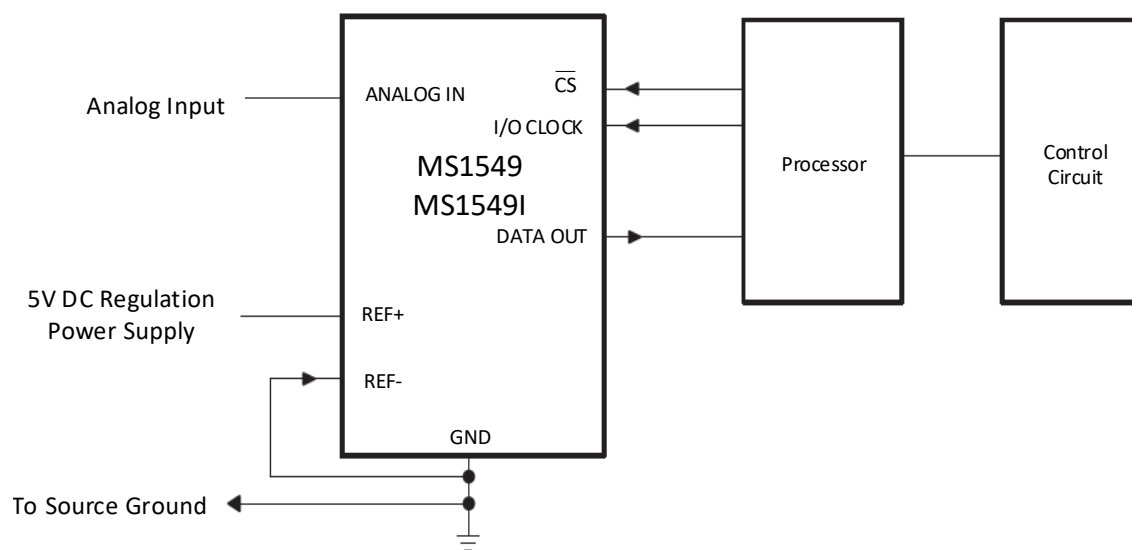
Chip Select

\overline{CS} transition can start all modes and stops any mode conversion. In specified time, when \overline{CS} goes from high to level, the device would return to initial state (output register still remains the previous conversion result). It is noted that if \overline{CS} is pulled at the end of conversion, data may be lost.

Reference Input

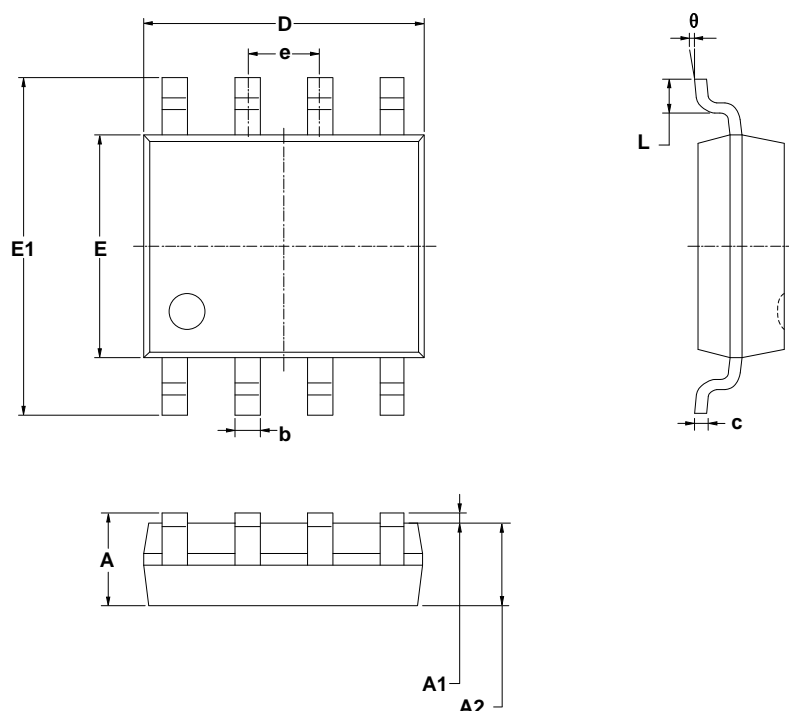
The MS1549/MS1549I has two reference voltages, REF+ and REF-. These two voltage values set the upper and lower limit of analog input voltage respectively. Analog input voltage cannot exceed power supply and cannot be less than GND. When input signal is more than or equal to REF+, digital output is full-scale. When input signal is less than or equal to REF-, digital output is 0.

TYPICAL APPLICATION DIAGRAM



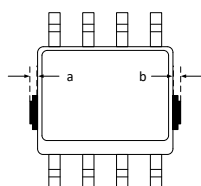
PACKAGE OUTLINE DIMENSIONS

SOP8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Note: In addition to the package size, a and b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.



MARKING and PACKAGE SPECIFICATION**1. Marking Drawing Description**

Product Name: MS1549, MS1549I

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS1549	SOP8	2500	1	2500	8	20000
MS1549I	SOP8	2500	1	2500	8	20000

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**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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