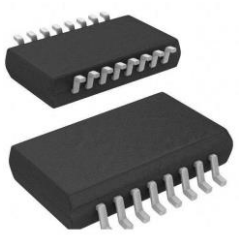
LVDS Quad Bus Driver

PRODUCT DESCRIPTION

The MS90C031 is low power dissipation, high data rate, four-channel, CMOS, differential LVDS signal bus driver.

The supported data receiving rate exceeds 155.5Mbps (77.7MHz). The MS90C031 converts TTL/CMOS input signal to low-voltage (350mV), differential output signal. The driver also supports tri-state output function and can be used to shut down output driving stage. According to the shutdown of output current, 11mW static power dissipation could be get. In addition, the MS90C031 has power-down shutdown function. When VCC is open-circuit, LVDS output is in high-impedance state. The function can maintain the minimum load on LVDS bus at power down.

The MS90C031 bus driver and bus receiver (MS90C032) provide a new method for high point-to-point interface application.



SOP16

FEATURES

- More than 155.5Mbps (77.7MHz) Switch Frequency
- LVDS Output Hi-Z at Power-down
- ±350mV Differential Output Signal
- Low Power Dissipation
- the Maximum 400ps Channel Propagation Delay Difference (5V,25°C)
- the Maximum 3.5ns Propagation Delay
- Industrial-grade Temperature Application Range
- Compatible with DS26C31, MB571(PECL) and 41LG(PECL)
- Compatible with ANSI/TIA/EIA-644 LVDS Standard
- SOP16 Package

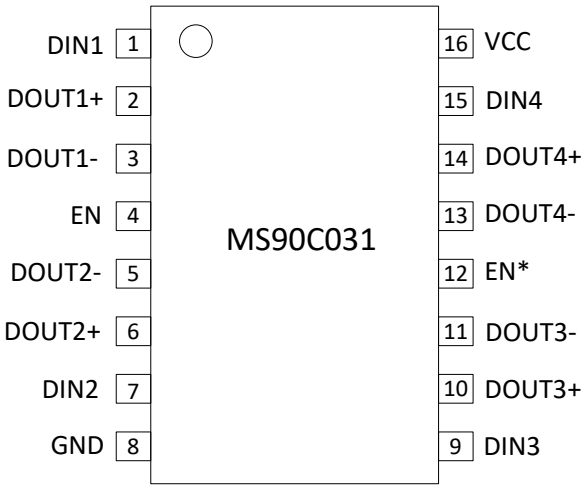
APPLICATIONS

- Flat Panel Display Interface
- High-speed Data Communication
- Monitor Camera

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS90C031	SOP16	MS90C031

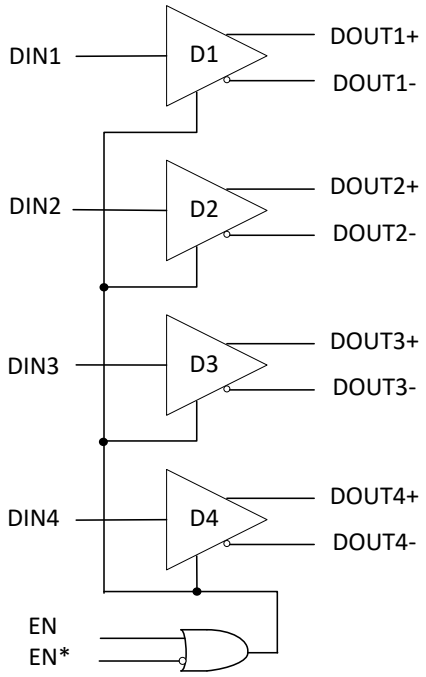
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1, 7, 9, 15	DIN	I	CMOS/TTL Input Signal
2, 6, 10, 14	DOUT+	O	LVDS No-inverting Output
3, 5, 11, 13	DOUT-	O	LVDS Inverting Output
4	EN	I	Active High, OR with EN*
12	EN*	I	Active Low, OR with EN
16	VCC	-	Power Supply, +5V ± 10%
8	GND	-	Ground

BLOCK DIAGRAM



Function Table

Enable		Input	Output	
EN	EN*	Din	Dout+	Dout-
L	H	X	Z	Z
Other Condition		L	L	H
		H	H	L

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VCC	-0.3 ~ 6	V
Input Voltage	Din	-0.3 ~ VCC+0.3	V
Input Voltage for Enables	EN, EN*	-0.3 ~ VCC+0.3	V
Output Voltage	Dout+, Dout-	-0.3 ~ VCC+0.3	V
Maximum Junction Temperature	Tj	+150	°C
Storage Temperature	Tstg	-60 ~ 150	°C
ESD (HBM)	1.5kΩ, 100pF	≥ 3500	V
ESD (EIAJ)	0 Ω, 200pF	≥ 250	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	VCC	2.5	5	5.5	V
Operating Temperature		-40	25	125	°C

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Pin	Condition	Min	Typ	Max	Unit
Differential Output Voltage	Vod1	Dout- Dout+	RL=100Ω (Figure 1),VCC=5.0V	320	398	450	mV
			RL=100Ω (Figure 1),VCC=3.3V	300	380	420	mV
Differential Output Voltage Difference (Complementary Output)	ΔVod1		RL=100Ω (Figure 1),VCC=5.0V		4	35	mV
			RL=100Ω (Figure 1),VCC=3.3V		4	35	mV
Common-mode Output Voltage	Vos		RL=100Ω (Figure 1),VCC=5.0V	1.16	1.43	1.53	V
			RL=100Ω (Figure 1),VCC=3.3V	1.13	1.39	1.40	V
Common-mode Output Voltage Difference (Complementary Output)	ΔVos		RL=100Ω (Figure 1),VCC=5.0V		5	25	mV
			RL=100Ω (Figure 1),VCC=3.3V		5	25	mV
Output High Level	V_{OH}		RL=100Ω,VCC=5.0V		1.58	1.75	V
			RL=100Ω,VCC=3.3V		1.55	1.62	V
Output Low Level	V_{OL}		RL=100Ω,VCC=5.0V	0.98	1.20		V
			RL=100Ω,VCC=3.3V	0.95	1.18		V
Input High Level	V_{IH}	Din, EN, EN*	VCC=5.0V	2.0		VCC	V
			VCC=3.3V	1.5		VCC	V
Input Low Level	V_{IL}		VCC=5.0V	GND		0.8	V
			VCC=3.3V	GND		0.7	V
Input Current	I_I		VCC=5.0V,Vin=VCC, GND, 2.5V or 0.4V	-10	±1	+10	μA
			VCC=3.3V,Vin=VCC, GND, 2.5V or 0.4V	-10	±1	+10	μA
Input Clamp Voltage	V_{CL}		I_{CL}=-18mA,VCC=5.0V	-1.5	-0.8		V
			I_{CL}=-18mA,VCC=3.3V	-1.5	-0.8		V
Output Short-circuit Current	I_{OS}	Dout- Dout+	Vout=0V (Note 4),VCC=5.0V		-4.5	-6.0	mA
			Vout=0V (Note 4),VCC=3.3V		-4.0	-5.0	mA
Output Tri-state Current	I_{OZ}		VCC=5.0V,EN=0.8V, EN*=2.0V,Vout=0 or VCC	-10	±1	+10	μA
			VCC=3.3V,EN=0.8V, EN*=2.0V,Vout=0 or VCC	-10	±1	+10	μA
Off Current	I_{OFF}	VCC	Vo=0V,VCC=0V or Open-circuit	-10	±1	+10	μA
			Vo=2.4V,VCC=0V or Open-circuit	-10	±1	+10	μA

No Load Power Supply Current at Driver Enabled	I_{CC}	VCC	VCC=5.0V, Din=VCC or GND		1.9	4.0	mA
			VCC=3.3V, Din=VCC or GND		1.7	3.0	
			VCC=5.0V, Din=2.5V or 0.4V		4.0	6.5	
			VCC=3.3V, Din=2.5V or 0.4V		3.3	6	
Load Power Supply Current at Driver Enabled	I_{CCL}		VCC=5.0V, RL=100Ω, Vin=VCC or GND		16.8	21.0	mA
			VCC=3.3V, RL=100Ω, Vin=VCC or GND		18	22.0	mA
No Load Power Supply Current at Driver Disabled	I_{CCZ}		VCC=5.0V, Din=VCC or GND, EN=GND, EN*=VCC		1.7	4.0	mA
			VCC=3.3V, Din=VCC or GND, EN=GND, EN*=VCC		2.0	4.2	mA

Switch Characteristic 1

VCC=+5.0V, TA=+25°C (Note 1, 3, 5)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Differential Propagation Delay (High to Low)	tPHLD	RL=100Ω, CL=5PF Figure 2 and Figure 3	1.0	2.0	3.0	ns
Differential Propagation Delay (Low to High)	tPLHD		1.0	2.0	3.0	ns
Differential Propagation Delay Difference |tPHLD- tPLHD|	tSDK		0	80	400	ps
Channel Propagation Delay Difference (Note 2)	tSK1		0	300	600	ps
Rise Time	tTLH			0.35	1.5	ns
Fall Time	tRHLD			0.35	1.5	ns
Delay, Output High to Hi-Z	tPHZ	RL=100Ω, CL=5PF Figure 4 and Figure 5		2.5	10	ns
Delay, Output Low to Hi-Z	tPLZ			2.5	10	ns
Delay, Output Hi-Z to High	tPZH			2.5	10	ns
Delay, Output Hi-Z to Low	tPZL			2.5	10	ns

Switch Characteristic 2

VCC=+5.0V±10%, TA=-40 to +85°C, (Note 1, 3, 5)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Differential Propagation Delay (High to Low)	tPHLD	RL=100Ω, CL=5PF Figure 2 and Figure 3	1.0	2.0	3.5	ns
Differential Propagation Delay (Low to High)	tPLHD		1.0	2.0	3.5	ns
Differential Propagation Delay Difference |tPHLD- tPLHD|	tSDK		0	80	900	ps
Channel Propagation Delay Difference (Note 2)	tSK1		0	300	1000	ps
Rise Time	tTLH			0.35	2	ns
Fall Time	tRHLD			0.35	2	ns
Delay, Output High to Hi-Z	tPHZ	RL=100Ω, CL=5PF Figure 4 and Figure 5		2.5	15	ns
Delay, Output Low to Hi-Z	tPLZ			2.5	15	ns
Delay, Output Hi-Z to High	tPZH			2.5	15	ns
Delay, Output Hi-Z to Low	tPZL			2.5	15	ns

Note:

1. All typical values are measured at VCC =+5.0V, TA=+25°C.

2. Channel propagation delay difference is that the maximum propagation delay difference between the four channels.

3. In general test, input signal: f=1MHz, Zo=50Ω, tr, tf ≤6ns.

4. Output short-circuit current (I_{OS}), the value is magnitude and minus is current direction.

5. Load capacitance includes probe and soldering capacitance.

Test Circuit

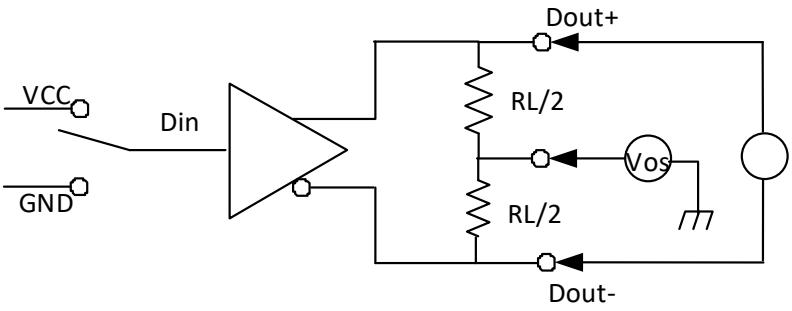


Figure 1. Vod and Vos Test Circuit

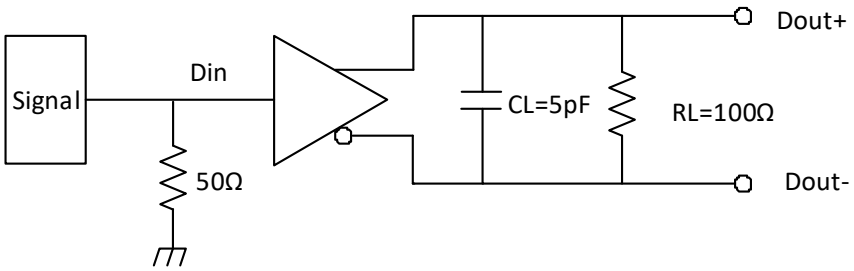


Figure 2. Propagation Delay and Edge Transition Time Test Circuit

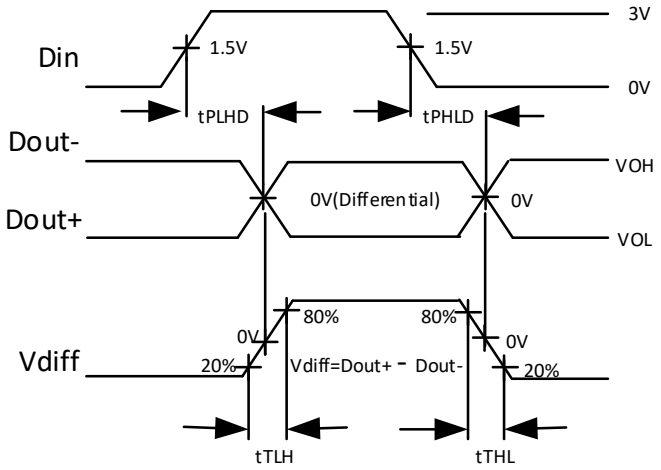


Figure 3. Propagation Delay and Edge Transition Time Waveforms

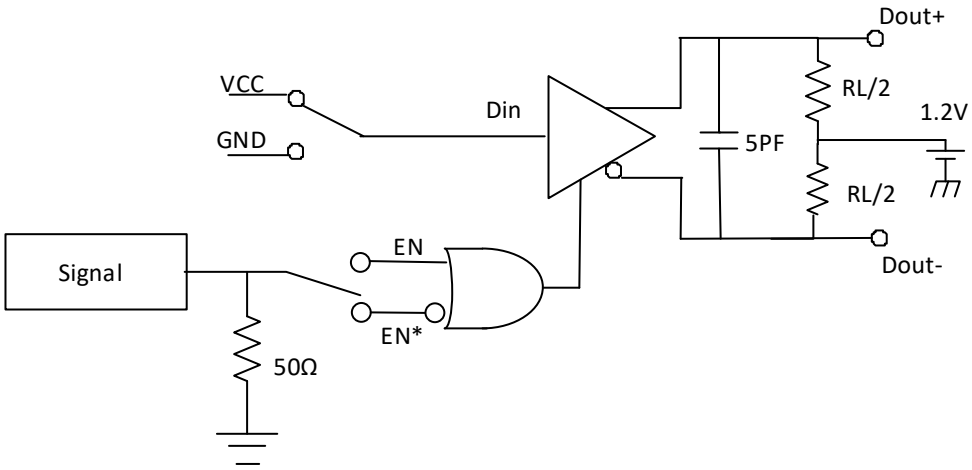
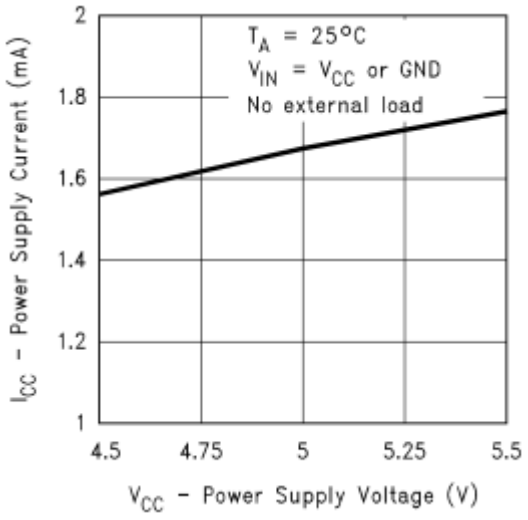
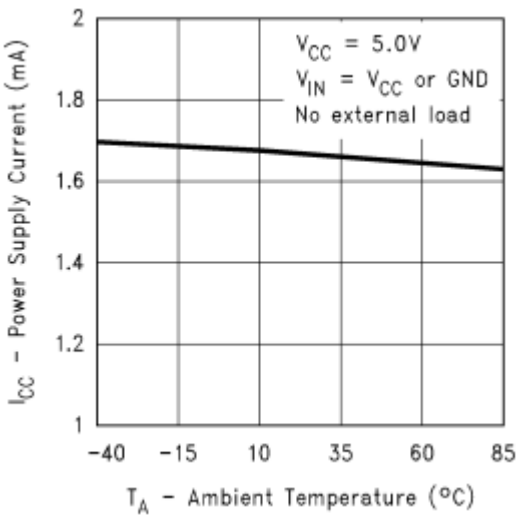


Figure 4. Tri-state Delay Test Circuit

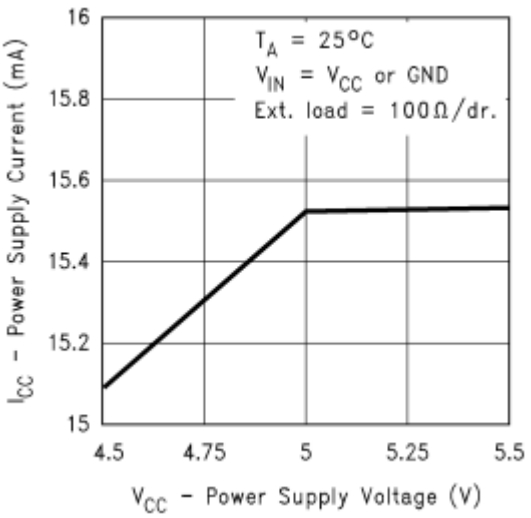
TYPICAL CHARACTERISTICS CURVES



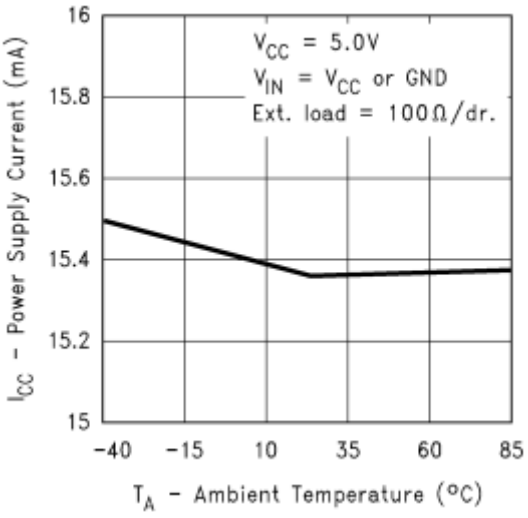
Power Supply Current VS. Power Supply (No load)



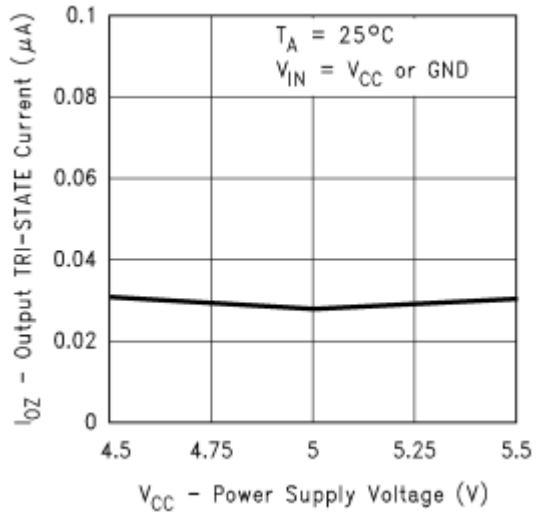
Power Supply Current VS. Temperature (No load)



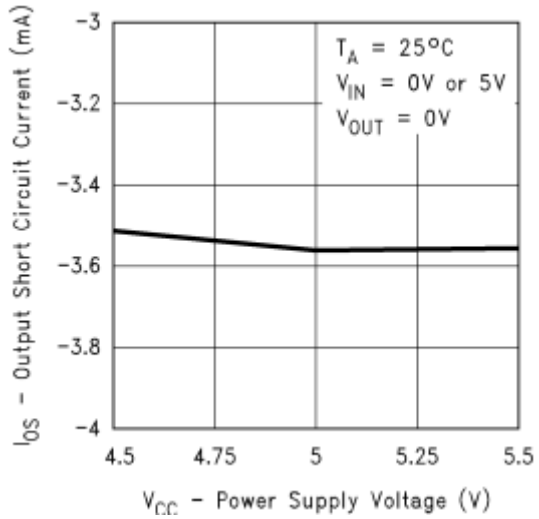
Power Supply Current VS. Power Supply (100Ω Load)



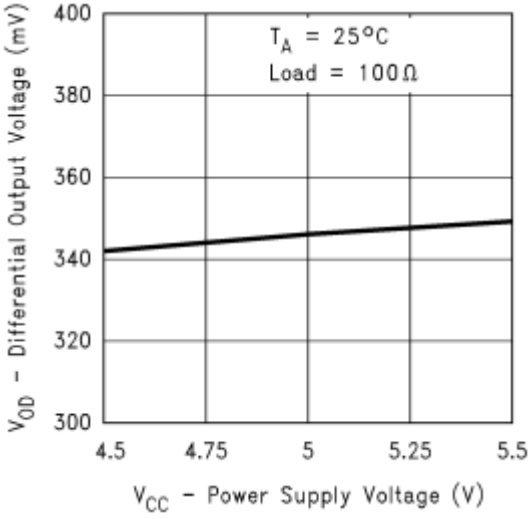
Power Supply Current VS. Temperature (100Ω Load)



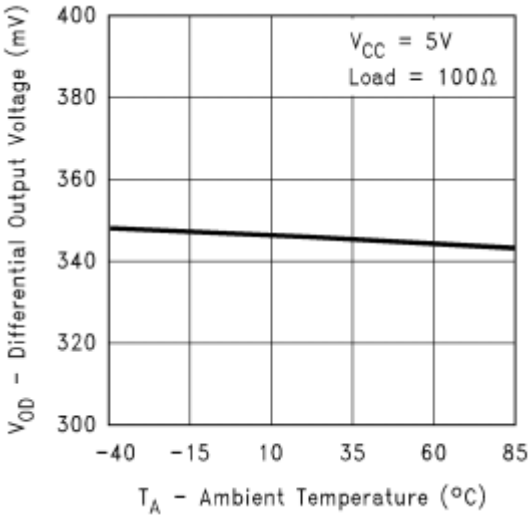
Output Tri-state Current VS. Power Supply



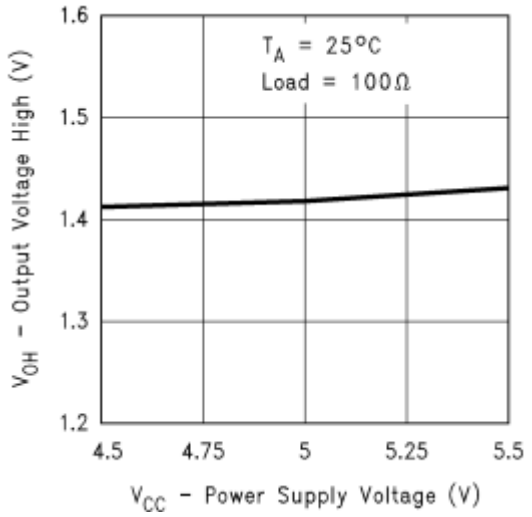
Output Short-circuit Current VS. Power Supply



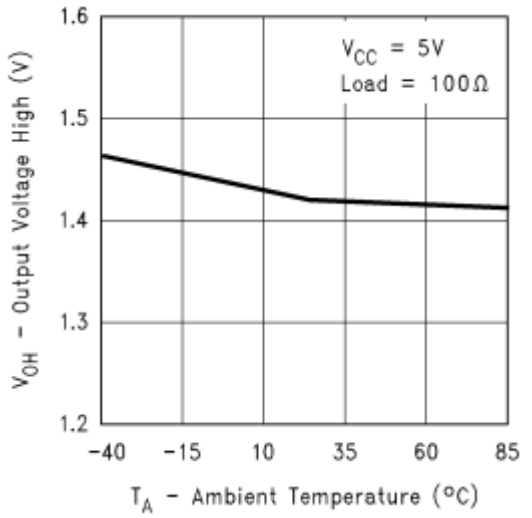
Differential Output Voltage VS. Power Supply



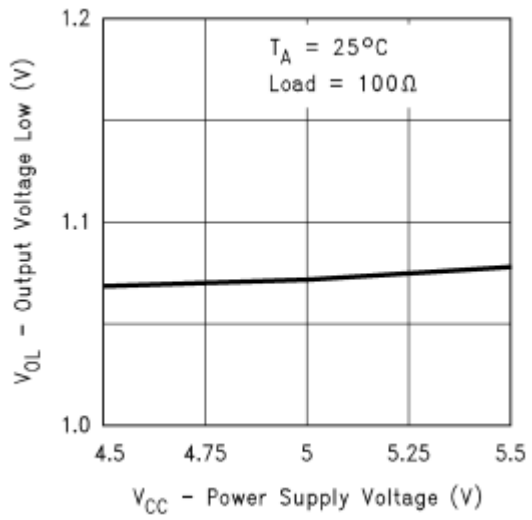
Differential Output VoltageVS. Temperature



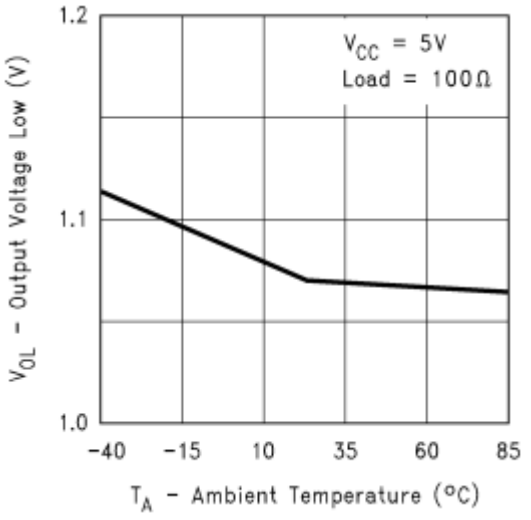
Output Voltage High VS. Power Supply



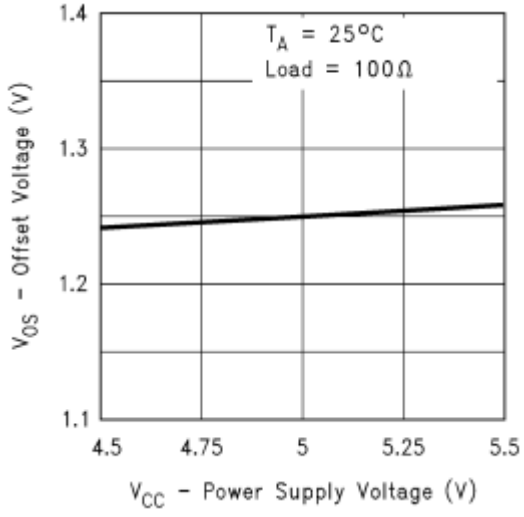
Output Voltage High VS. Temperature



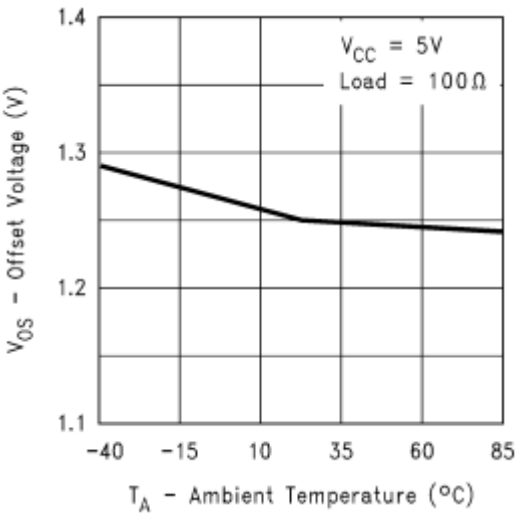
Output Voltage Low VS. Power Supply



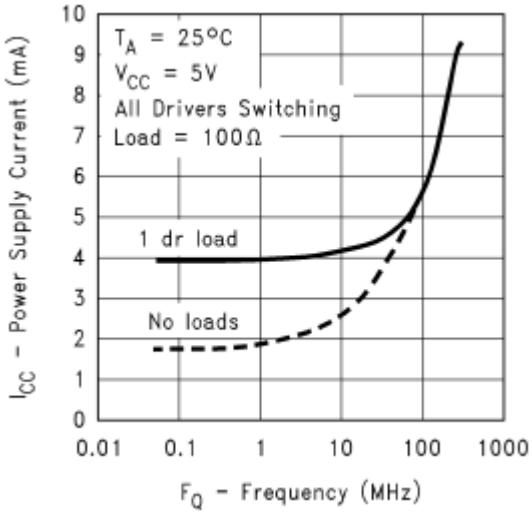
Output Voltage Low VS. Temperature



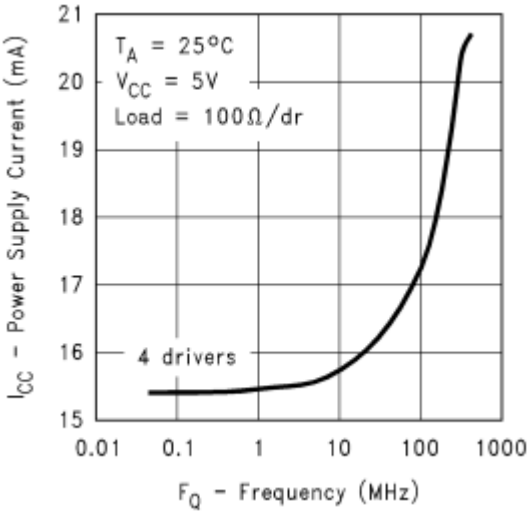
Offset Voltage VS. Power Supply



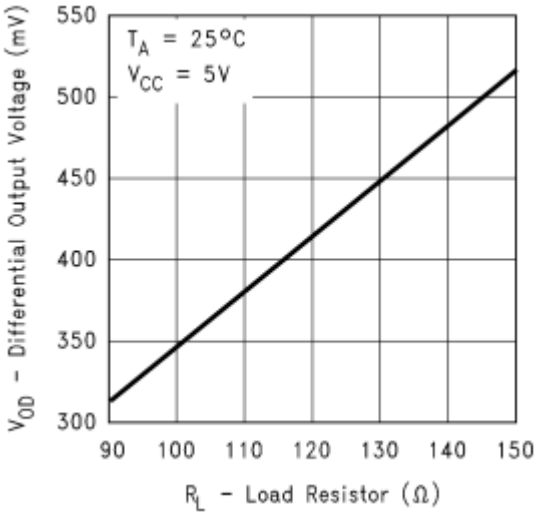
Offset Voltage VS. Temperature



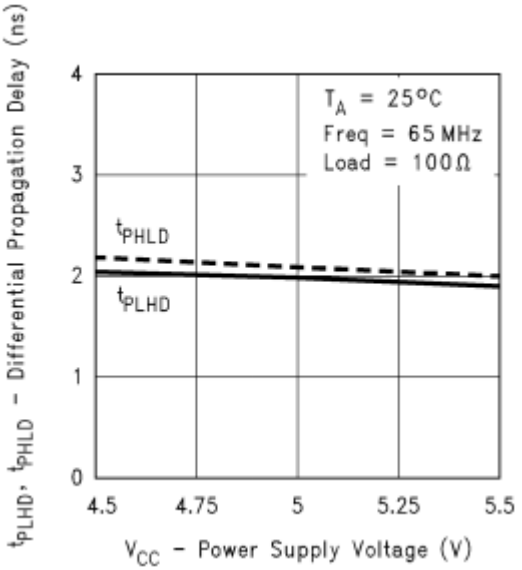
Power Supply Current VS. Operating Frequency



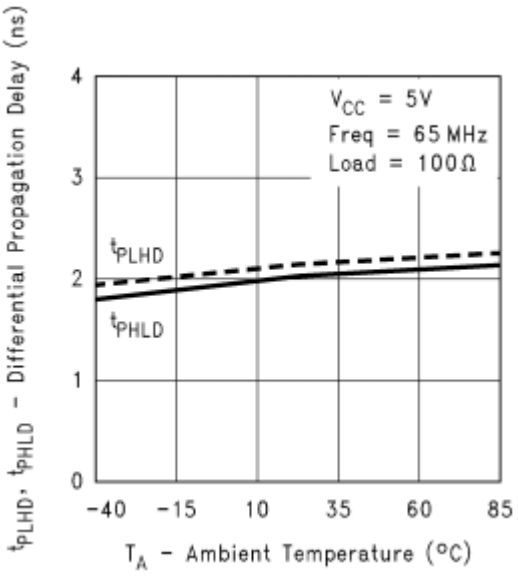
Power Supply Current VS. Operating Frequency



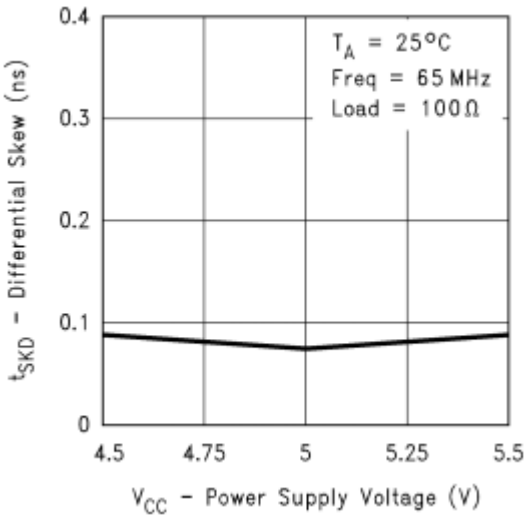
Differential Output Voltage VS. Load Resistor



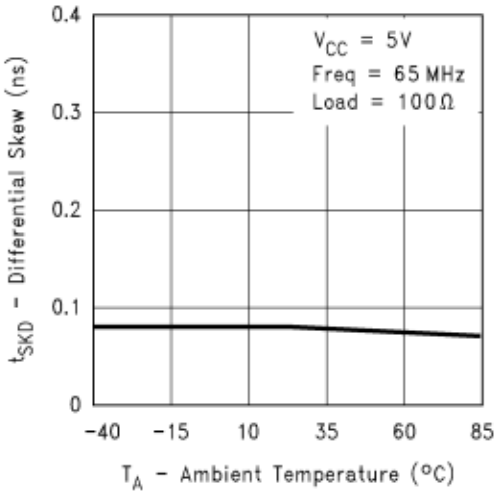
Differential Propagation Delay VS. Power Supply



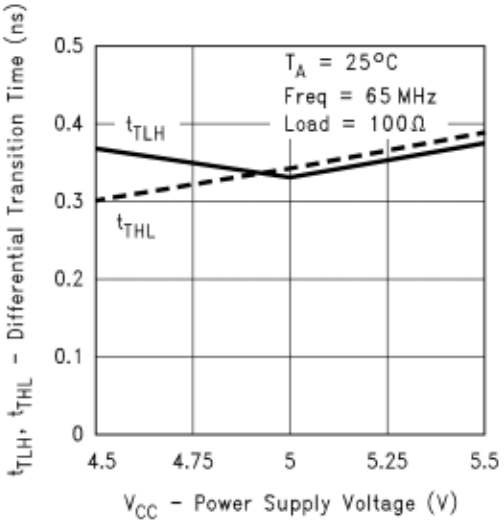
Differential Propagation Delay VS. Temperature



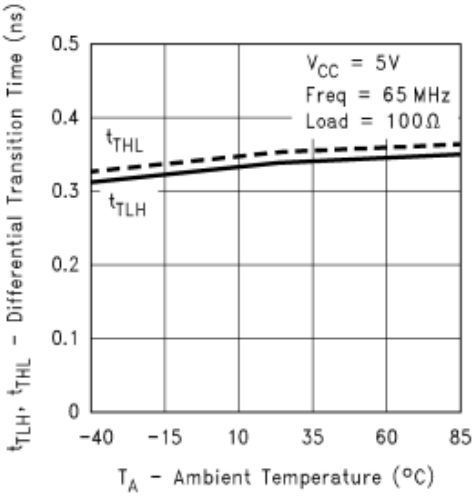
Differential Skew VS. Power Supply



Differential Skew VS. Temperature



Differential Transition Time VS. Power Supply



Differential Transition Time VS. Temperature

TYPICAL APPLICATION DIAGRAM

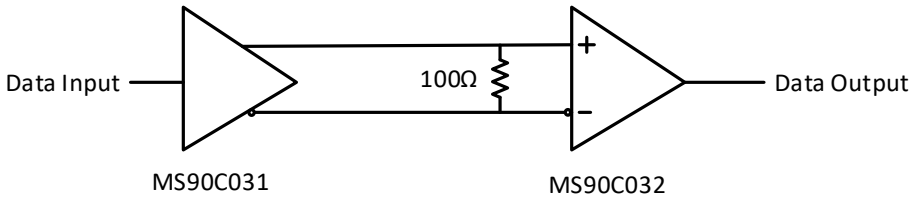


Figure 5. Typical Application Diagram

LVDS driver and receiver are mainly applied to simple point-to-point structure as shown in Figure 5. The structure provides a clean transmission channel for high-speed data rate signal. Transmission media can be twisted-pair, cable and PCB trace. The impedance of typical transmission media is less than 100Ω. In order to match the impedance of transmission media, 100Ω terminal resistor can be connected on differential input terminals. And it should be as close to the input terminal of the device as possible. The terminal resistor converts the current signal to voltage signal, thus to provide for the MS90C032. For other structures, such as multi-receiver, it should be considered that the impedance match of mid connector and cable interface and noise margin.

The MS90C031, differential bus driver is designed as current mode. The driver with current mode has high output impedance and outputs constant current within load range (while the driver with voltage mode outputs constant voltage within load range). When current flows from one direction of load, logic high level is generated; When current flows from opposite direction, logic low level is generated. The scaled output current is 3.4mA, minimum 2.5mA and maximum 4.5mA. When system is operating, a loop-circuit is needed to be connected as shown in Figure 5. On receiver terminal, 3.4mA loop-circuit current flows through a 100Ω resistor to generate 340mV differential voltage, which enables that the receiver terminal has 240mV noise margin (driving signal minus threshold on receiver terminal, 340mV-100mV=240mV). The common-mode point of differential LVDS signal is 1.2V(Vos) to ground. Figure 6 indicates the peak-to-peak value of steady-state voltage (Vss) is twice the differential voltage(Vod).

In operation, current-mode driver is superior to voltage-mode driver, such as RS-422. Current-mode driver could provide stable output current within wide frequency range. The output voltage like RS422 has obvious attenuation in 20MHz~40MHz range. This is caused by variation in switch current of internal gate circuit for voltage-mode driver, while the output current of current mode is fixed. This is similar to the operating modes of ECL and PECL devices, but without large current like ECL and PECL. Compare with similar PECL circuit,the required current of LVDS may less than 80%. The AC characteristics of the MS90C031 are 10 times superior to RS-422 voltage-mode driver.

When input is floating, internal protection circuit ensures that outputs are logic 0 (the true output is low level, the another is high level).

Tri-state output function can realize output high impedance, thus power dissipation is reduced when the driver is not operating.

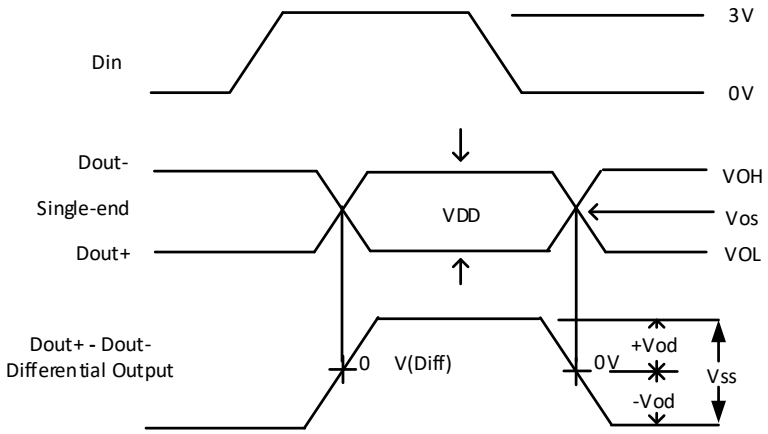
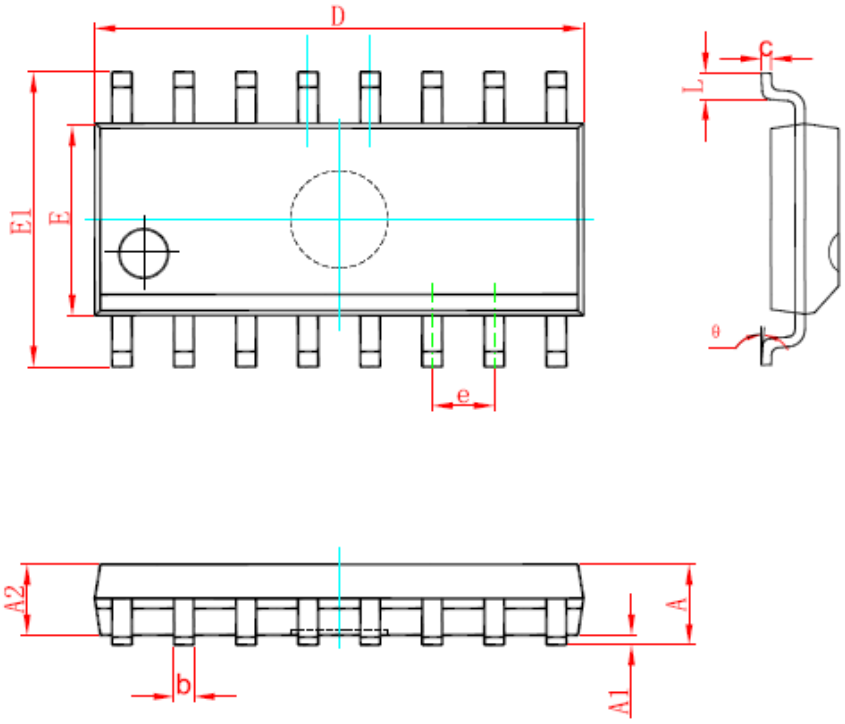


Figure 6. Driver Output Level

PACKAGE OUTLINE DIMENSIONS

SOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name: MS90C031

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS90C031	SOP16	2500	1	2500	8	20000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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