

Three Phase Brushless Motor Pre-driver

PRODUCT DESCRIPTION

The MS8829 is a three-phase brush-less motor driver chip, up to 35V operating voltage and 1.5A current.

The chip has functions of stall guard ,over temperature protection,and synchronous rectification. Internal synchronization allows the chip to reduce power consumption by turning on the appropriate power MOSFETS during current decay.

The chip has direction,brake,and PWM input to Control motor rotation,FG outputs the rotation states.

FEATURES

- Integrated 6 N-type Power MOSFETS,Rdson up+down=1.1Ω
- Synchronous Rectifier ,Shutdown Mode,Low Power
- Low Voltage Protection ,over Temperature Protection
- Hall Elements Input or Hall IC Input
- PWM Control Speed, Positive and Reverse Rotation Model
- FG Output
- 5V LDO Out
- Stall Guard Protection
- QFN24 Package



QFN24

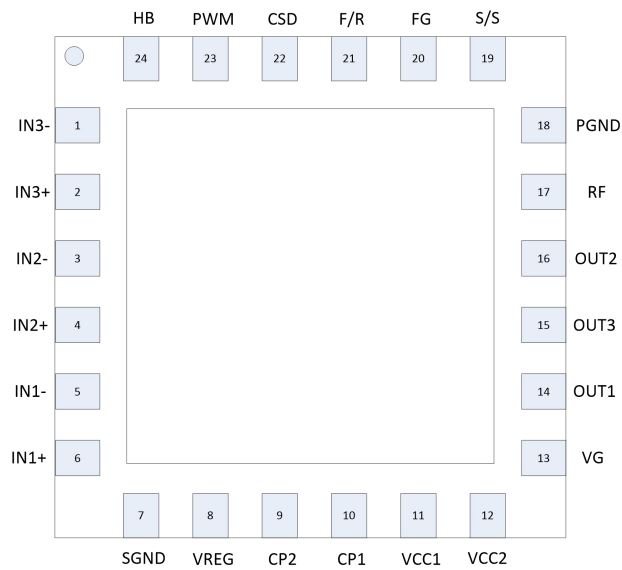
APPLICATIONS

- Laser Printer, Copier
- Power Rotate Tools
- Water Pump ,Gas Pump
- Monitoring Camera

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS8829	QFN24	MS8829

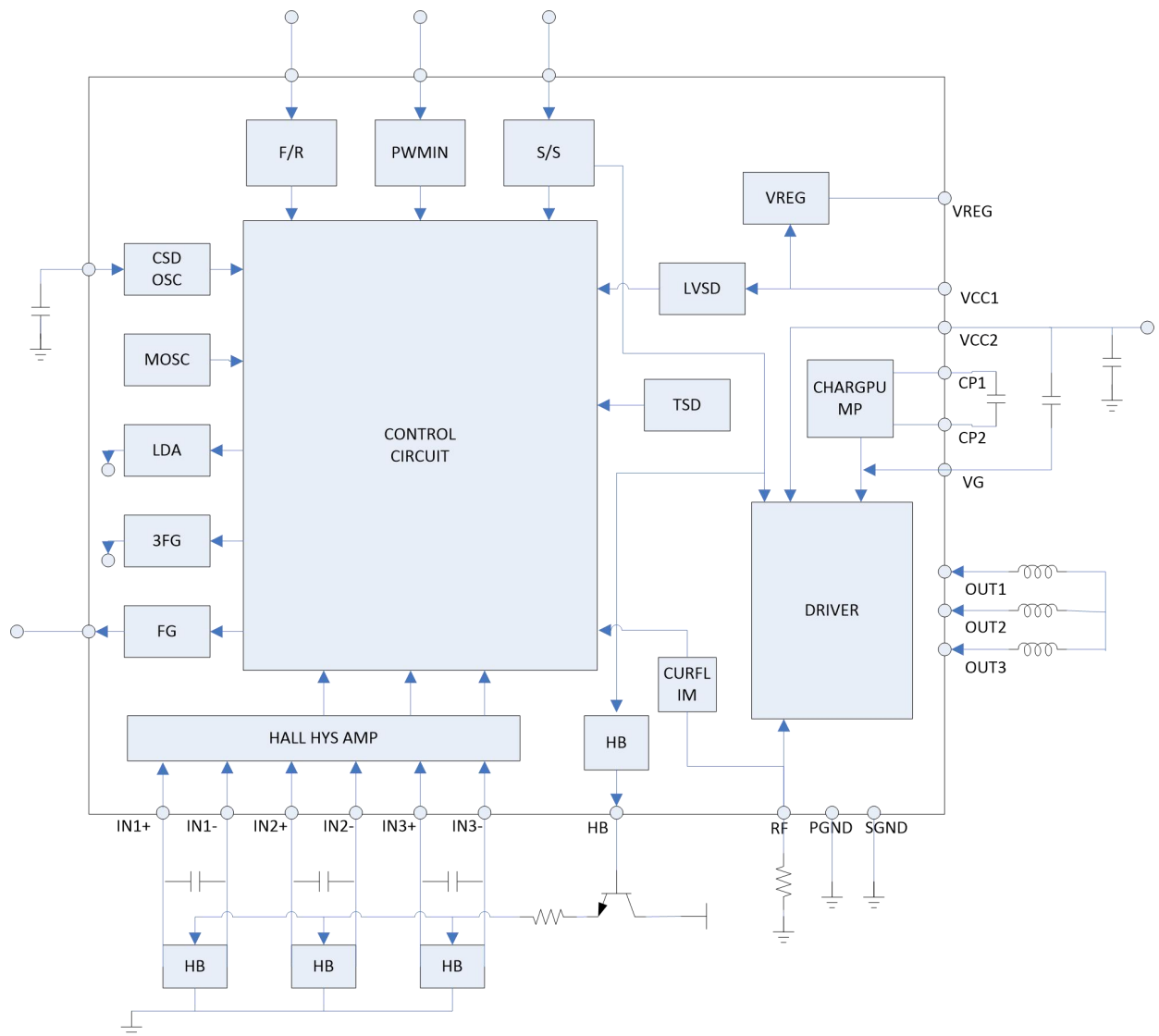
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	IN3-	I	HALL Input H: IN+>IN-; L: IN->IN+
2	IN3+		
3	IN2-		
4	IN2+		
5	IN1-		
6	IN1+		
7	GND	GND	Ground
8	VREG	O	5V LDO Out
9	CP2	O	Charge-pump Capacitor
10	CP1		
11	VCC1	POWER	Power for Inter Circuit
12	VCC2	POWER	Power for Half H Bridge
13	VG	I/O	Charge-pump Output
14	OUT1	O	H-bridge Low Side Output 1
15	OUT3		H-bridge Low Side Output 3
16	OUT2		H-bridge Low Side Output 2
17	RF	I/O	H-bridge Current Sense Pin
18	PGND	GND	Power Ground
19	SS	I	Motor Brake
20	FG	O	Hall Output(1 ϕ)
21	F/R	I	Rotate F/Rection
22	CSD	I/O	Stall Guard Capacitor
23	PWM	I	PWM Speed Control
24	HB	O	3.6V Hall Bias

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Supply Voltage	VCCmax	35	V
Charge-pump Voltage	VGmax	42	V
Max Output Current	I _{max}	1.5	A
Junction Temperature	T _{jmax}	150	°C
Operating Temperature Range	T _{opr}	-40 ~ 105	°C
LDO Output Current	I _{REG}	0 ~ -200	mA
FG Voltage	V _{FG}	0~6	V
FG Current	I _{FG}	0~14	mA

ELECTRICAL CHARACTERISTICS

(VCC=24V, TA = 25°C. Unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply current 1	ICC1			3.8	4.7	mA
Supply current 2	ICC2	Charge-pump on,output disable		0.89	1.1	mA
Output Driver						
Rdson,Downside	RON(L1)	IO=1A		0.47	0.65	Ω
Rdson,Upside	RON(H1)	IO=-1A		0.6	0.9	Ω
Downside Current Leakage	IL(L)				50	uA
Upside Current Leakage	IL(H)		-50			uA
Diode forward Voltage	VD(L1)	ID=-1A		0.73	1.3	V
5V VREG						
VREG Output Voltage	VREG	IO=-5mA	5.07	5.16	5.20	V
Line Regulation	ΔV(REG1)	VCC=8 to 35V, IO=-5mA			7	mV
Load Regulation	ΔV(REG2)	IO=-5mA to -10mA			0.4	mV
HALL Amplifier						
Hall Input Current	IB(HA)		-130			nA
Common Mode Input Range	VICM2	When use hall IC	0		VREG	V
Hall Input Range	VHIN	Sine waive input	80			mVp-p
Hall Input Hysteresis	ΔVIN(HA)			20		mV
Hall Input Threshold Up	VSLH			8		mV
Hall Input Threshold Down	VSHL			-12		mV

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CSD Oscillator						
CSD High Level	VOH(CSD)		3.03	3.07	3.10	V
CSD Low Level	VOL(CSD)		1.07	1.08	1.12	V
Amplitude	V(CSD)		2.0	2.0	2.0	Vp-p
External Capacitor Charge Current	ICHG1 (CSD)	VCHG1=2V	-11.1	-11.3	-11.4	uA
External Capacitor Discharge Current	ICHG2 (CSD)	VCHG2=2V	11.1	11.3	11.4	uA
Oscillator Frequency	F(CSD)	C=0.022uf		129		HZ
Charge-pump						
VG Voltage	VGOUT			VCC+5		V
Pump Frequency	F(CP)		42	50	70	KHZ
Inner PWM						
Oscillation Frequency	F(PWM)		41	51.5	62	KHZ
Current Limit						
Rf Pin Limit Voltage	VRF			0.21		V
Blank Time	Tblank			1.2		us
Over Temperature Protection						
Shutdown Temperature	TSD		146	154	148	℃
Hysteresis Width	△TSD		20	30	40	℃
Low Voltage Protection (5V VREG)						
Operation Voltage	VSD		4.17	4.17	4.15	V
Hysteresis Width	△VSD		0.3	0.31	0.29	V
Hall Bias HB						
HB Voltage	VHB	IHB=100uA	3.56	3.61	3.63	V
FG						
Output on Resistor	VOL(FG)	IFG=5mA		17	20	Ω
Leakage Current	IL(FG)	Vo=5V			10	uA
Logic Input Pins(SS, PWM,F/R)						
High Level Input Voltage	VIH		1.75		VREG	V
Low Level Input Voltage	VIL		0		1.65	V
Left Open DC Voltage	VIO			3/5*VR EG		V
Input Hysteresis Width	VIS		0.3	0.4	0.4	V
High Level Input Current	IIH	VSS=VREG	41	51	65	uA
Low Level Input Current	IIL	VSS=0V	-65	-76	-95	uA

Logic True Table

(IN="High" means $IN^+ > IN^-$), ("H"=SOURCE,"L"=SINK,M=OFF)

F/R=H			F/R=L			OUTPUT		
IN1	IN2	IN3	IN1	IN2	IN3	OUT1	OUT2	OUT3
H	L	H	L	H	L	L	H	M
H	L	L	L	H	H	L	M	H
H	H	L	L	L	H	M	L	H
L	H	L	H	L	H	H	L	M
L	H	H	H	L	L	H	M	L
L	L	H	H	H	L	M	H	L

FG

IN1	IN2	IN3	FG
H	L	H	H
H	L	L	H
H	H	L	H
L	H	L	L
L	H	H	L
L	L	H	L

SS,PWM

	SS	PWM
High or open	Active	Output off
low	STOP(short brake)	Output on

CSD Function

SS Set High	——>	Protection released and count reset(Initial reset)
F/R Switched	——>	Protection released and count reset
PWM 0% Duty	——>	Protection released and count reset
Low Voltage Protection	——>	Protection released and count reset
Over Temperature Protection	——>	Stop counting

FUNCTIONAL DESCRIPTION

Output Drive Circuit

This IC adopts a direct PWM drive method to reduce power loss in the output. It regulates the drive force of the motor by changing the output on duty. The output PWM switching is performed by the upper-side output transistor. The current regeneration route during the normal PWMOFF passes through the parasitic diode of the output DMOS. This IC performs synchronous rectification, and is intended to reduce heat generation compared to diode regeneration.

Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation $I = V_{RF}/R_f$ ($V_{RF}=0.21V$ (typical), R_f : current detection resistor). This circuit suppresses the output current by reducing the output on duty.

The current limiter circuit has an operation delay (approx. 1200ns) to detect reverse recovery current flowing in the diode due to the PWM operation, and prevent a malfunction of the current limiting operation. If the coil resistance of the motor is small, or the inductance is low, the current at startup (the state in which there is no back electromotive force generated in the motor) will change rapidly. As a result, the operation delay may sometimes cause the current limiting operation to take place at a value above the set current. In such case, it is necessary to set the current limit value while taking into consideration the increase in current due to the delay.

The PWM frequency in the current limiter circuit is determined by the internal reference oscillator, and is approximately 50kHz.

Speed Control Method

Pulses are input to the PWMIN pin, and the output can be controlled by varying the duty cycle of these pulses.

When a low-level input voltage is applied to PWMIN pin, the output at the PWM side (upper side) is set to ON.

When a high-level input voltage is applied to PWMIN pin, the output at the PWM side (upper side) is set to OFF.

If it is necessary to input pulses using inverted logic, this can be done by adding an external transistor (NPN).

When the input to the PWMIN pin remains high-level for a certain period, the IC judges that the duty is 0%, causing the CSD circuit count to be reset.

Constraint Protection Circuit

The MS8829 includes a constraint protection circuit for protecting the IC and the motor in a motor constraint mode. This circuit operates when the motor is in an operation condition and the Hall signal does not switch over for a certain period. Note that while this constraint protection is operating, the upper-side output transistor will be OFF.

Time setting is performed according to the capacitance of the capacitor connected to the CSD pin.

Set time (s) $\approx 90 \times C$ (μF)

When a 0.022 μF capacitor is connected, the protection time becomes approximately 2.0 seconds. The set time must be selected to a value that provides adequate margin with respect to the motor startup time.

Conditions for releasing the constraint protection state:

- When the S/S pin is in a STOP state → Protection released and count reset (Initial reset)
- When the F/R pin is switched → Protection released and count reset
- When 0% duty is detected at the PWMIN pin input → Protection released and count reset
- When low-voltage condition is detected → Protection released and count reset (Initial reset)
- When TSD condition is detected → Stop counting

The CSD pin also functions as the initial reset pulse generation pin. If it is connected to ground, the logic circuit will go into a reset state, preventing speed control from taking place. Consequently, when not using constraint protection, connect a resistor of approximately 220kΩ and a capacitor of about 4700pF in parallel to ground.

Low-voltage Protection Circuit

The MS8829 incorporates a comparator that uses the band gap voltage as the reference. The circuit monitors the voltage at the VREG pin (5V) while the S/S pin is low and activates the protection circuit when the voltage at the VREG pin falls below 4.15V (typ.).

When this happens, the state of the output transistors for all phases set to OFF.

Charge-Pump

The charge-pump is used to generate a gate supply greater than the VCC in order to drive the source-side DMOS gates.

A 0.22 uF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes.

A 0.22 uF ceramic capacitor is required between VG and VCC to act as a reservoir to operate the high-side DMOS devices.

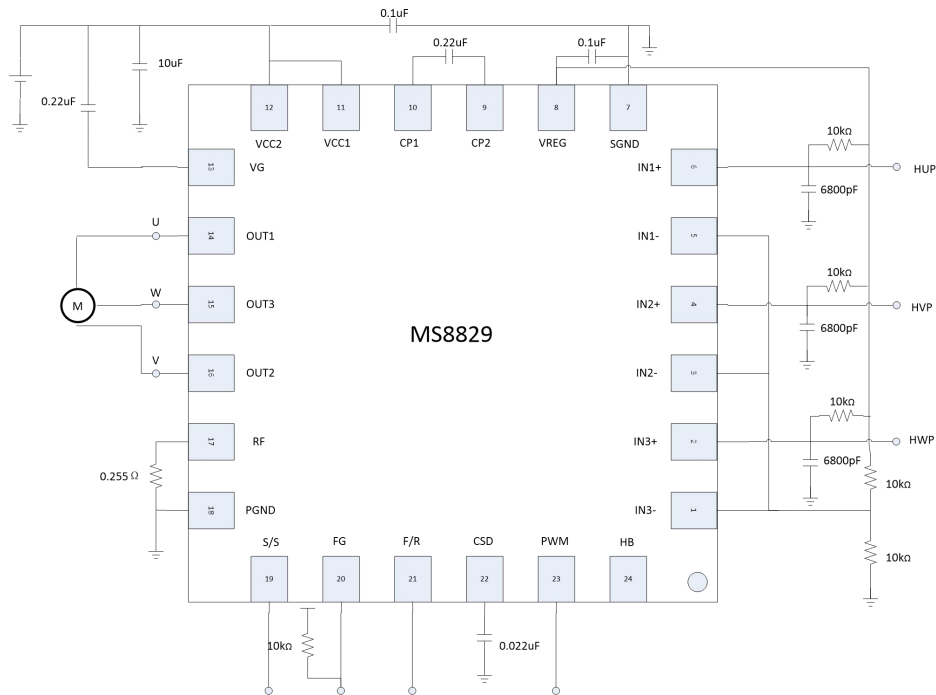
Thermal Shutdown Circuit

When the IC junction temperature exceeds 165°C (design target value), the thermal shutdown circuit is activated, and all the output transistors are set to OFF.

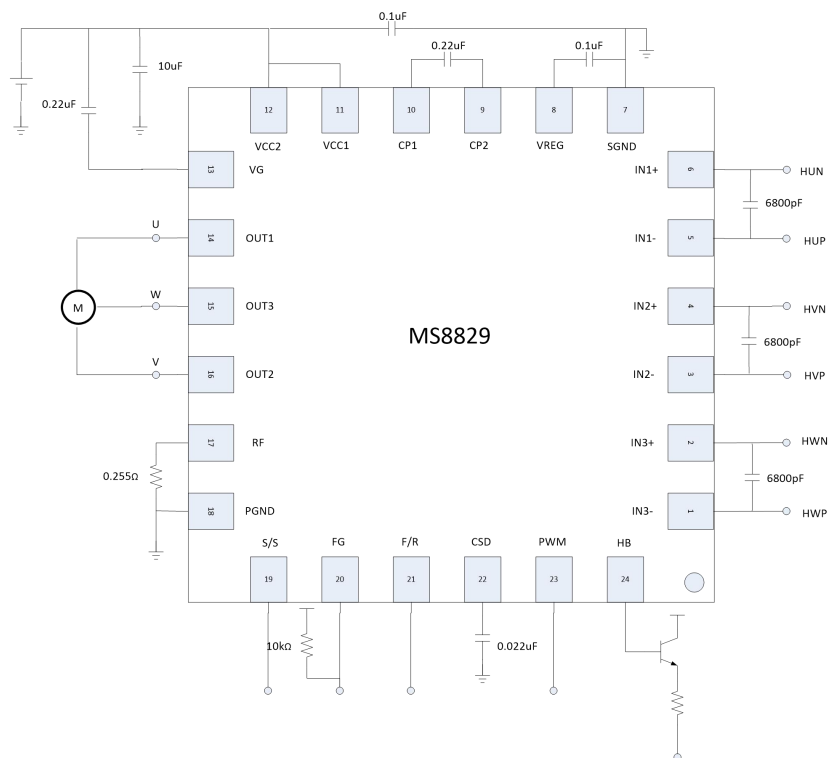
Hall Input Signal

A pulse input with the amplitude in excess of the hysteresis (35mV maximum) is required for the Hall inputs. It is desirable that the amplitude of the Hall input signal be 100mVp-p or more in consideration of the effect of noise and phase displacement.

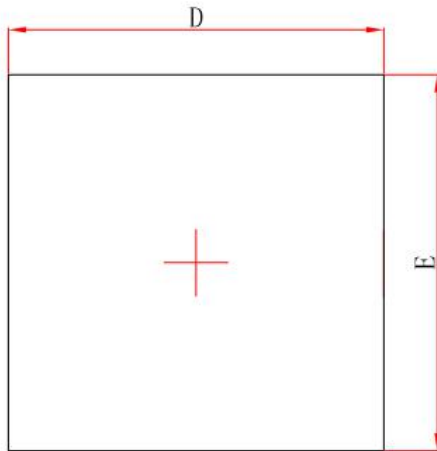
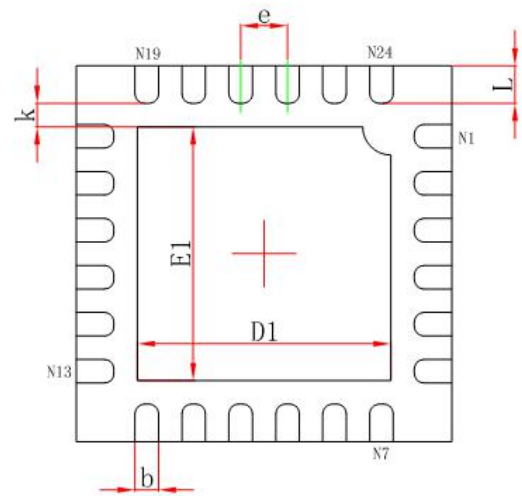
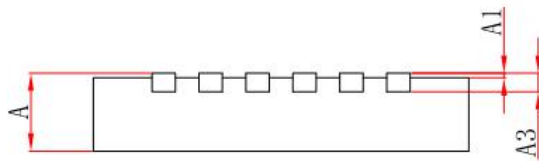
TYPICAL APPLICATION DIAGRAM



With Hall IC



With Hall element

PACKAGE OUTLINE DIMENSIONS
QFN24

Top View

Bottom View

Side View

Symbol	Millimeter		Inch	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN		0.008MIN	
b	0.180	0.300	0.007	0.012
e	0.500TYP		0.020TYP	
L	0.300	0.500	0.012	0.020

MARKING and PACKAGING SPECIFICATIONS**1. Marking Drawing Description**

Product Name: MS8829

Product Code : XXXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS8829	QFN24	4000	1	4000	8	32000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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