

High-speed, Low Power Dissipation DAC

PRODUCT DESCRIPTION

The MS9708/MS9714 is a 8bit/14bit high-speed and low power dissipation DAC. When sample rate reaches 125MSPS, the MS9708/MS9714 can also provide perfect AC and DC characteristics.

The DVDD normal operating voltage ranges from +1.8V to +5.5V and the AVDD normal operating voltage ranges from +2.7V to +5.5V. The feature of low power dissipation can make it suitable for portable and low power dissipation products.

The MS9708/MS9714 adopts a segmented current source architecture and specialized switch technique, in order to reduce parasitic effect and improve dynamic characteristics. Edge-triggered latch and temperature compensated bandgap reference are integrated together so as to get a complete monolithic DAC solution. Full-scale current output is 20mA and output impedance is more than 100kΩ.

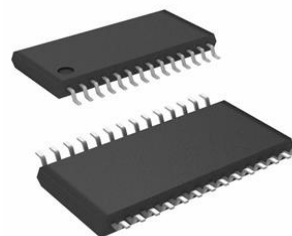
Complementary current output provides single-end or differential applications. Current output terminal can be connected with two output resistors, achieving two complementary, single-ended voltage outputs.

The MS9708/MS9714 includes a 1.2V internal reference and reference current control amplifier, which can set full-scale current by adjusting external resistor. The MS9708/MS9714 can also connect with external reference. The output current is from 2mA to 20mA without affecting dynamic characteristics.

The MS9708/MS9714 is available in TSSOP28 package.

FEATURES

- 8bit Resolution (MS9708), 14bit Resolution (MS9714)
- Update Rate: 125MSPS
- Power Dissipation: 190mW @ 5V; 45mW @ 3V
- Internal Reference: 1.2V
- Edge-Triggered Latch
- TSSOP28 Package



TSSOP28

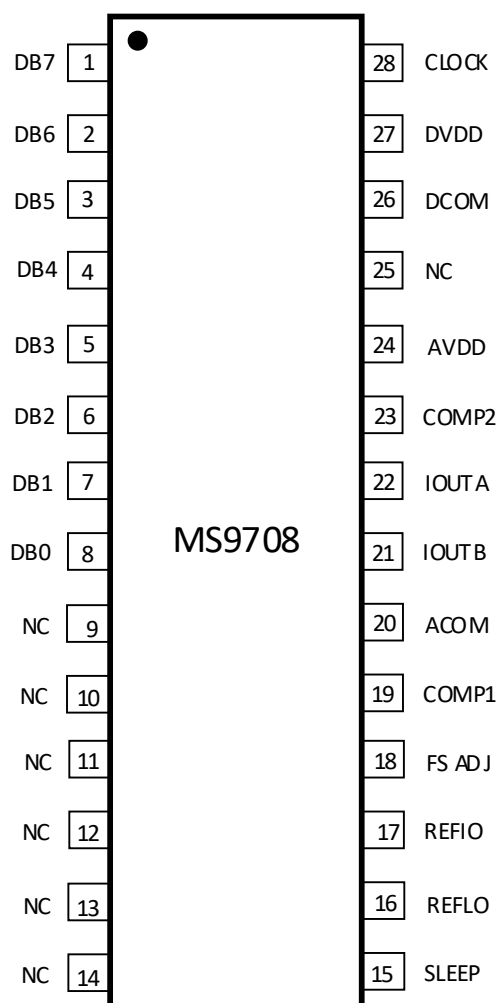
APPLICATIONS

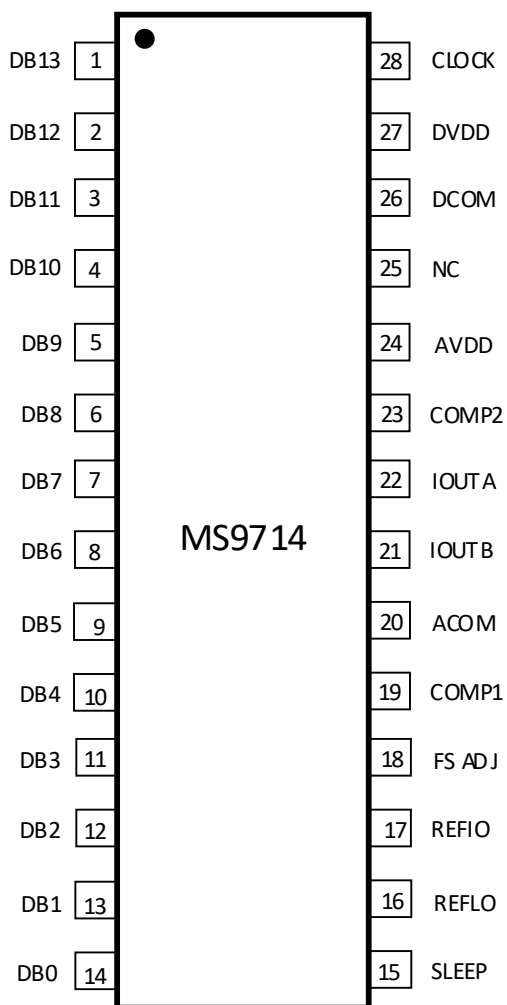
- Communication
- Signal Reconstruction
- Portable Device

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS9708	TSSOP28	MS9708
MS9714	TSSOP28	MS9714

PIN CONFIGURATION

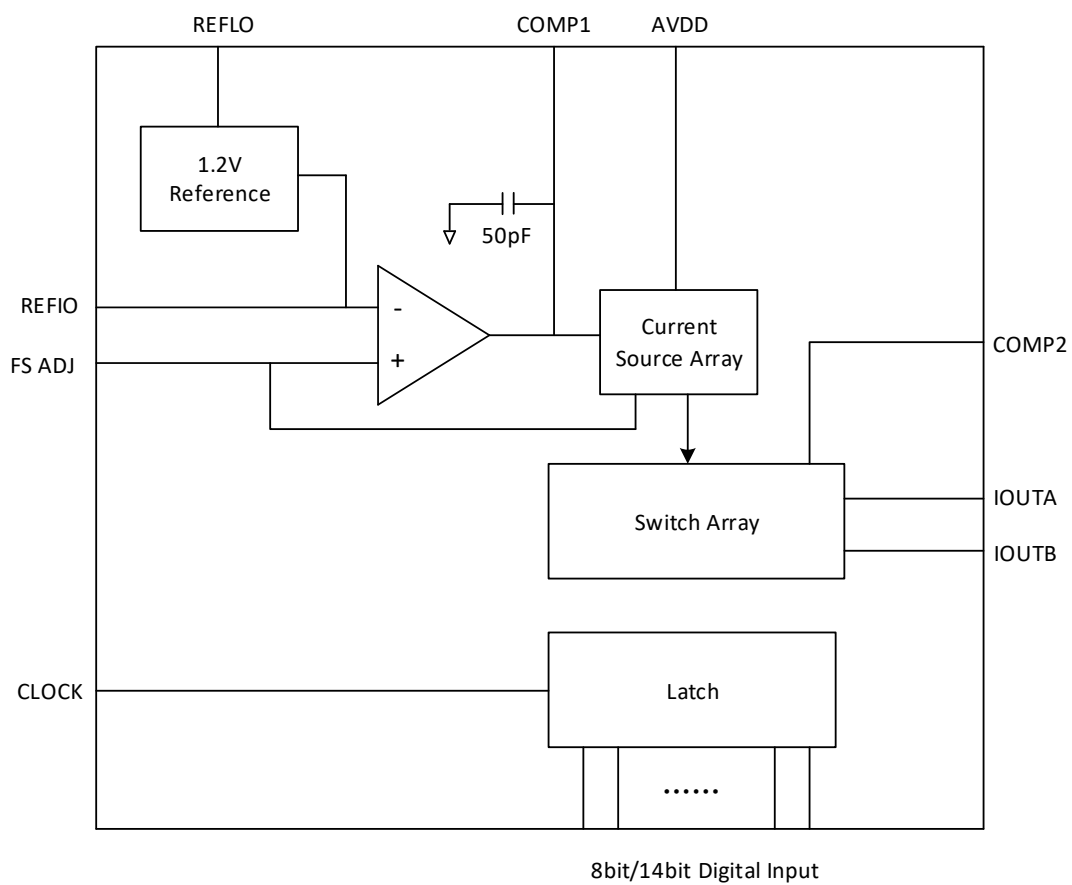




PIN DESCRIPTION

Pin	Name	Type	Description
1-7	DB7-DB0	I	Digital Data Input (MS9708)
1-14	DB13-DB0	I	Digital Data Input (MS9714)
-	NC	-	Not Connection
15	SLEEP	I	Low Power Dissipation Control Input, Activate High. Interior includes valid pull-down circuit, float when it is not used.
16	REFLO	I	When 1.2V internal reference is used, it is connect to reference ground. When it is connected to AVDD, internal reference is disabled.
17	REFIO	IO	Reference Input or Output. It is as reference input when internal reference is inactivate (for example, REFLO is connected to AVDD). It is as 1.2V reference output when internal reference is activate (for example, REFLO is connected to ACOM) and 0.1μF capacitor is externally connected to ACOM at this time.
18	FS ADJ	I	Full-scale Current Output Adjustment
19	COMP1	O	Bandwidth/ Noise Reduce Pin. Best effect is get by AVDD connected with 0.1μF capacitor.
20	ACOM	-	Analog Ground
21	IOUTB	O	Complementary DAC Current Output. When DB7~DB0/DB13~DB0 inputs are all 0, there is the maximum output.
22	IOUTA	O	DAC Current Output. When DB7~DB0/DB13~DB0 inputs are all 1, there is the maximum output.
23	COMP2	O	Internal Bias Point of Switch Driver Circuit. ACOM is connected with 0.1μF decouple capacitor.
24	AVDD	-	Analog Power Supply (+2.7V to +5.5V Valid)
26	DCOM	-	Digital Ground
27	DVDD	-	Digital Power Supply (+1.8V to +5.5V Valid)
28	CLOCK	I	Clock Input. Digital latch is valid on the rising edge of CLOCK.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Reference Point	Ratings	Unit
AVDD	ACOM	-0.3 ~ +6.5	V
DVDD	DCOM	-0.3 ~ +6.5	V
ACOM	DCOM	-0.3 ~ +0.3	V
AVDD	DVDD	-6.5 ~ +6.5	V
CLOCK,SLEEP	DCOM	-0.3 ~ DVDD+0.3	V
Digital Input	DCOM	-0.3 ~ DVDD+0.3	V
IOUTA, IOUTB	ACOM	-1.0~ AVDD+0.3	V
COMP1, COMP2	ACOM	-0.3 ~ AVDD+0.3	V
REFIO, FS ADJ	ACOM	-0.3 ~ AVDD+0.3	V
REFLO	ACOM	-0.3 ~ +0.3	V
Maximum Junction Temperature	T _{JMAX}	+150	°C
Storage Temperature	T _{STG}	-65 ~ +150	°C
Soldering Temperature (10s)	T _{SOLDER}	260	°C

Thermal Resistor

Parameter	Symbol	Value	Unit
Junction to Ambient	R _{θJA}	77.09	°C/W
Junction to Package Cover	R _{θJC}	23.49	°C/W

ELECTRICAL CHARACTERISTICS

DC Characteristics

Unless other noted, AVDD=+5V, DVDD=+5V. I_{OUTFS}=20mA, T_A=25°C.

Parameter	MS9708			MS9714			Unit
	Min	Typ	Max	Min	Typ	Max	
Resolution		8			14		Bit
DC Precision ¹							
INL	-0.25	±0.1	+0.25	-8	±4	+8	LSB
DNL	-0.25	±0.1	+0.25	-4	±2	+4	LSB
Analog Output							
Offset Error	-0.025		+0.025	-0.025		+0.025	% of FSR
Gain Error (Without internal reference)		±2			±2		% of FSR
Gain Error (With internal reference)	-5	±1	+5	-5	±1	+5	% of FSR
Full-scale Output Current ²	2		20	2		20	mA
Output Voltage Default Range	-1		1.25	-1		1.25	V
Output Resistance		100			100		kΩ
Output Capacitance		5			5		pF
Reference Output							
Reference Voltage	1.08	1.20	1.32	1.08	1.20	1.32	V
Reference Output Current ³		100			100		nA
Reference Input							
Input Voltage Range	0.1		1.25	0.1		1.25	V
Reference Input Resistance		1			1		MΩ
Small-signal Bandwidth (W/O C _{COMP1}) ⁴		0.4			0.4		MHz
Temperature Coefficient							
Zero Temperature Drift		0			0		ppm of FSR/°C
Gain Temperature Drift (Without internal reference)		±50			±50		ppm of FSR/°C

Parameter	MS9708			MS9714			Unit
	Min	Typ	Max	Min	Typ	Max	
Gain Temperature Drift (With internal reference)		±100			±100		ppm of FSR/°C
Reference Voltage Temperature Drift		±50			±50		ppm/°C
Power							
AVDD Power Supply ⁵	2.7	5	5.5	2.7	5	5.5	V
DVDD Power Supply	1.8	5	5.5	1.8	5	5.5	V
Analog Power Supply Current (I _{AVDD})		25	30		25	30	mA
Digital Power Supply Current (I _{DVDD}) ⁶		3	6		3	6	mA
Current in Sleep Mode (I _{AVDD})			8.5			8.5	mA
Power Dissipation ⁶ (5V, I _{OUTFS} =20mA)		140			140		mW
Power Dissipation ⁷ (5V, I _{OUTFS} =20mA)		190			190		mW
Power Dissipation ⁷ (3V, I _{OUTFS} =2mA)		45			45		mW
Power Supply Rejection Ratio - AVDD	-0.4		+0.4	-0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio - DVDD	-0.025		+0.025	-0.025		+0.025	% of FSR/V
Operating Temperature	-40		+85	-40		+85	°C

Note:

1. Measured on IOUTA.
2. Normally, full-scale current is I_{OUTFS}=32×I_{REF}.
3. Use an external buffer amplifier to drive any external load.
4. Reference bandwidth is a function of external capacitance on COMP1 pin. The current value is measured on COMP1 pin without external capacitor.
5. When actual input is less than 3V, output current is recommended to reduce to 12mA or less to maintain optimum performance.
6. Measured when f_{CLOCK}=50 MSPS and f_{OUT}=1.0 MHz.
7. Measured when unbuffered voltage is output into 50Ω R_{LOAD} on IOUTA and IOUTB pins, f_{CLOCK}=100 MSPS and f_{OUT}=40 MHz.

Dynamic Characteristics

Unless other noted, AVDD=+5V, DVDD=+5V, I_{OUTFS}=20mA, Singe-ended output, IOUTA, 50Ω doubly terminated, T_A=25°C.

Parameter	MS9708			MS9714			Unit
	Min	Typ	Max	Min	Typ	Max	
Dynamic Characteristic							
Maximum Output Update Frequency (f _{CLOCK})	100	125		100	125		MSPS
Output Settling Time (t _{ST}) (to 0.1%) ¹		35			35		ns
Output Propagation Delay (t _{PD})		1			1		ns
Glitch Pulse		5			5		pV-s
Output Rise Time (10% ~ 90%) ¹		2.5			2.5		ns
Output Fall Time (10% ~ 90%) ¹		2.5			2.5		ns
Output Noise (I _{OUTFS} =20mA)		50			50		pA/√Hz
Output Noise (I _{OUTFS} =2mA)		30			30		pA/√Hz
AC Characteristic							
Signal-to-Noise and Distortion Ratio							
f _{CLOCK} =10MSPS; f _{OUT} =1.00MHz		55			63		dB
f _{CLOCK} =50MSPS; f _{OUT} =1.00MHz		50			60		dB
f _{CLOCK} =50MSPS; f _{OUT} =12.51MHz		48			50		dB
f _{CLOCK} =100MSPS; f _{OUT} =5.01MHz		53			61		dB
f _{CLOCK} =100MSPS; f _{OUT} =25.01MHz		48			50		dB
Total Harmonic Distortion							
f _{CLOCK} =10MSPS; f _{OUT} =1.00MHz		-66			-67		dBc
f _{CLOCK} =50MSPS; f _{OUT} =1.00MHz		-65			-69		dBc
f _{CLOCK} =50MSPS; f _{OUT} =12.51MHz		-50			-52		dBc
f _{CLOCK} =100MSPS; f _{OUT} =5.01MHz		-64			-69		dBc
f _{CLOCK} =100MSPS; f _{OUT} =25.01MHz		-51			-47		dBc

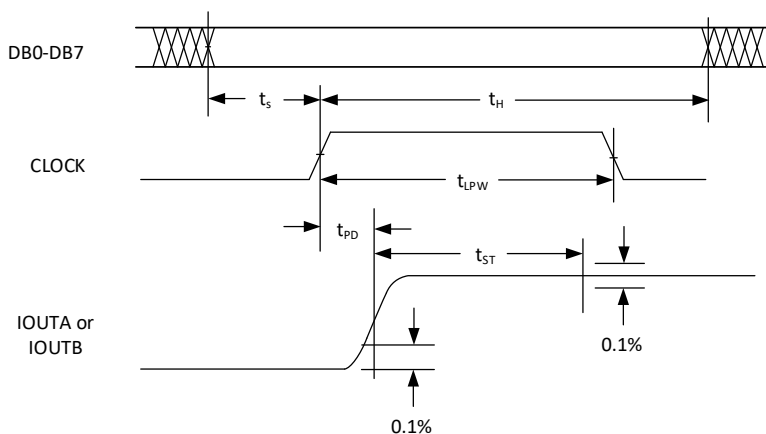
Parameter	MS9708			MS9714			Unit
	Min	Typ	Max	Min	Typ	Max	
Spurious-Free Dynamic Range							
f _{CLOCK} =10MSPS; f _{OUT} =1.00MHz		70			71		dBc
f _{CLOCK} =50MSPS; f _{OUT} =1.00MHz		69			72		dBc
f _{CLOCK} =50MSPS; f _{OUT} =12.51MHz		53			54		dBc
f _{CLOCK} =100MSPS; f _{OUT} =5.01MHz		67			72		dBc
f _{CLOCK} =100MSPS; f _{OUT} =25.01MHz		55			52		dBc

Note 1: Measured only when load is 50Ω.

Digital Characteristic

Unless other noted, AVDD=+5V, DVDD=+5V, IOUTFS=20mA, TA=25°C.

Access Other Notes: [AVDD](#), [DVDD](#), [IOVDD](#), [IOVDD2](#), [VDD](#), [VDD2](#), [VDD3](#), [VDD4](#), [VDD5](#), [VDD6](#), [VDD7](#), [VDD8](#), [VDD9](#), [VDD10](#), [VDD11](#), [VDD12](#), [VDD13](#), [VDD14](#), [VDD15](#), [VDD16](#), [VDD17](#), [VDD18](#), [VDD19](#), [VDD20](#), [VDD21](#), [VDD22](#), [VDD23](#), [VDD24](#), [VDD25](#), [VDD26](#), [VDD27](#), [VDD28](#), [VDD29](#), [VDD30](#), [VDD31](#), [VDD32](#), [VDD33](#), [VDD34](#), [VDD35](#), [VDD36](#), [VDD37](#), [VDD38](#), [VDD39](#), [VDD40](#), [VDD41](#), [VDD42](#), [VDD43](#), [VDD44](#), [VDD45](#), [VDD46](#), [VDD47](#), [VDD48](#), [VDD49](#), [VDD50](#), [VDD51](#), [VDD52](#), [VDD53](#), [VDD54](#), [VDD55](#), [VDD56](#), [VDD57](#), [VDD58](#), [VDD59](#), [VDD60](#), [VDD61](#), [VDD62](#), [VDD63](#), [VDD64](#), [VDD65](#), [VDD66](#), [VDD67](#), [VDD68](#), [VDD69](#), [VDD70](#), [VDD71](#), [VDD72](#), [VDD73](#), [VDD74](#), [VDD75](#), [VDD76](#), [VDD77](#), [VDD78](#), [VDD79](#), [VDD80](#), [VDD81](#), [VDD82](#), [VDD83](#), [VDD84](#), [VDD85](#), [VDD86](#), [VDD87](#), [VDD88](#), [VDD89](#), [VDD90](#), [VDD91](#), [VDD92](#), [VDD93](#), [VDD94](#), [VDD95](#), [VDD96](#), [VDD97](#), [VDD98](#), [VDD99](#), [VDD100](#), [VDD101](#), [VDD102](#), [VDD103](#), [VDD104](#), [VDD105](#), [VDD106](#), [VDD107](#), [VDD108](#), [VDD109](#), [VDD110](#), [VDD111](#), [VDD112](#), [VDD113](#), [VDD114](#), [VDD115](#), [VDD116](#), [VDD117](#), [VDD118](#), [VDD119](#), [VDD120](#), [VDD121](#), [VDD122](#), [VDD123](#), [VDD124](#), [VDD125](#), [VDD126](#), [VDD127](#), [VDD128](#), [VDD129](#), [VDD130](#), [VDD131](#), [VDD132](#), [VDD133](#), [VDD134](#), [VDD135](#), [VDD136](#), [VDD137](#), [VDD138](#), [VDD139](#), [VDD140](#), [VDD141](#), [VDD142](#), [VDD143](#), [VDD144](#), [VDD145](#), [VDD146](#), [VDD147](#), [VDD148](#), [VDD149](#), [VDD150](#), [VDD151](#), [VDD152](#), [VDD153](#), [VDD154](#), [VDD155](#), [VDD156](#), [VDD157](#), [VDD158](#), [VDD159](#), [VDD160](#), [VDD161](#), [VDD162](#), [VDD163](#), [VDD164](#), [VDD165](#), [VDD166](#), [VDD167](#), [VDD168](#), [VDD169](#), [VDD170](#), [VDD171](#), [VDD172](#), [VDD173](#), [VDD174](#), [VDD175](#), [VDD176](#), [VDD177](#), [VDD178](#), [VDD179](#), [VDD180](#), [VDD181](#), [VDD182](#), [VDD183](#), [VDD184](#), [VDD185](#), [VDD186](#), [VDD187](#), [VDD188](#), [VDD189](#), [VDD190](#), [VDD191](#), [VDD192](#), [VDD193](#), [VDD194](#), [VDD195](#), [VDD196](#), [VDD197](#), [VDD198](#), [VDD199](#), [VDD200](#), [VDD201](#), [VDD202](#), [VDD203](#), [VDD204](#), [VDD205](#), [VDD206](#), [VDD207](#), [VDD208](#), [VDD209](#), [VDD210](#), [VDD211](#), [VDD212](#), [VDD213](#), [VDD214](#), [VDD215](#), [VDD216](#), [VDD217](#), [VDD218](#), [VDD219](#), [VDD220](#), [VDD221](#), [VDD222](#), [VDD223](#), [VDD224](#), [VDD225](#), [VDD226](#), [VDD227](#), [VDD228](#), [VDD229](#), [VDD230](#), [VDD231](#), [VDD232](#), [VDD233](#), [VDD234](#), [VDD235](#), [VDD236](#), [VDD237](#), [VDD238](#), [VDD239](#), [VDD240](#), [VDD241](#), [VDD242](#), [VDD243](#), [VDD244](#), [VDD245](#), [VDD246](#), [VDD247](#), [VDD248](#), [VDD249](#), [VDD250](#), [VDD251](#), [VDD252](#), [VDD253](#), [VDD254](#), [VDD255](#), [VDD256](#), [VDD257](#), [VDD258](#), [VDD259](#), [VDD260](#), [VDD261](#), [VDD262](#), [VDD263](#), [VDD264](#), [VDD265](#), [VDD266](#), [VDD267](#), [VDD268](#), [VDD269](#), [VDD270](#), [VDD271](#), [VDD272](#), [VDD273](#), [VDD274](#), [VDD275](#), [VDD276](#), [VDD277](#), [VDD278](#), [VDD279](#), [VDD280](#), [VDD281](#), [VDD282](#), [VDD283](#), [VDD284](#), [VDD285](#), [VDD286](#), [VDD287](#), [VDD288](#), [VDD289](#), [VDD290](#), [VDD291](#), [VDD292](#), [VDD293](#), [VDD294](#), [VDD295](#), [VDD296](#), [VDD297](#), [VDD298](#), [VDD299](#), [VDD300](#), [VDD301](#), [VDD302](#), [VDD303](#), [VDD304](#), [VDD305](#), [VDD306](#), [VDD307](#), [VDD308](#), [VDD309](#), [VDD310](#), [VDD311](#), [VDD312](#), [VDD313](#), [VDD314](#), [VDD315](#), [VDD316](#), [VDD317](#), [VDD318](#), [VDD319](#), [VDD320](#), [VDD321](#), [VDD322](#), [VDD323](#), [VDD324](#), [VDD325](#), [VDD326](#), [VDD327](#), [VDD328](#), [VDD329](#), [VDD330](#), [VDD331](#), [VDD332](#), [VDD333](#), [VDD334](#), [VDD335](#), [VDD336](#), [VDD337](#), [VDD338](#), [VDD339](#), [VDD340](#), [VDD341](#), [VDD342](#), [VDD343](#), [VDD344](#), [VDD345](#), [VDD346](#), [VDD347](#), [VDD348](#), [VDD349](#), [VDD350](#), [VDD351](#), [VDD352](#), [VDD353](#), [VDD354](#), [VDD355](#), [VDD356](#), [VDD357](#), [VDD358](#), [VDD359](#), [VDD360](#), [VDD361](#), [VDD362](#), [VDD363](#), [VDD364](#), [VDD365](#), [VDD366](#), [VDD367](#), [VDD368](#), [VDD369](#), [VDD370](#), [VDD371](#), [VDD372](#), [VDD373](#), [VDD374](#), [VDD375](#), [VDD376](#), [VDD377](#), [VDD378](#), [VDD379](#), [VDD380](#), [VDD381](#), [VDD382](#), [VDD383](#), [VDD384](#), [VDD385](#), [VDD386](#), [VDD387](#), [VDD388](#), [VDD389](#), [VDD390](#), [VDD391](#), [VDD392](#), [VDD393](#), [VDD394](#), [VDD395](#), [VDD396](#), [VDD397](#), [VDD398](#), [VDD399](#), [VDD400](#), [VDD401](#), [VDD402](#), [VDD403](#), [VDD404](#), [VDD405](#), [VDD406](#), [VDD407](#), [VDD408](#), [VDD409](#), [VDD410](#), [VDD411](#), [VDD412](#), [VDD413](#), [VDD414](#), [VDD415](#), [VDD416](#), [VDD417](#), [VDD418](#), [VDD419](#), [VDD420](#), [VDD421](#), [VDD422](#), [VDD423](#), [VDD424](#), [VDD425](#), [VDD426](#), [VDD427](#), [VDD428](#), [VDD429](#), [VDD430](#), [VDD431](#), [VDD432](#), [VDD433](#), [VDD434](#), [VDD435](#), [VDD436](#), [VDD437](#), [VDD438](#), [VDD439](#), [VDD440](#), [VDD441](#), [VDD442](#), [VDD443](#), [VDD444](#), [VDD445](#), [VDD446](#), [VDD447](#), [VDD448](#), [VDD449](#), [VDD450](#), [VDD451](#), [VDD452](#), [VDD453](#), [VDD454](#), [VDD455](#), [VDD456](#), [VDD457](#), [VDD458](#), [VDD459](#), [VDD460](#), [VDD461](#), [VDD462](#), [VDD463](#), [VDD464](#), [VDD465](#), [VDD466](#), [VDD467](#), [VDD468](#), [VDD469](#), [VDD470](#), [VDD471](#), [VDD472](#), [VDD473](#), [VDD474](#), [VDD475](#), [VDD476](#), [VDD477](#), [VDD478](#), [VDD479](#), [VDD480](#), [VDD481](#), [VDD482](#), [VDD483](#), [VDD484](#), [VDD485](#), [VDD486](#), [VDD487](#), [VDD488](#), [VDD489](#), [VDD490](#), [VDD491](#), [VDD492](#), [VDD493](#), [VDD494](#), [VDD495](#), [VDD496](#), [VDD497](#), [VDD498](#), [VDD499](#), [VDD500](#), [VDD501](#), [VDD502](#), [VDD503](#), [VDD504](#), [VDD505](#), [VDD506](#), [VDD507](#), [VDD508](#), [VDD509](#), [VDD510](#), [VDD511](#), [VDD512](#), [VDD513](#), [VDD514](#), [VDD515](#), [VDD516](#), [VDD517](#), [VDD518](#), [VDD519](#), [VDD520](#), [VDD521](#), [VDD522](#), [VDD523](#), [VDD524](#), [VDD525](#), [VDD526](#), [VDD527](#), [VDD528](#), [VDD529](#), [VDD530](#), [VDD531](#), [VDD532](#), [VDD533](#), [VDD534](#), [VDD535](#), [VDD536](#), [VDD537](#), [VDD538](#), [VDD539](#), [VDD540](#), [VDD541](#), [VDD542](#), [VDD543](#), [VDD544](#), [VDD545](#), [VDD546](#), [VDD547](#), [VDD548](#), [VDD549](#), [VDD550](#), [VDD551](#), [VDD552](#), [VDD553](#), [VDD554](#), [VDD555](#), [VDD556](#), [VDD557](#), [VDD558](#), [VDD559](#), [VDD560](#), [VDD561](#), [VDD562](#), [VDD563](#), [VDD564](#), [VDD565](#), [VDD566](#), [VDD567](#), [VDD568](#), [VDD569](#), [VDD570](#), [VDD571](#), [VDD572](#), [VDD573](#), [VDD574](#), [VDD575](#), [VDD576](#), [VDD577](#), [VDD578](#), [VDD579](#), [VDD580](#), [VDD581](#), [VDD582](#), [VDD583](#), [VDD584](#), [VDD585](#), [VDD586](#), [VDD587](#), [VDD588](#), [VDD589](#), [VDD590](#), [VDD591](#), [VDD592](#), [VDD593](#), [VDD594](#), [VDD595](#), [VDD596](#), [VDD597](#), [VDD598](#), [VDD599](#), [VDD600](#), [VDD601](#), [VDD602](#), [VDD603](#), [VDD604](#), [VDD605](#), [VDD606](#), [VDD607](#), [VDD608](#), [VDD609](#), [VDD610](#), [VDD611](#), [VDD612](#), [VDD613](#), [VDD614](#), [VDD615](#), [VDD616](#), [VDD617](#), [VDD618](#), [VDD619](#), [VDD620](#), [VDD621](#), [VDD622](#), [VDD623](#), [VDD624](#), [VDD625](#), [VDD626](#), [VDD627](#), [VDD628](#), [VDD629](#), [VDD630](#), [VDD631](#), [VDD632](#), [VDD633](#), [VDD634](#), [VDD635](#), [VDD636](#), [VDD637](#), [VDD638](#), [VDD639](#), [VDD640](#), [VDD641](#), [VDD642](#), [VDD643](#), [VDD644](#), [VDD645](#), [VDD646](#), [VDD647](#), [VDD648](#), [VDD649](#), [VDD650](#), [VDD651](#), [VDD652](#), [VDD653](#), [VDD654](#), [VDD655](#), [VDD656](#), [VDD657](#), [VDD658](#), [VDD659](#), [VDD660](#), [VDD661](#), [VDD662](#), [VDD663](#), [VDD664](#), [VDD665](#), [VDD666](#), [VDD667](#), [VDD668](#), [VDD669](#), [VDD670](#), [VDD671](#), [VDD672](#), [VDD673](#), [VDD674](#), [VDD675](#), [VDD676](#), [VDD677](#), [VDD678](#), [VDD679](#), [VDD680](#), [VDD681](#), [VDD682](#), [VDD683](#), [VDD684](#), [VDD685](#), [VDD686](#), [VDD687](#), [VDD688](#), [VDD689](#), [VDD690](#), [VDD691](#), [VDD692](#), [VDD693](#), [VDD694](#), [VDD695](#), [VDD696](#), [VDD697](#), [VDD698](#), [VDD699](#), [VDD700](#), [VDD701](#), [VDD702](#), [VDD703](#), [VDD704](#), [VDD705](#), [VDD706](#), [VDD707](#), [VDD708](#), [VDD709](#), [VDD710](#), [VDD711](#), [VDD712](#), [VDD713](#), [VDD714](#), [VDD715](#), [VDD716](#), [VDD717](#), [VDD718](#), [VDD719](#), [VDD720](#), [VDD721](#), [VDD722](#), [VDD723](#), [VDD724](#), [VDD725](#), [VDD726](#), [VDD727](#), [VDD728](#), [VDD729](#), [VDD730](#), [VDD731](#), [VDD732](#), [VDD733](#), [VDD734](#), [VDD735](#), [VDD736](#), [VDD737](#), [VDD738](#), [VDD739](#), [VDD740](#), [VDD741](#), [VDD742](#), [VDD743](#), [VDD744](#), [VDD745](#), [VDD746](#), [VDD747](#), [VDD748](#), [VDD749](#), [VDD750](#), [VDD751](#), [VDD752](#), [VDD753](#), [VDD754](#), [VDD755](#), [VDD756](#), [VDD757](#), [VDD758](#), [VDD759](#), [VDD760](#), [VDD761](#), [VDD762](#), [VDD763](#), [VDD764](#), [VDD765](#), [VDD766](#), [VDD767](#), [VDD768](#), [VDD769](#), [VDD770](#), [VDD771](#), [VDD772](#), [VDD773](#), [VDD774](#), [VDD775](#), [VDD776](#), [VDD777](#), [VDD778](#), [VDD779](#), [VDD780](#), [VDD781](#), [VDD782](#), [VDD783](#), [VDD784](#), [VDD785](#), [VDD786](#), [VDD787](#), [VDD788](#), [VDD789](#), [VDD790](#), [VDD791](#), [VDD792](#), [VDD793](#), [VDD794](#), [VDD795](#), [VDD796](#), [VDD797](#), [VDD798](#), [VDD799](#), [VDD800](#), [VDD801](#), [VDD802](#), [VDD803](#), [VDD804](#), [VDD805](#), [VDD806](#), [VDD807](#), [VDD808](#), [VDD809](#), [VDD810](#), [VDD811](#), [VDD812](#), [VDD813](#), [VDD814](#), [VDD815](#), [VDD816](#), [VDD817](#), [VDD818](#), [VDD819](#), [VDD820](#), [VDD821](#), [VDD822](#), [VDD823](#), [VDD824](#), [VDD825](#), [VDD826](#), [VDD827](#), [VDD828](#), [VDD829](#), [VDD830](#), [VDD831](#), [VDD832](#), [VDD833](#), [VDD834](#), [VDD835](#), [VDD836](#), [VDD837](#), [VDD838](#), [VDD839](#), [VDD840](#), [VDD841](#), [VDD842](#), [VDD843](#), [VDD844](#), [VDD845](#), [VDD846](#), [VDD847](#), [VDD848](#), [VDD849](#), [VDD850](#), [VDD851](#), [VDD852](#), [VDD853](#), [VDD854](#), [VDD855](#), [VDD856](#), [VDD857](#), [VDD858](#), [VDD859](#), [VDD860](#), [VDD861](#), [VDD862](#), [VDD863](#), [VDD864](#), [VDD865](#), [VDD866](#), [VDD867](#), [VDD868](#), [VDD869](#), [VDD870](#), [VDD871](#), [VDD872](#), [VDD873](#), [VDD874](#), [VDD875](#), [VDD876](#), [VDD877](#), [VDD878](#), [VDD879](#), [VDD880](#), [VDD881](#), [VDD882](#), [VDD883](#), [VDD884](#), [VDD885](#), [VDD886](#), [VDD887](#), [VDD888](#), [VDD889](#), [VDD890](#), [VDD891](#), [VDD892](#), [VDD893](#), [VDD894](#), [VDD895](#), [VDD896](#), [VDD897](#), [VDD898](#), [VDD899](#), [VDD900](#), [VDD901](#), [VDD902](#), [VDD903](#), [VDD904](#), [VDD905](#), [VDD906](#), [VDD907](#), [VDD908](#), [VDD909](#), [VDD910](#), [VDD911](#), [VDD912](#), [VDD913](#), [VDD914](#), [VDD915](#), [VDD916](#), [VDD917](#), [VDD918](#), [VDD919](#), [VDD920](#), [VDD921](#), [VDD922](#), [VDD923](#), [VDD924](#), [VDD925](#), [VDD926](#), [VDD927](#), [VDD928](#), [VDD929](#), [VDD930](#), [VDD931](#), [VDD932](#), [VDD933](#), [VDD934](#), [VDD935](#), [VDD936](#), [VDD937](#), [VDD938](#), [VDD939](#), [VDD940](#), [VDD941](#), [VDD942](#), [VDD943](#), [VDD944](#), [VDD945](#), [VDD946](#), [VDD947](#), [VDD948](#), [VDD949](#), [VDD950](#), [VDD951](#), [VDD952](#), [VDD953](#), [VDD954](#), [VDD955](#), [VDD956](#), [VDD957](#), [VDD958](#), [VDD959](#), [VDD960](#), [VDD961](#), [VDD962](#), [VDD963](#), [VDD964](#), [VDD965](#), [VDD966](#), [VDD967](#), [VDD968](#), [VDD969](#), [VDD970](#), [VDD971](#), [VDD972](#), [VDD973](#), [VDD974](#), [VDD975](#), [VDD976](#), [VDD977](#), [VDD978](#), [VDD979](#), [VDD980](#), [VDD981](#), [VDD982](#), [VDD983](#), [VDD984](#), [VDD985](#), [VDD986](#), [VDD987](#), [VDD988](#), [VDD989](#), [VDD990](#), [VDD991](#), [VDD992](#), [VDD993](#), [VDD994](#), [VDD995](#), [VDD996](#), [VDD997](#), [VDD998](#), [VDD999](#), [VDD1000](#), [VDD1001](#), [VDD1002](#), [VDD1003](#), [VDD1004](#), [VDD1005](#), [VDD1006](#), [VDD1007](#), [VDD1008](#), [VDD1009](#), [VDD1010](#), [VDD1011](#), [VDD1012](#), [VDD1013](#), [VDD1014](#), [VDD1015](#), [VDD1016](#), [VDD1017](#), [VDD1018](#), [VDD1019](#), [VDD1020](#), [VDD1021](#), [VDD1022](#), [VDD1023](#), [VDD1024](#), [VDD1025](#), [VDD1026](#), [VDD1027](#), [VDD1028](#), [VDD1029](#), [VDD1030](#), [VDD1031](#), [VDD1032](#), [VDD1033](#), [VDD1034](#), [V](#)



Timing Diagram of the MS9708

TYPICAL CHARACTERISTICS CURVES

MS9708 Characteristics Curves

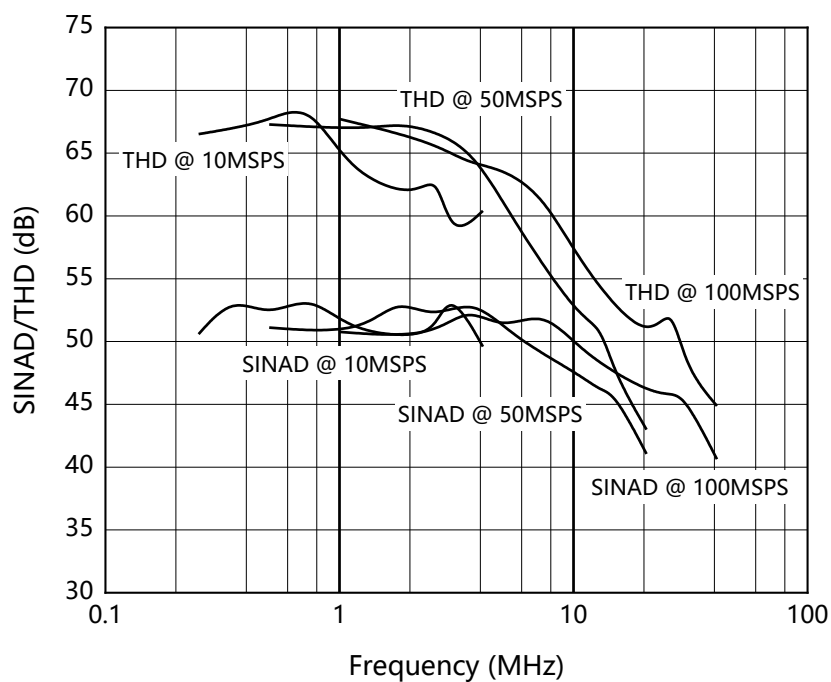


Figure 1 . SINAD/THD VS. f_{OUT} (AVDD=DVDD=5V)

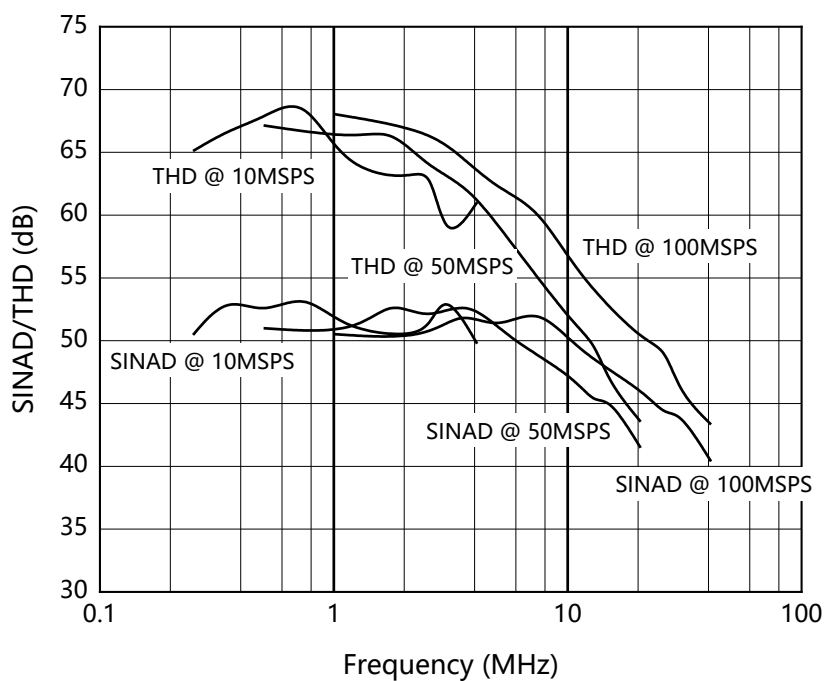


Figure 2. SINAD/THD VS. f_{OUT} (Differential Outputs, AVDD=DVDD=5V)

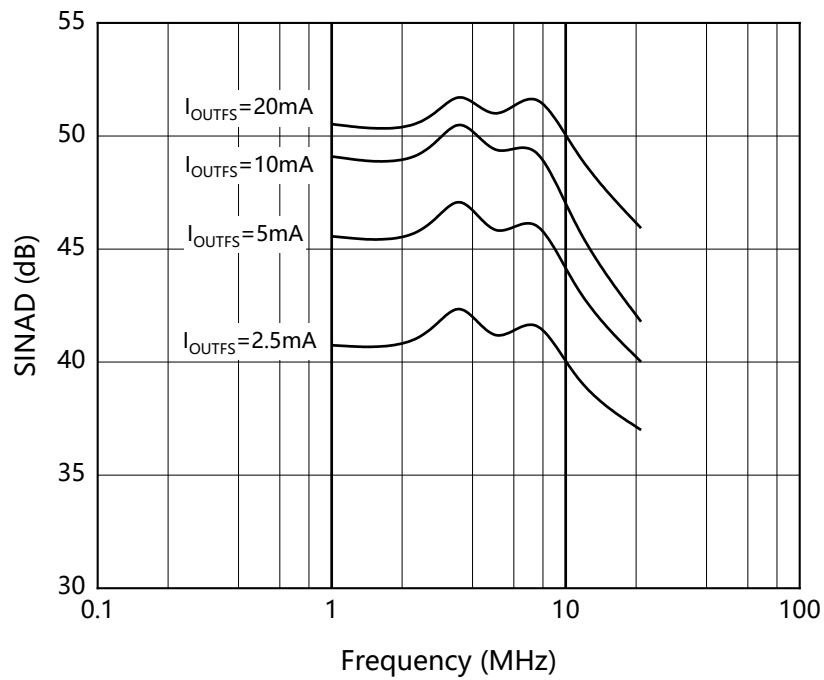


Figure 3. SINAD VS. I_{OUTFS} @ 100MSPS

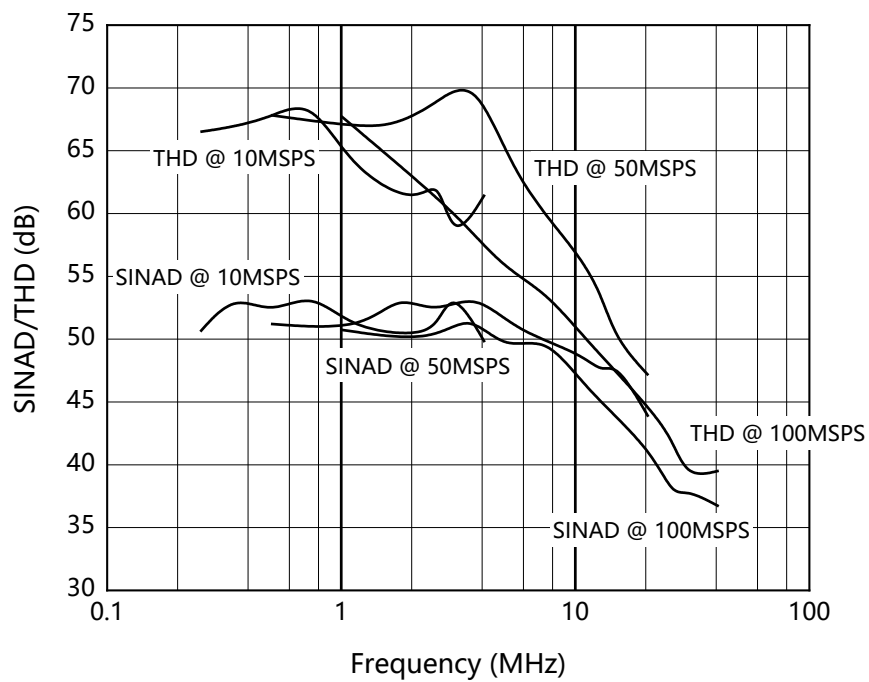


Figure 4. SINAD/THD VS. f_{OUT} (AVDD= DVDD=3V)

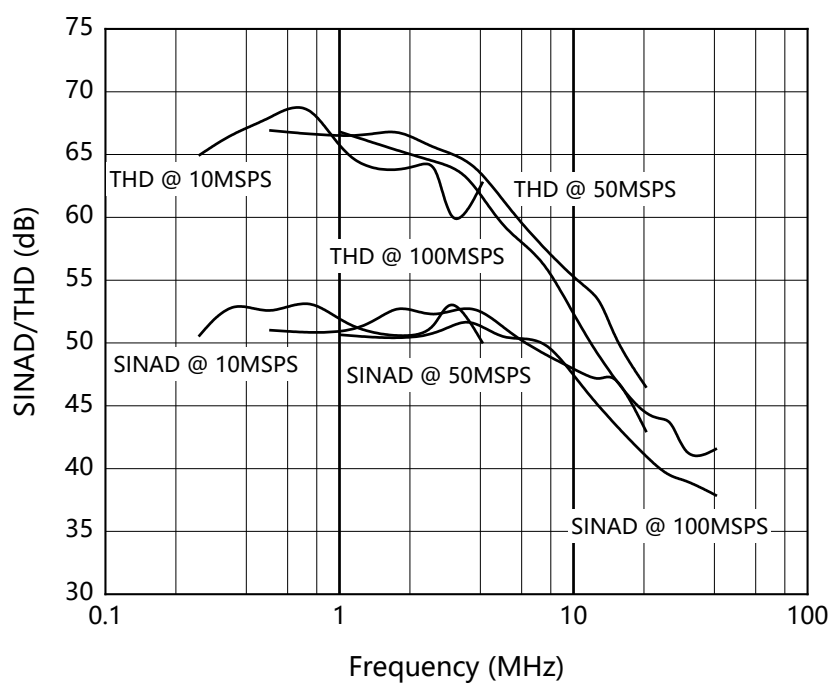


Figure 5. SINAD/THD VS. f_{OUT} (Differential Outputs, $AVDD=DVDD=3V$)

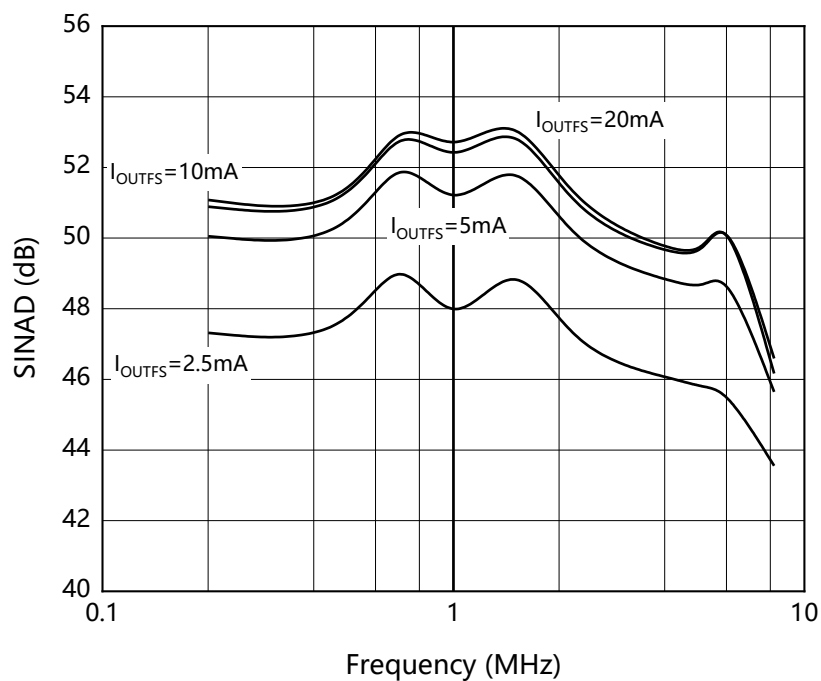


Figure 6. SINAD VS. I_{OUTFS} @ 20MSPS

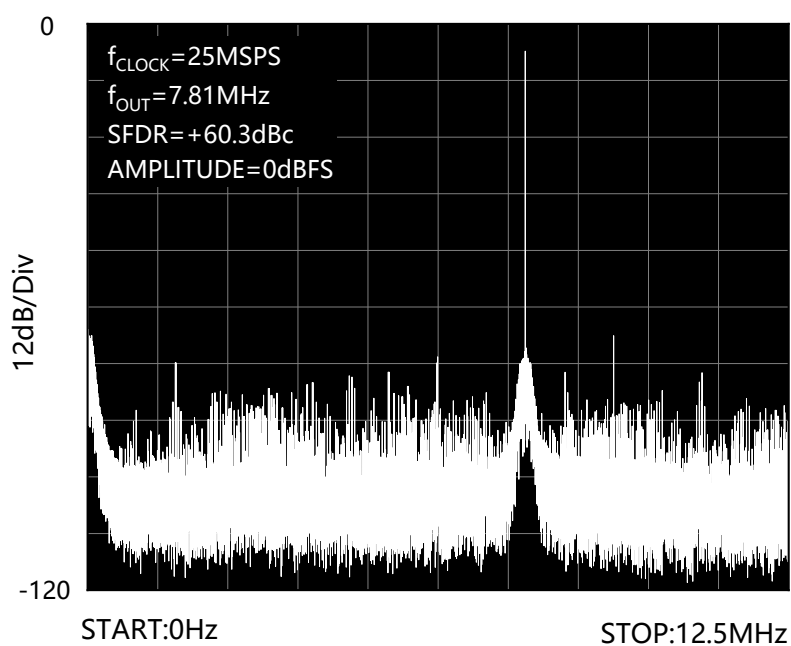


Figure 7. Single-Tone Spectral Plot @ 25MSPS

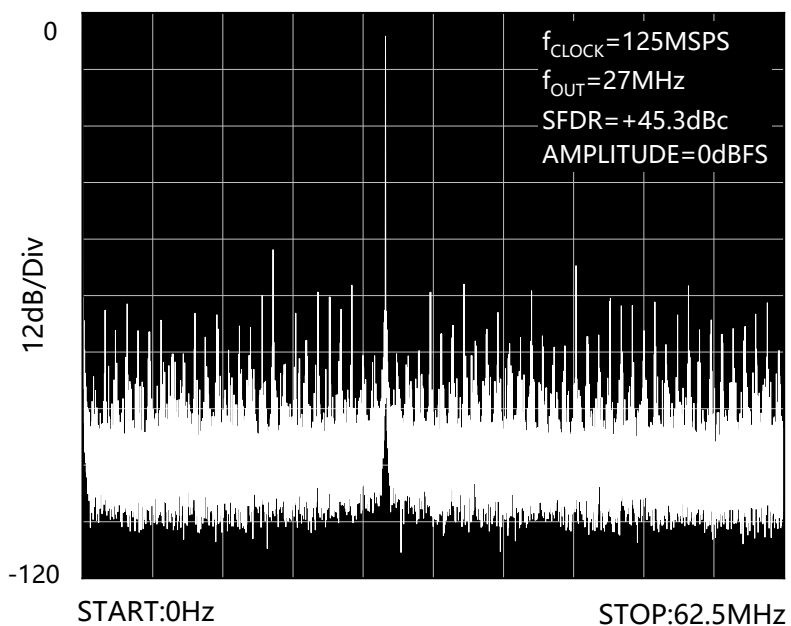


Figure 8. Single-Tone Spectral Plot @ 125MSPS

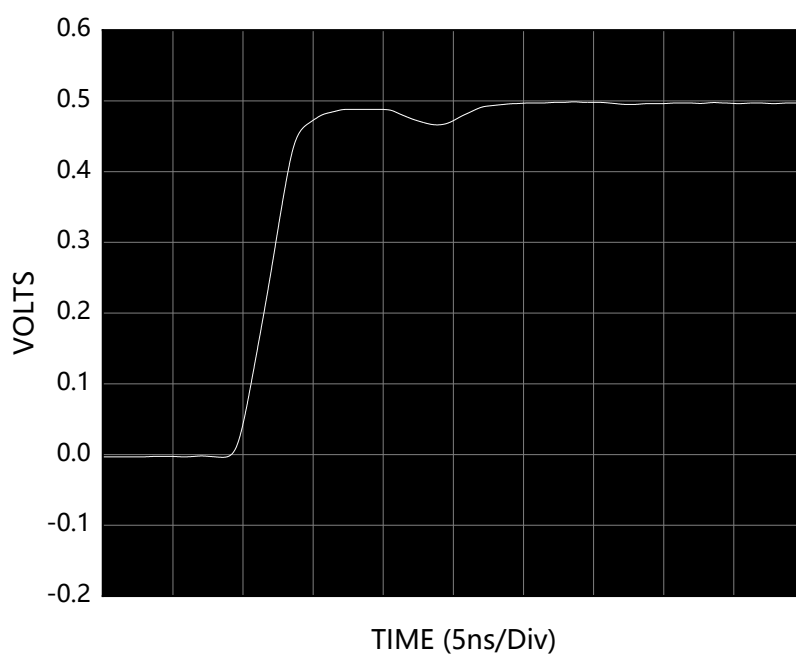


Figure 9. Step Response

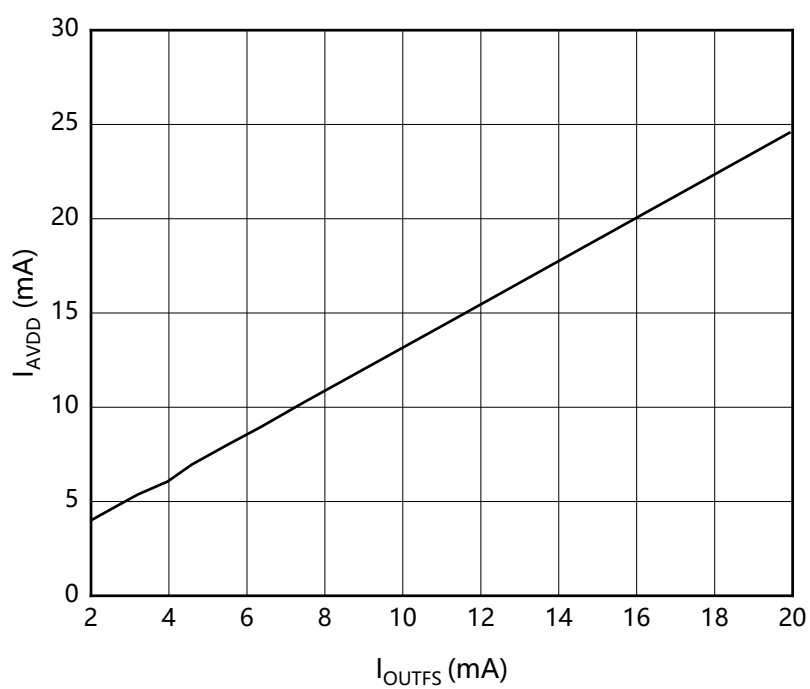


Figure 10. I_{AVD} VS. I_{OUTFS}

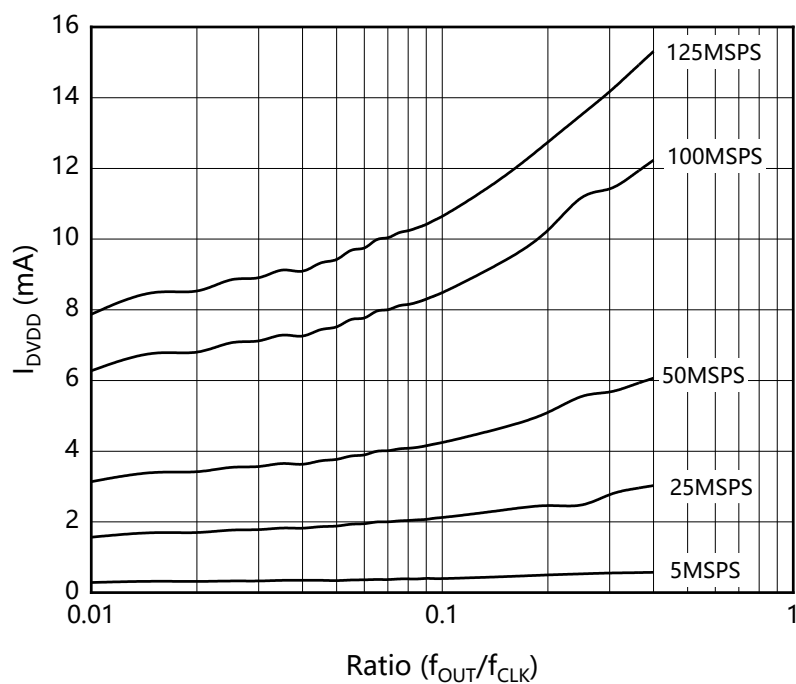


Figure 11. I_{DVDD} VS. Ratio @DVDD=5V

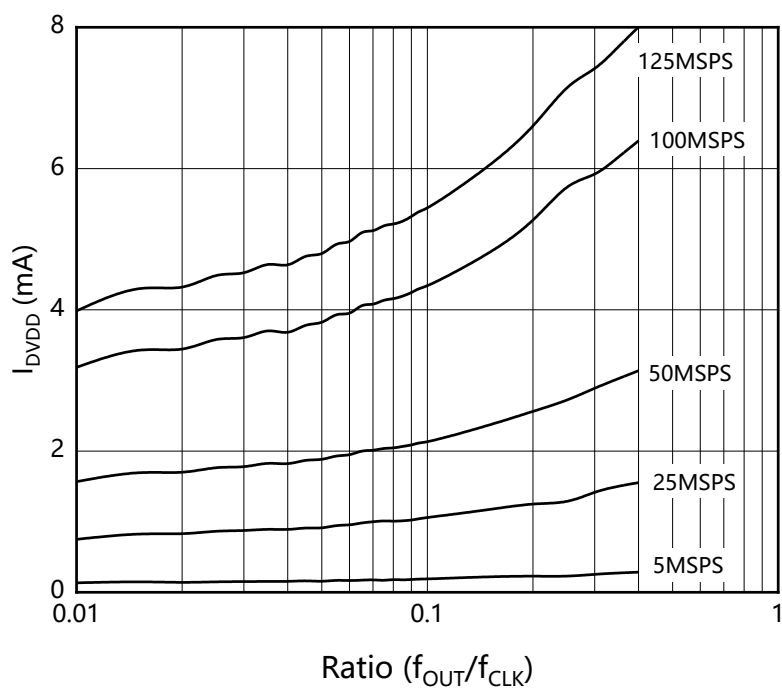


Figure 12. I_{DVDD} VS. Ratio @DVDD=3V

MS9714 Characteristics Curves

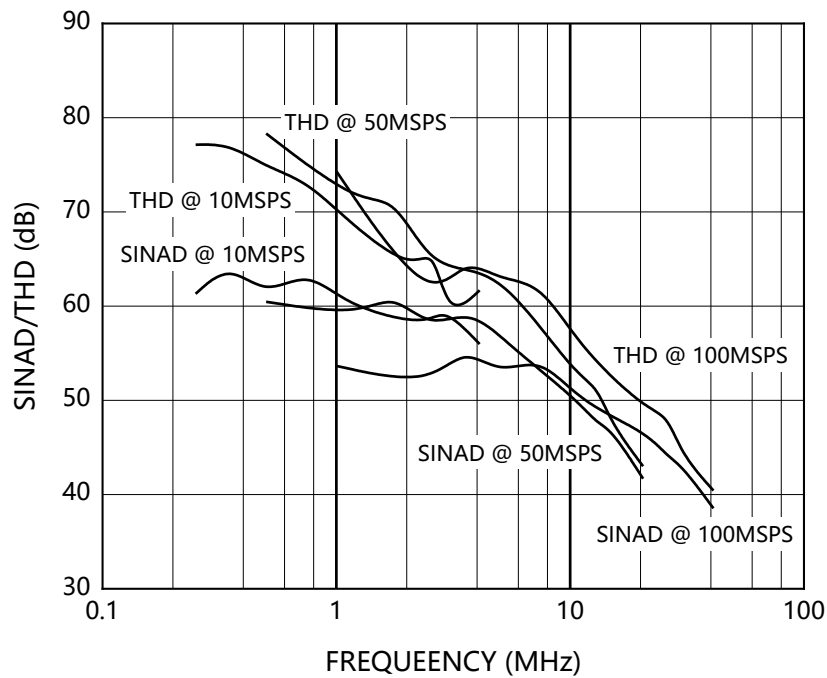


Figure 13 . SINAD/THD VS. f_{OUT} (AVDD=DVDD=5V)

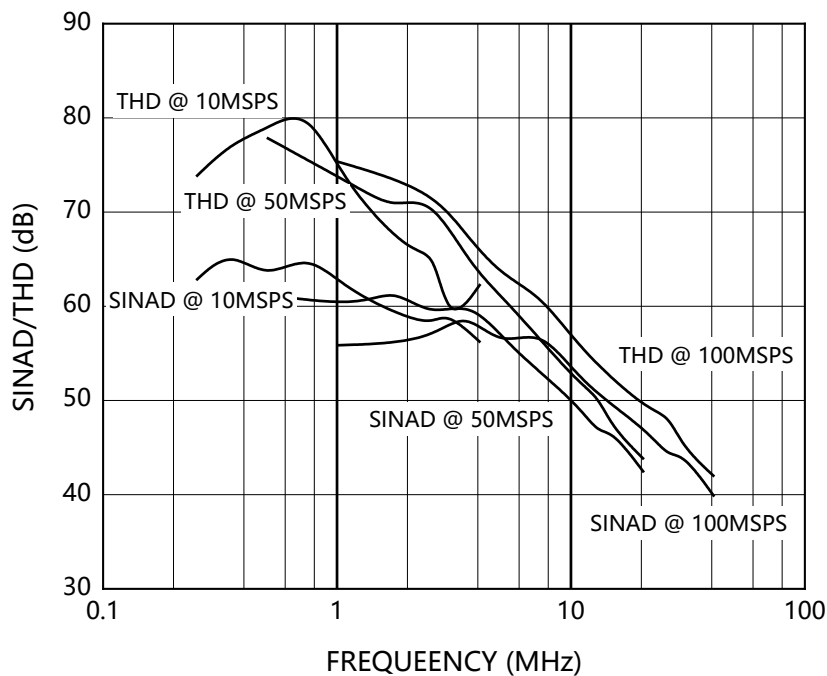


Figure 14. SINAD/THD VS. f_{OUT} (Differential Outputs, AVDD=DVDD=5V)

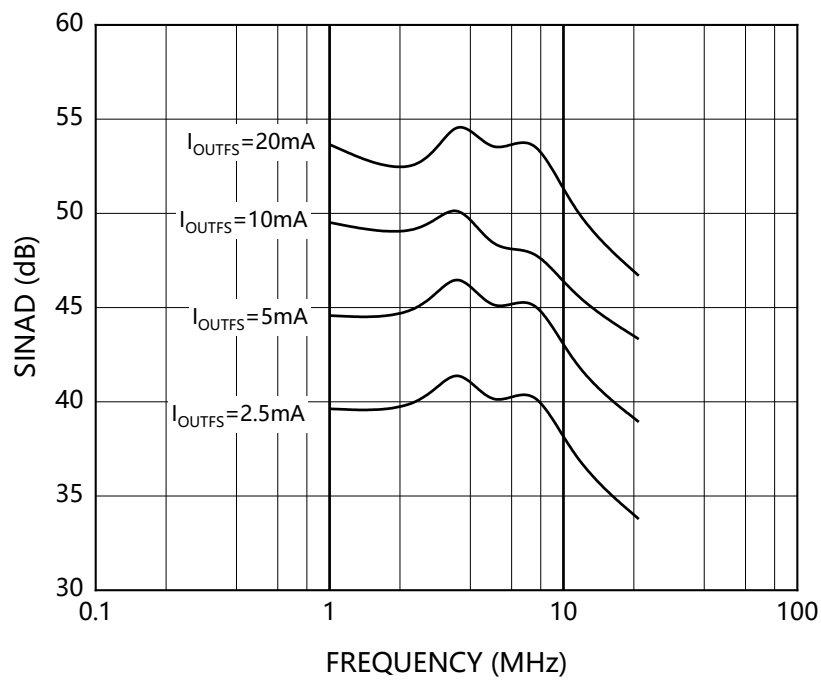


Figure 15. SINAD VS. I_{OUTFS} @ 100MSPS

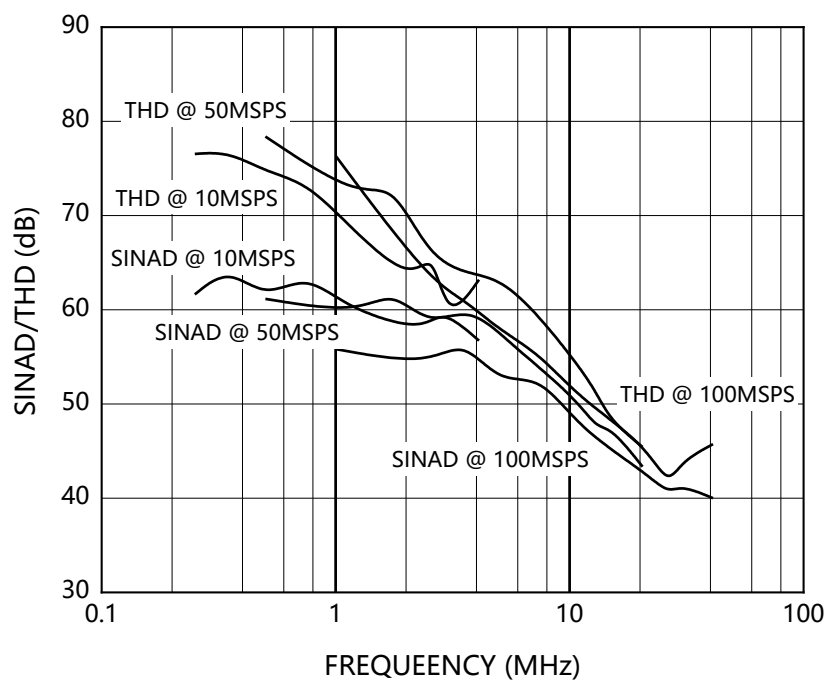


Figure 16. SINAD/THD VS. f_{OUT} ($AVDD = DVDD = 3V$)

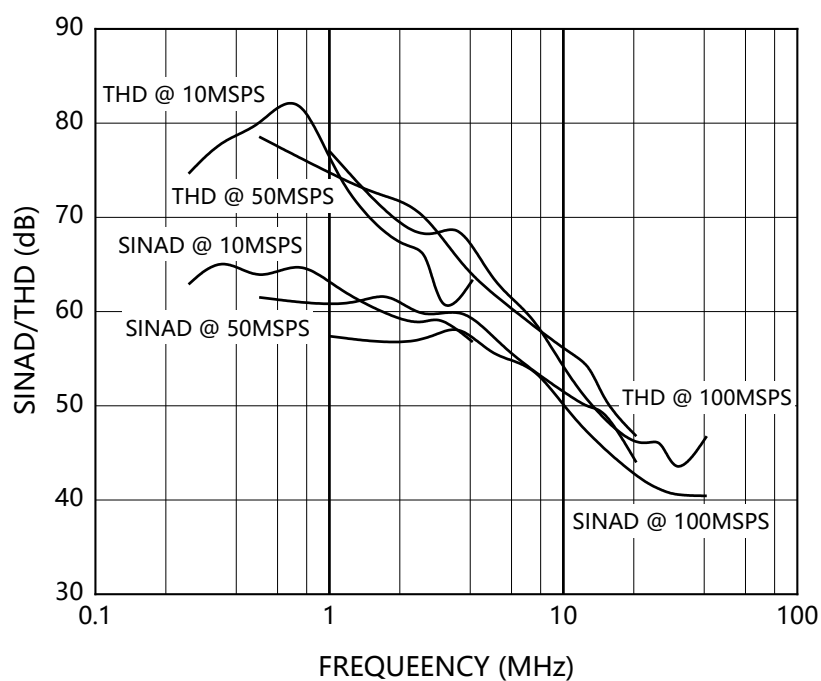


Figure 17. SINAD/THD VS. f_{OUT} (Differential Outputs, $AVDD=DVDD=3V$)

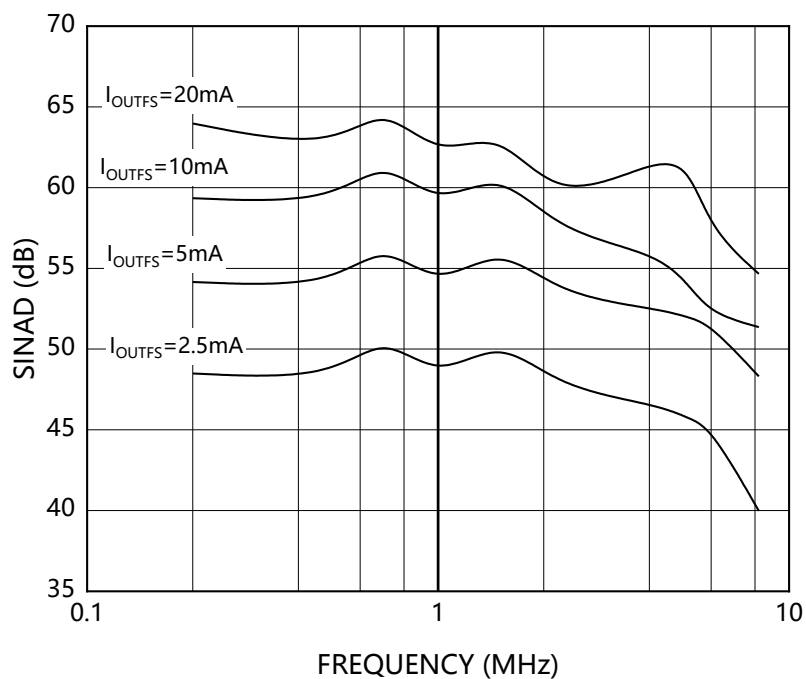


Figure 18. SINAD VS. I_{OUTFS} @ 20MSPS

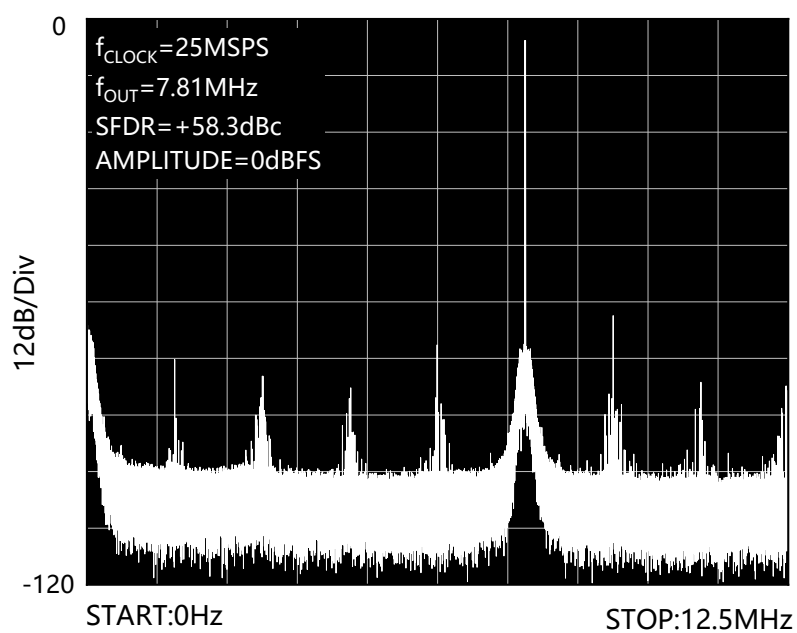


Figure 19. Single-Tone Spectral Plot @ 25MSPS

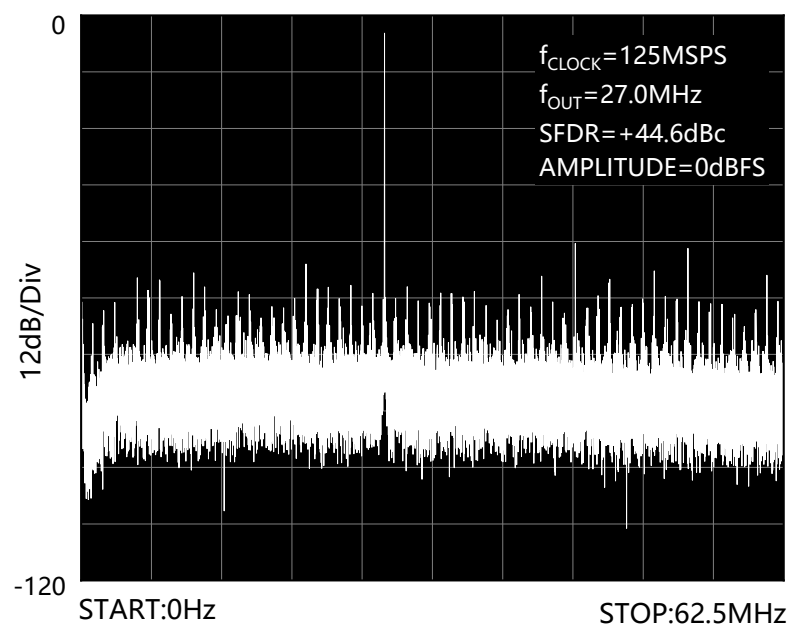


Figure 20. Single-Tone Spectral Plot @ 125MSPS

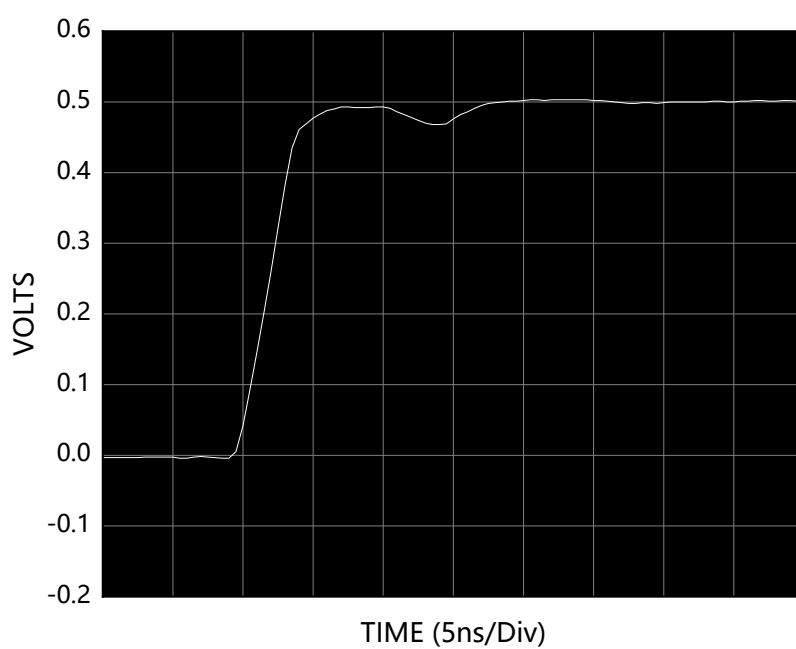


Figure 21. Step Response

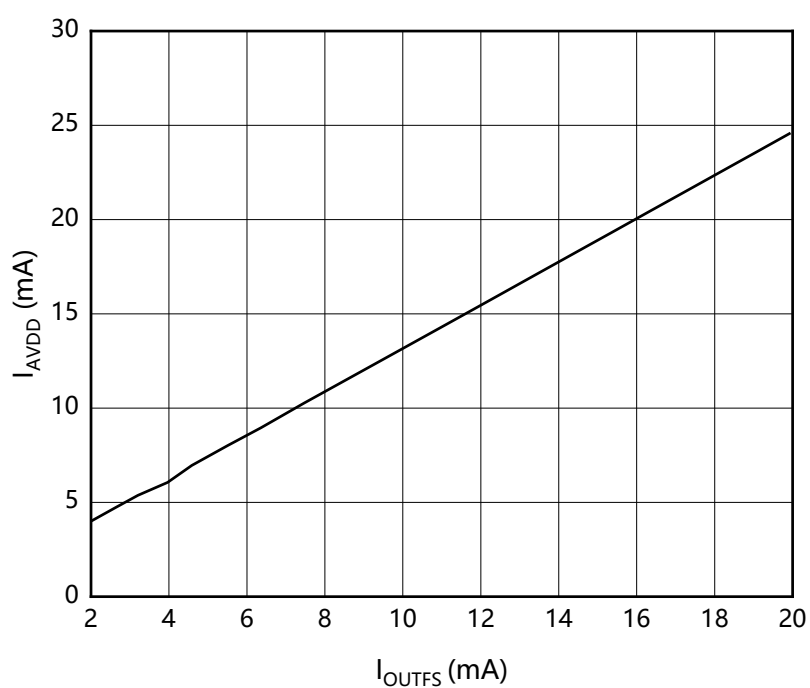


Figure 22. I_{AVDD} VS. I_{OUTFS}

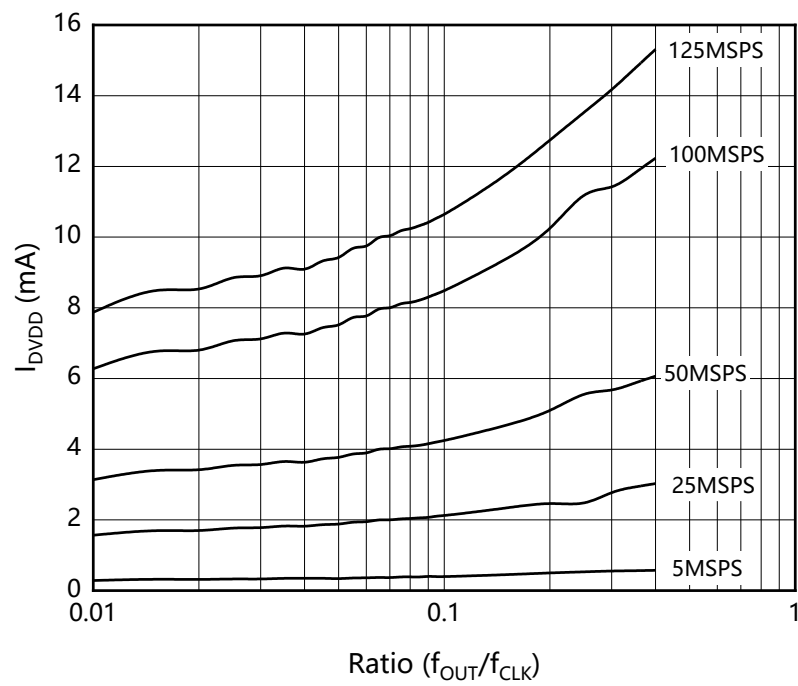


Figure 23. I_{DVDD} VS. Ratio @DVDD=5V

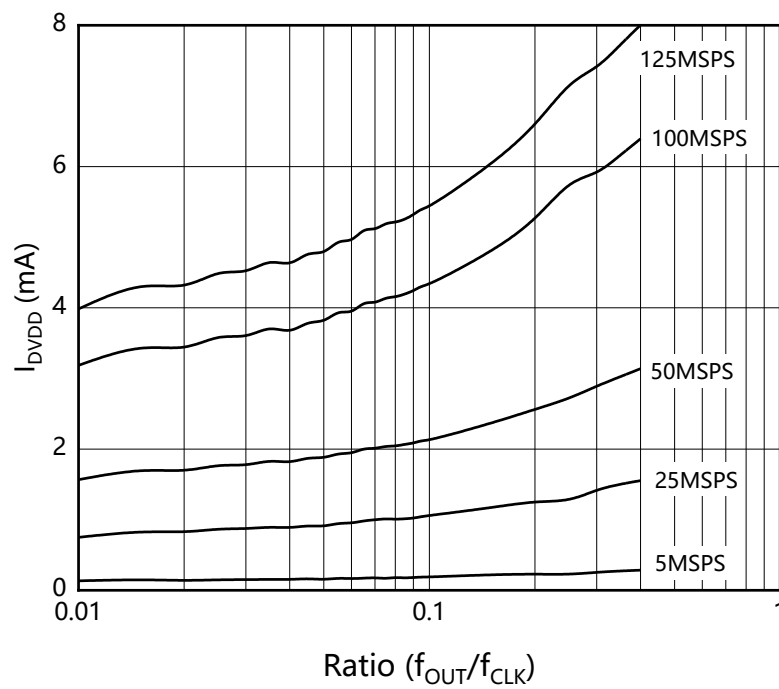


Figure 24. I_{DVDD} VS. Ratio @DVDD=3V

FUNCTION DESCRIPTION

The MS9708/MS9714 includes a PMOS current source array, which can generate up to 20mA current. The analog and digital circuits have differential power supplies (AVDD and DVDD) that AVDD can operate from 2.7V to 5.5V and DVDD can operate from 1.8V to 5.5V . The digital section operates in 125 MSPS clock rate and includes edge-triggered latches and decode unit. The analog section includes the PMOS current source array, the associated differential switches, a 1.2V bandgap voltage reference and a reference control amplifier.

The full-scale current, I_{OUTFS} can be adjusted from 2mA to 20mA by an external resistor, R_{set} . The external resistor is connected with reference control amplifier and voltage reference V_{REFIO} , and generates the reference current I_{REF} . The full-scale current, I_{OUTFS} is thirty-two times the value of I_{REF} .

DAC Transmission Characteristic

The MS9708/MS9714 has two complementary outputs, I_{OUTA} and I_{OUTB} . For example, the calculation formula for the MS9708 is as follows:

$$I_{OUTA} = (DAC\ CODE/256) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (255 - DAC\ CODE)/256 \times I_{OUTFS} \quad (2)$$

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

Two current outputs can be directly connected to resistive load. The resistors connected on I_{OUTA} and I_{OUTB} must be matched. The other end of resistor is connected to ground. The resistance is 50Ω or 75Ω.

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

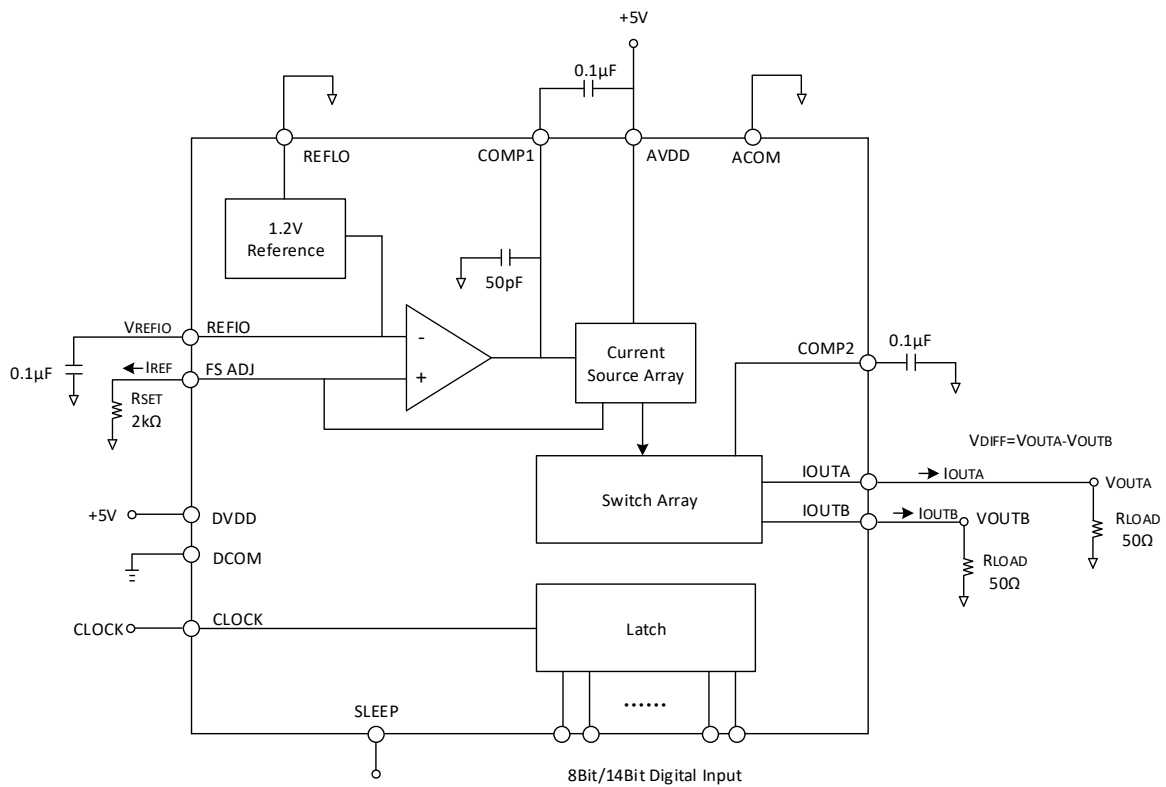
$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

The voltage values of V_{OUTA} 和 V_{OUTB} cannot exceed the allowable maximum, otherwise nonlinearity error would be produced.

The differential value between V_{OUTA} and V_{OUTB} :

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

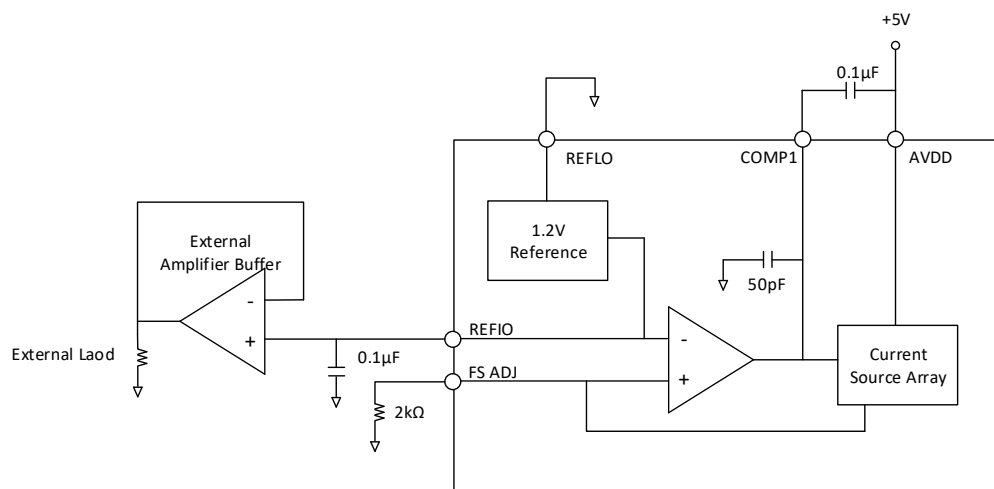
$$V_{DIFF} = \{(2\ DAC\ CODE - 255)/256\} \times (32\ R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$



Function Block Diagram

Voltage Reference and Control Amplifier

The MS9708/MS9714 includes an internal 1.2V bandgap reference source that can connect with external reference. When REFLO is connected to ground, internal reference is activated and REFIO acts as output pin. When REFLO is connected to power supply, external reference is activated, REFIO acts as input pin and connected to external reference source. When internal reference is used, 0.1μF capacitor needs to be connected on REFIO. REFIO cannot drive any external load. It should be buffered with an external amplifier whose input current should not exceed 100nA if external load is needed.



Internal Reference

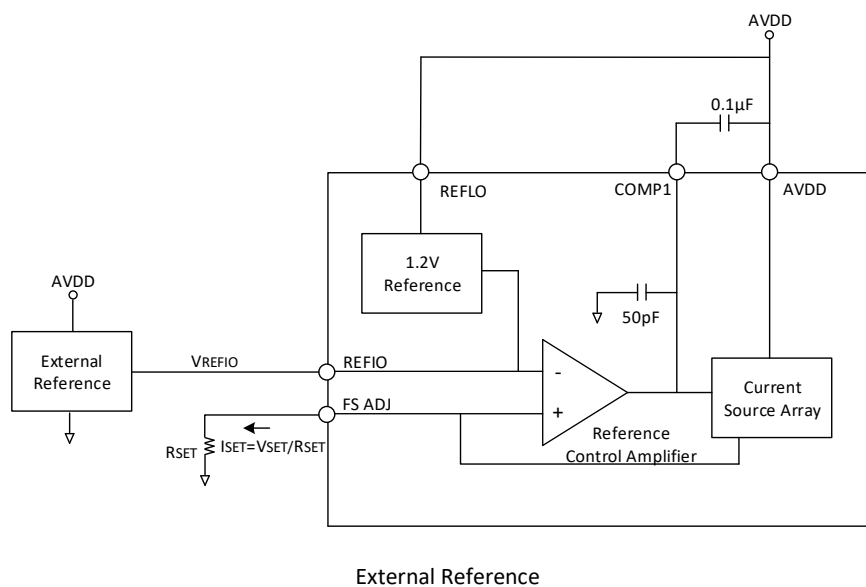
The internal reference can be inactivated by connecting REFLO to AVDD. External reference can be applied to REFIO. The external reference can improve precision. 0.1 μ F capacitor can not be connected when external reference is applied. The input impedance of REFIO is 1M Ω and can minimize the load of external reference.

The MS9708/MS9714 includes an internal bias current control amplifier, which can control the DAC's full-scale current, I_{OUTFS} . The amplifier is set as a V-I converter as follows. The current output, I_{REF} is determined by the ratio of V_{REFIO} and an external resistor, R_{SET} .

I_{OUTFS} ranges from 2mA to 20mA and the corresponding I_{REF} range is between 62.5 μ A and 625 μ A. The first benefit is to control power dissipation. Another benefit is to control system gain.

The small-signal input bandwidth is about 0.4MHz for reference control amplifier. It relates to the capacitor connected on COMP1. The capacitor can filter the noise caused by reference amplifier and the recommendation value is 0.1 μ F.

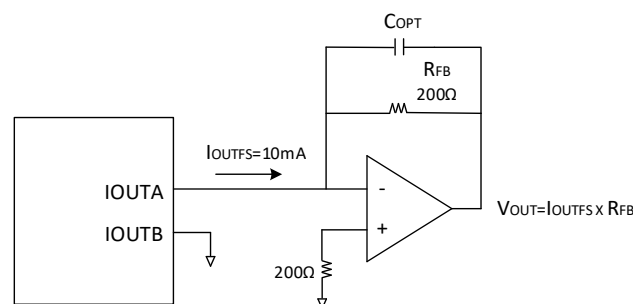
I_{REF} can be changed by changing the value of external reference, whose range is from 0.1V to 1.25V.



Analog Output and Output Setting

The MS9708/MS9714 has two complementary current outputs, I_{OUTA} and I_{OUTB} . V_{OUTA} and V_{OUTB} are get by external resistor. Can only use one terminal. The unused terminal can connect with ground or connect with matched resistor.

The output voltage can be converted to negative value by externally connecting operational amplifier, as follows.



Digital Input

The digital selection of the MS9708/MS9714 includes 8/14bit data input and 1bit clock input. For the MS9708, DB7 is the MSB and DB0 is the LSB. The digital interface is implemented using an edge-triggered latch. The DAC output is latched on the rising edge of the clock. The clock maximum frequency is 125MHz. The input level of digital selection is from 1.8V to 5.5V. When DVDD level is same as the highest level of digital selection, digital input can be matched with TTL level. 3V to 3.3V DVDD can match with most TTL circuits.

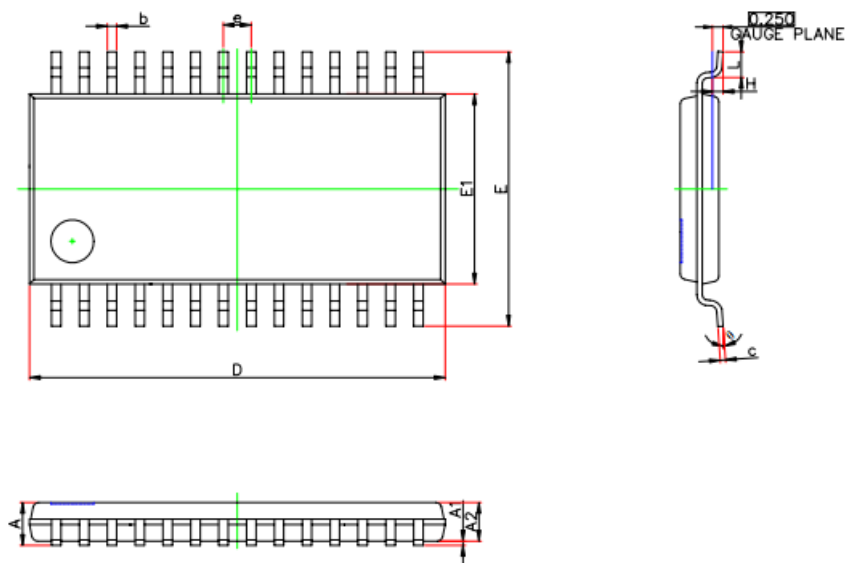
Because the operating frequency is higher, the maximum sample rate is 125MSPS. Must ensure the quality of input digital signal. Settling time and hold time of trigger must be met. Input level also needs to meet requirement.

Sleep Mode

The sleep mode of the MS9708/MS9714 can greatly reduce power dissipation. When SLEEP pin is applied to high-level, chip enters into sleep mode and current can drop to less than 8.5mA. SLEEP pin is built in pull-down circuit, which can ensure the normal operation when input is floating. The on and off characteristics of power supply depend on the capacitor on COMP2. The typical value is 0.1μF. The off time is 5μs and restart time is 3.25ms.

PACKAGE OUTLINE DIMENSIONS

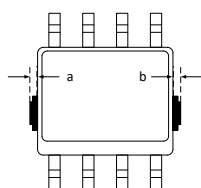
TSSOP28



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	6.250	6.550	0.246	0.258
E1	4.300	4.500	0.169	0.177
e	0.650(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.250(TYP)		0.010(TYP)	
θ	1°	7°	1°	7°

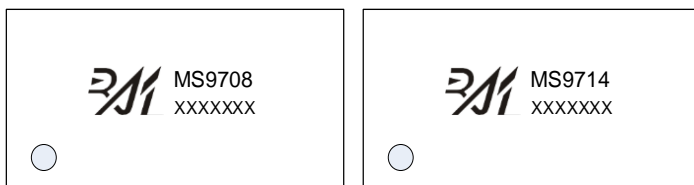
Note: In addition to the package size, a and b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.



MARKING and PACKAGE SPECIFICATION

1. Marking Drawing Description



Product Name : MS9708, MS9714

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS9708	TSSOP28	2000	1	2000	8	16000
MS9714	TSSOP28	3000	1	3000	8	24000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.
Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



+86-571-89966911



Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang



[http:// www.relmon.com](http://www.relmon.com)