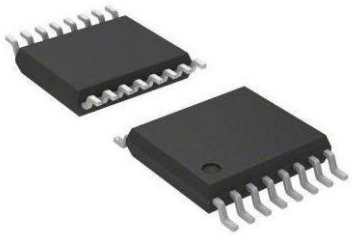
Four Channel LVDS Differential Cable Receiver

PRODUCT DESCRIPTION

The MS21148T is a four channel LVDS differential cable receiver. Each differential receiver could transform 100mV differential input voltage to effective logical output among the common-mode voltage range.

The MS21148T is applied for point-to-point base-band data transmission through 100Ω controlled impedance media. The transmission media could be PCB traces, backplane or cables. The data rate and distance depend on the media attenuation characteristic, the noise environment and other system characteristics. The operating temperature range is from -40°C to 125°C.



TSSOP16

FEATURES

- 200 Mbps(100MHz) Data Rate
- Propagation Delay Time 4.8ns (Typ.)
- Output high Impedance for LVDS Input on Power down mode
- 3.3V Power Supply
- Support 100mV~900mV Differential Signal Amplitude when input common range voltage located at 1.1V~1.3V
- Support Open, Short-circuit and Terminate Failure Safe
- TSSOP16 Package

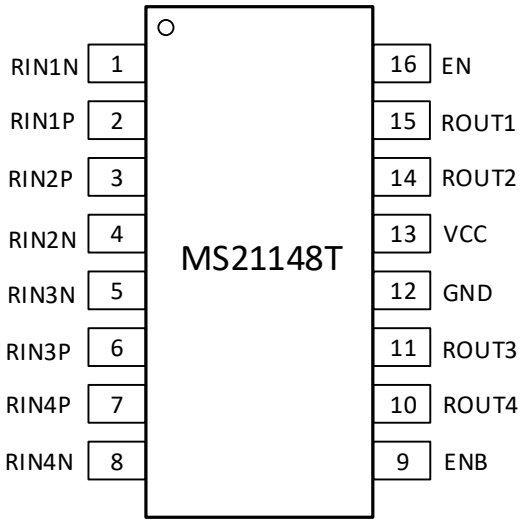
APPLICATIONS

- Multi-function Printer
- Flat Panel Display Interface
- Monitoring Camera

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS21148T	TSSOP16	MS21148T

PIN CONFIGURATION

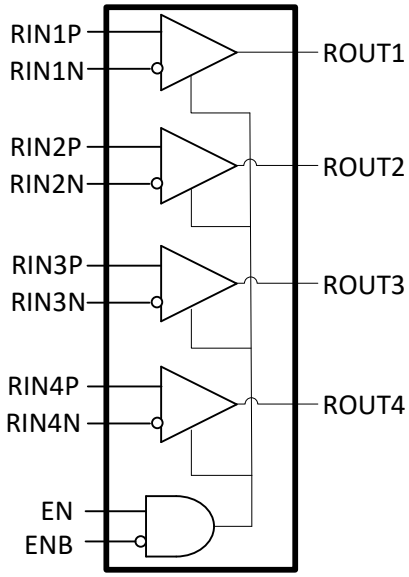


PIN DESCRIPTION

Pin	Name	Type	Description
1	RIN1N	I	Negative Input (Channel 1), LVDS Level
2	RIN1P	I	Positive Input (Channel 1), LVDS Level
3	RIN2P	I	Positive Input (Channel 2), LVDS Level
4	RIN2N	I	Negative Input (Channel 2), LVDS Level
5	RIN3N	I	Negative Input (Channel 3), LVDS Level
6	RIN3P	I	Positive Input (Channel 3), LVDS Level
7	RIN4P	I	Positive Input (Channel 4), LVDS Level
8	RIN4N	I	Negative Input (Channel 4), LVDS Level
9	ENB	I	Enable Input
10	ROUT4	O	Data Output (Channel 4), CMOS Logical Level
11	ROUT3	O	Data Output (Channel 3), CMOS Logical Level
12	GND	-	Ground
13	VCC	-	Power Supply
14	ROUT2	O	Data Output (Channel 2), CMOS Logical Level
15	ROUT1	O	Data Output (Channel 1), CMOS Logical Level
16	EN	I	Enable Input

Note: Not used LVDS input pins must be left floating.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	-0.5 ~ 4	V
All Inputs and Outputs Voltage	V_{CCIO}	-0.5 ~ (V_{CC}+0.3)	V
Operating Temperature Range	T_A	-40 ~ 125	°C
Storage Temperature Range	T_{STG}	-65 ~ 150	°C
Soldering Temperature (10s)	T_{SOLDER}	260	°C
ESD (HBM)	V_{HBM}	>±8000	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	3	3.3	3.6	V
Input Voltage Range of Receiver	V_{IN}	GND		V_{CC}	V
Common-mode Input Voltage Range	V_{ICMR}	V_{ID}/2		2.4-V_{ID}/2	V
Signal Rate	1/t_{UI}			200	Mbps

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{CC} = 3.0V to 3.6V, T_A= 25°C.

Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Forward Conversion Differential Input Voltage Threshold	V_{IT+}	Common-mode Input V_{CM}=0.05V,1.2V,2.35V			100	mV
Reverse Conversion Differential Input Voltage Threshold	V_{IT-}	Common-mode Input V_{CM}=0.05V,1.2V,2.35V	-100			mV
Input Common-mode Voltage [1]	V_{ICMR}		V_{ID}/2		2.4-V_{ID}/2	V
High-level Output Voltage	V_{OH}	I_{OH}=-0.4mA, V_{ID}=200mV	3.1	3.3		V
		I_{OH}=-0.4mA, Input Shorted	3.1	3.3		V
		I_{OH}=-0.4mA, Differential Input Bridged with 100Ω Resistor	3.1	3.3		V
Low-level Output Voltage	V_{OL}	I_{OL}=2mA,V_{ID}=-200mV		0.05	0.2	V
Input Current of RIN [2]	I_{IRIN}	V_{IN}=2.8V,V_{CC}=3.6V	-10	±1	+10	μA
		V_{IN}=0V,V_{CC}=3.6V	-15	±5	+15	μA
Input Current of EN and ENB [2]	I_{IEN}	V_{IN}=0V or V_{CC}=3.6V Other Inputs=V_{CC} or GND	-15	±5	+15	μA
Output Short-circuit Current	I_{OS}	Enable, V_{OUT}=0		-70	-60	mA
Output High-impedance Current	I_{OZ}	Disable, V_{OUT}=0 or 3.6V	-1	0	+1	μA
Input High Level	V_{IH}		2.4		V_{CC}	V
Input Low Level	V_{IL}		GND		0.8	V
Input Clamping Voltage	V_{CLAMP}	I_{CLAMP}=-18mA	-1.5	-0.78		V
With-load Power Supply Current	I_{CC}	EN=V_{CC}, Input Open		8.1	12	mA
Shutdown Current	I_{CCZ}	EN=0, Input Open		0.4	1.5	mA

Note:

1. The input common-mode voltage range relates to differential input voltage V_{ID}, and it decreases along with V_{ID} increasing.

2. +/- of input current represents the current flow direction.

Switching Characteristics

V_{CC} = 3.3V, T_A = 25°C, external load C_L=15pF [3,4].

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Differential Propagation Delay (High to Low)	t_{PHLD}	C_L=15pF V_{ID}=200mV Figure 1 and Figure 2		4.8		ns
Differential Propagation Delay (Low to High)	t_{PLHD}			4.8		ns
Differential Propagation Delay Skew $\|t_{PHLD}- t_{PLHD}\|$	t_{SDK}			200		ps
Channel Propagation Delay Skew [5]	t_{SK1}			50		ps
Rise Time	t_R			2.3		ns
Fall Time	t_F			2.3		ns
Output High Level to High Impedance Delay	t_{PHZ}	C_L=15pF R_L=2kΩ Figure 3 and Figure 4		16		ns
Output Low Level to High Impedance Delay	t_{PLZ}			12.1		ns
Output High Impedance to High Level Delay	t_{PZH}			5.6		ns
Output High Impedance to Low Level Delay	t_{PZL}			8.8		ns
Maximum Operating Frequency	f_{MAX}			100		MHz

Note:

3. Normal test for input signal: f=1MHz, Z_O=50Ω.

4. Load capacitance includes probe and soldering capacitance.

5. Channel Propagation Delay Skew is the maximum propagation delay difference between four channels.

Test Circuit

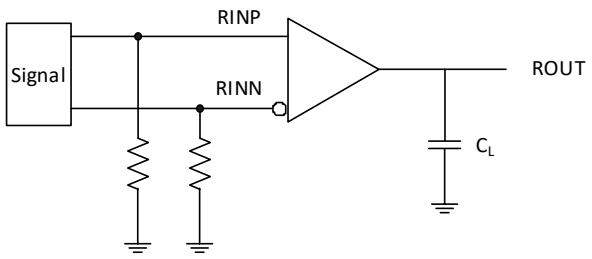


Figure 1. Propagation Delay and Transition Time Test Circuit

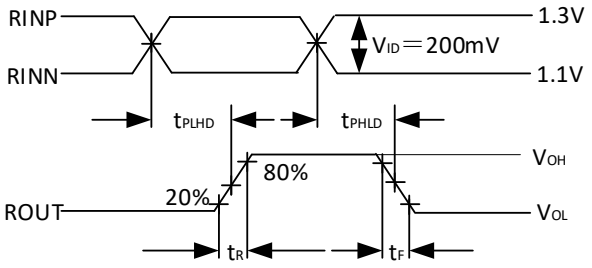


Figure 2. Propagation Delay and Transition Time Waveform

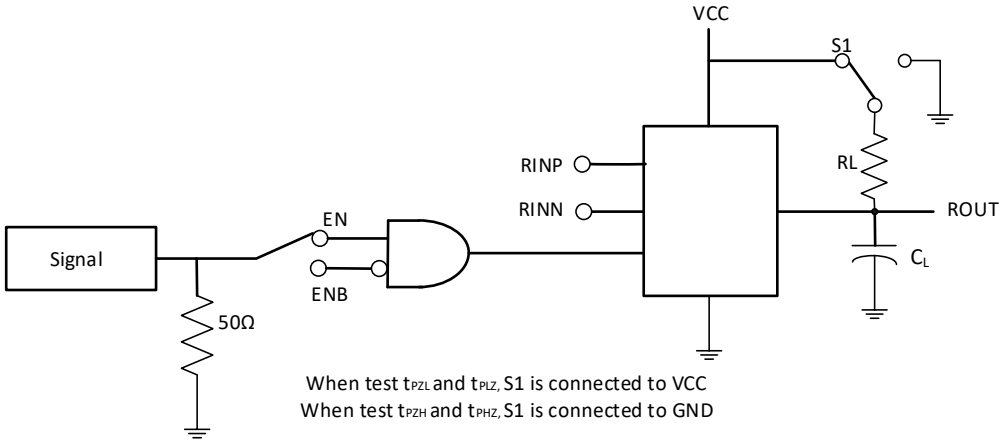


Figure 3. Three-state Delay Test Circuit

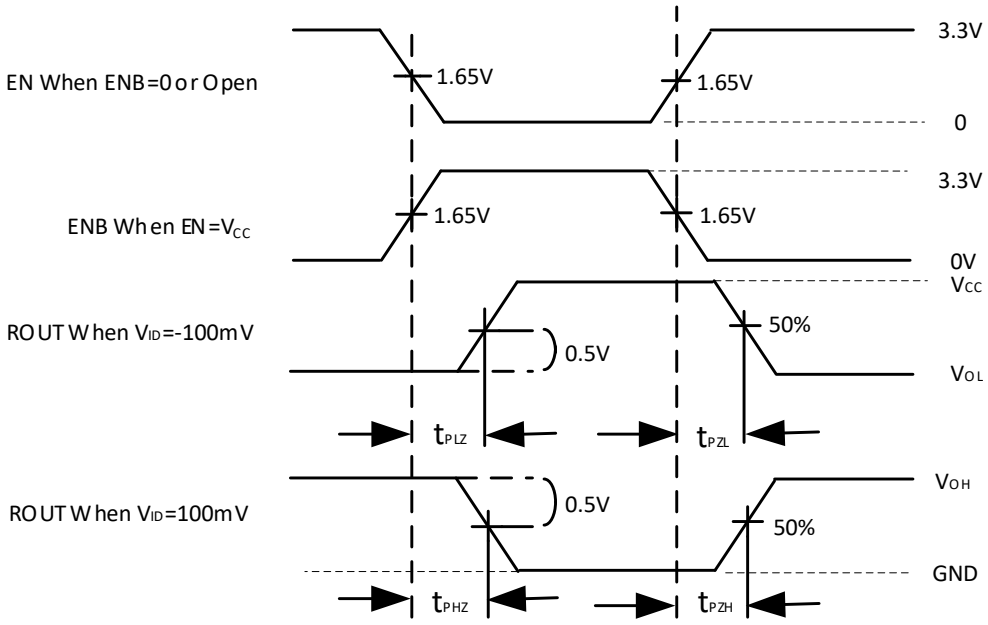
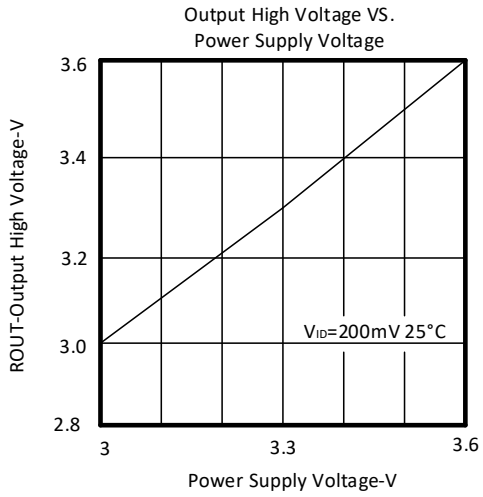
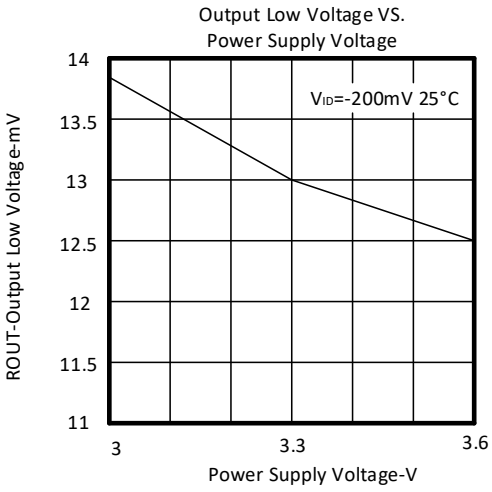
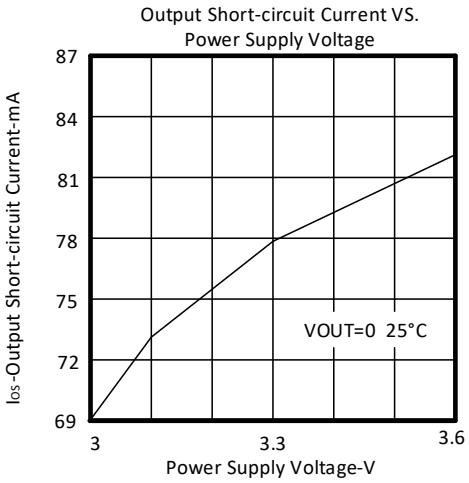


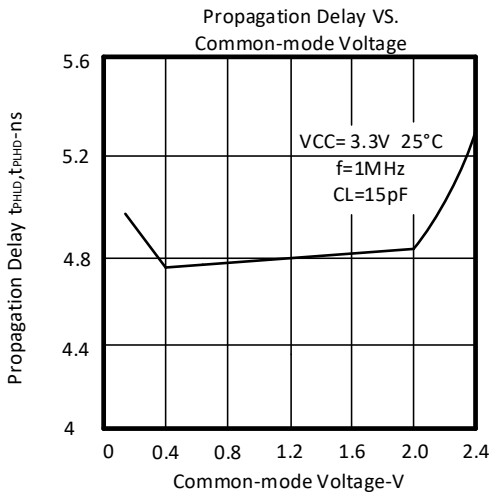
Figure 4. Three-state Delay Waveform

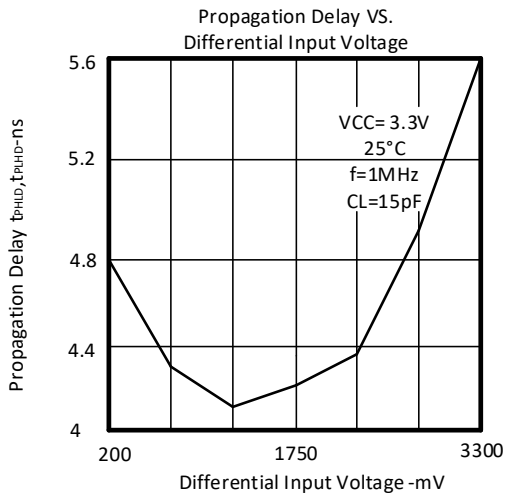
TYPICAL CHARACTERISTICS CURVE

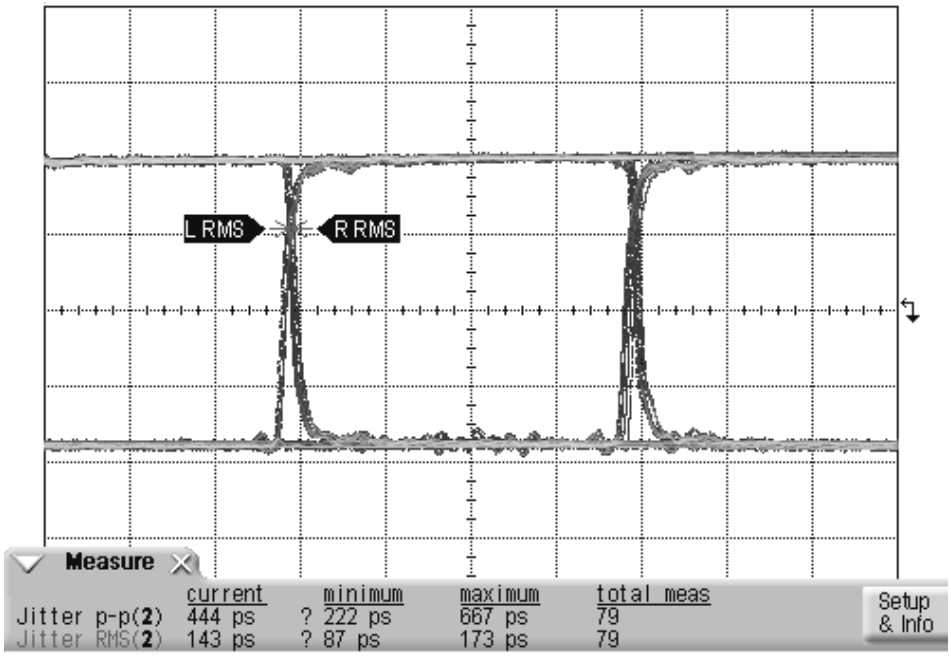




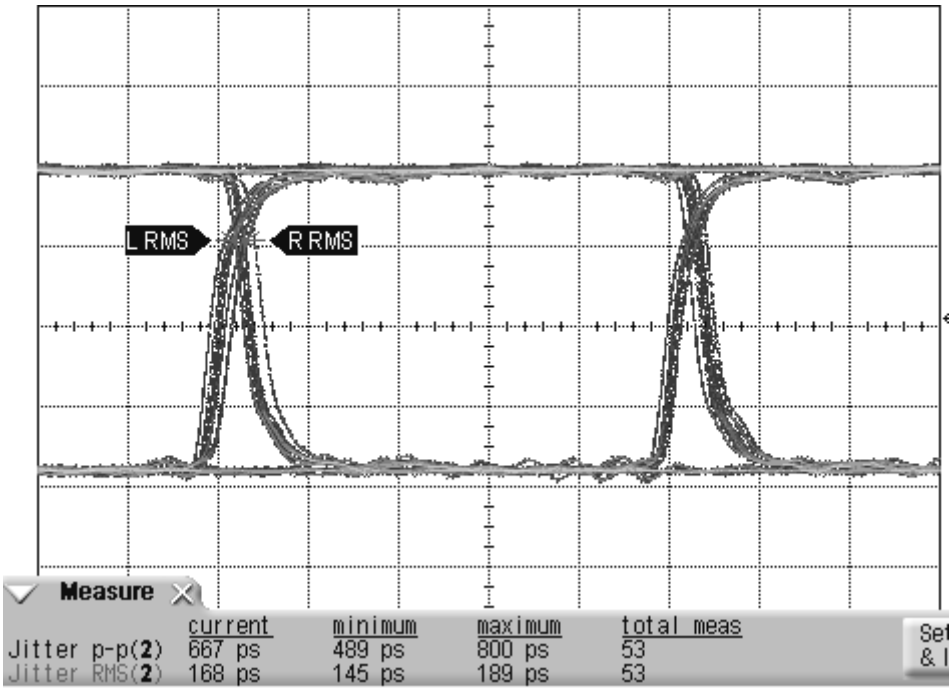








The Eye Diagram of the MS21147T as Driver and the MS21148T as Receiver: V_{CC}=3.3V, PRBS7 50Mbps CAT5E 10m



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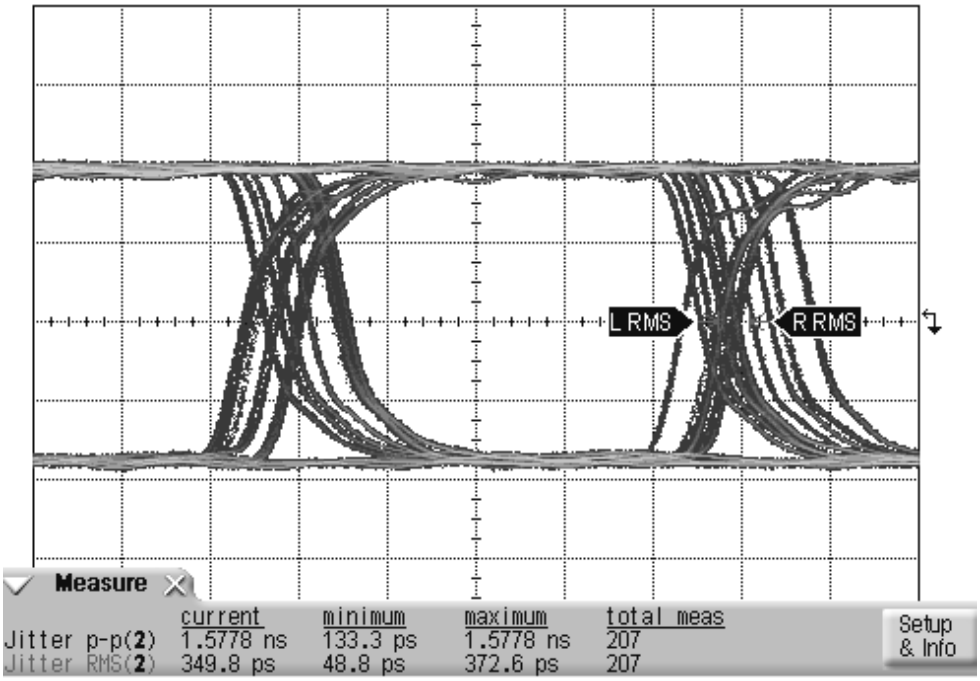
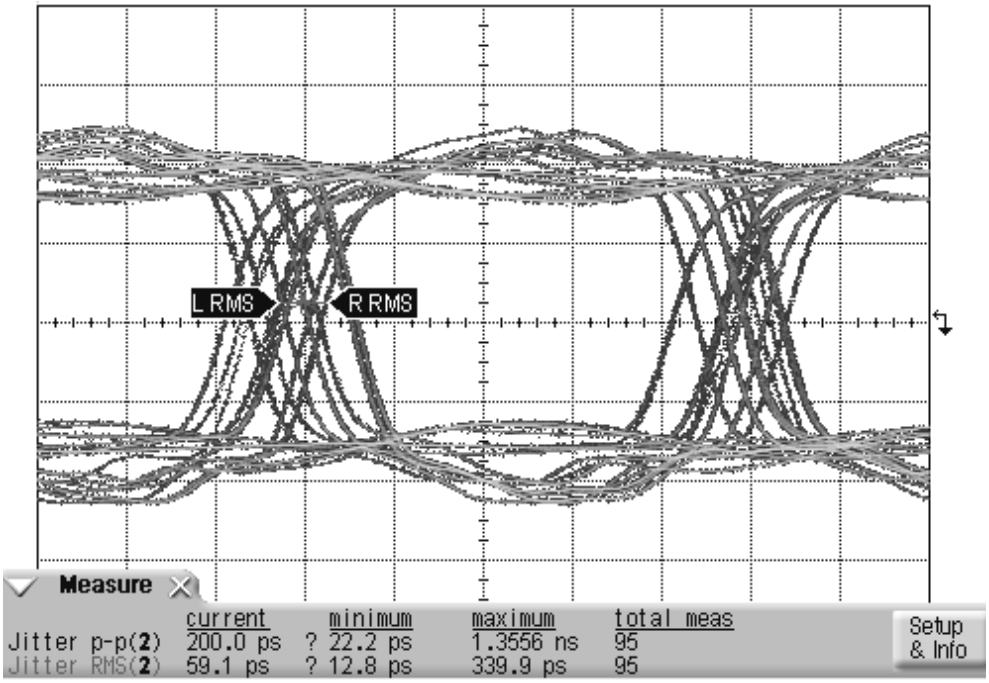


The Eye Diagram of the MS21147T as Driver and the MS21148T as Receiver: V_{CC}=3.3V, PRBS7 200Mbps CAT5E 4.5m



The Eye Diagram of the MS21147T as Driver and the MS21148T as Receiver: V_{CC}=3.3V,PRBS7 200Mbps CAT6E 10m

FUNCTION DESCRIPTION

The MS21148T is a four channel LVDS differential cable receiver, meeting the electrical characteristics of low voltage differential signaling (LVDS). The transmission media could be PCB traces, backplane or cables. The data rate and distance depend on the media attenuation characteristic, noise environment and other system characteristics.

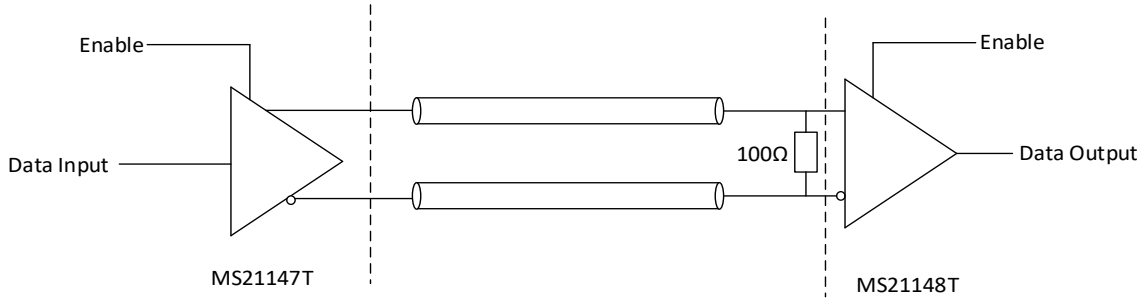
The MS21148T could receive LVDS level, and transform it to CMOS logical level. The MS21148T also has three-state output function, controlled by EN and ENB pins. In addition, the power dissipation would decrease when the MS21148T is disabled. The enable function table is shown as follows.

Enable		Differential Input	Output
EN	ENB	RINP-RINN	ROUT
H	L or Open	$V_{ID} \geq 100mV$	H
H	L or Open	$V_{ID} \leq -100mV$	L
H	L or Open	Open, Short-circuit or Input Terminate	H
Others		X	Z

The forward and reverse voltage threshold are between 50mV and 70mV typically.

The MS21148T has failure safe function. If the LVDS differential input terminals are in shorted or open condition, the output is set as high level. In addition, if the input terminals of the MS21148T are terminated, for examples, the driver output is high impedance or without cable or power down, the output is high level as well. Pay attention to that, If the four channels of the MS21148T are not used totally, the LVDS input terminates of unused channels must be left floating.

TYPICAL APPLICATION DIAGRAM



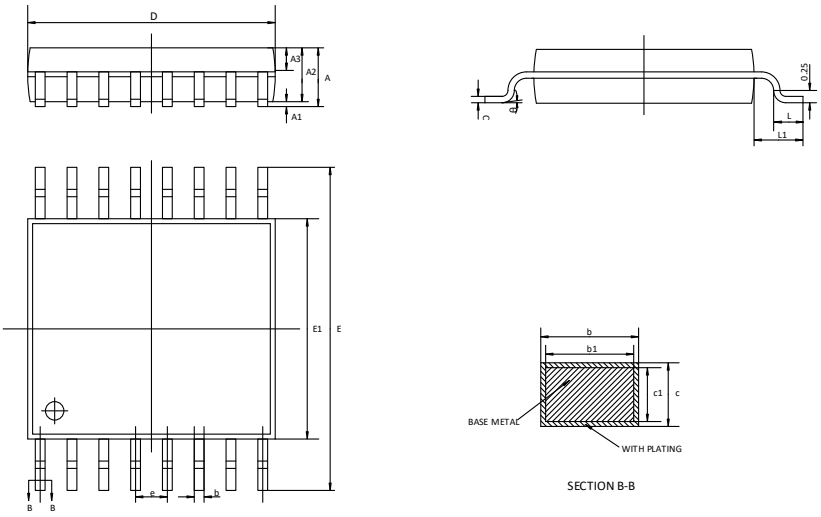
The typical application is shown as above. The MS21148T could act as receiver for other LVDS driver (such as MS21147T). The MS21148T has TSSOP package and the pin configuration makes it easy to perform PCB layout. It is necessary to connect with 100Ω load resistor, which is close to receiving side to achieve perfect data transmission effect.

Transmission Distance

Normally, the MS21147T is used to cooperate with the MS21148T together. For CAT5E network line, at least 10 meters could be reached for data rate less than 100Mbps. While the rate increases to 200Mbps, the transmission distance would reduce to about 5 meters. When the transmission distance is less than 0.5 meter and the data rate is below 200Mbps, most cables could be used.

PACKAGE OUTLINE DIMENSIONS

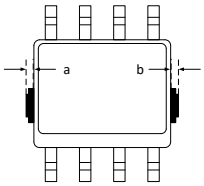
TSSOP16



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	-	8°

Note: In addition to the package size, a, b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.



MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description

Product Name: MS21148T

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS21148T	TSSOP16	3000	1	3000	8	24000

STATEMENT

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.


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