

## 10 to 16 Bit, R/D Converter with Built-in Reference Oscillator

### FEATURES

- Maximum Tracking Rate: 3125rps (10-bit Resolution Rate)
- Angular Accuracy:  $\pm 2.5$  Arc Minutes (+1LSB)
- Configurable Resolution Rate: 10/12/14/16 Bits
- Parallel and Serial 10-bit to 16-bit Data Ports
- Position and Velocity Outputs
- System Fault Detection
- Programmable Fault Detection Threshold
- Differential Inputs
- Integration Incremental Encoder Emulation
- Built-in Programmable Sine Wave Excitation Source
- Compatible with DSP and SPI Interface Protocol
- Power Supply: 5V, Interface Voltage: 2.3V to 5V
- Operating Temperature Range:  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$

### PRODUCT DESCRIPTION

The MS5910PA is a resolver-to-digital converter, which can configure the 10-bit to 16-bit resolution rate. The sine wave excitation circuit is integrated on this chip. Peak-to-peak amplitude that sine and cosine allow to input is from 2.3V to 4.0V. And The frequency range is from 2kHz to 20kHz. The converter can output angles and digits corresponding to velocity in parallel and serial.

The MS5910PA is available in LQFP48 package.

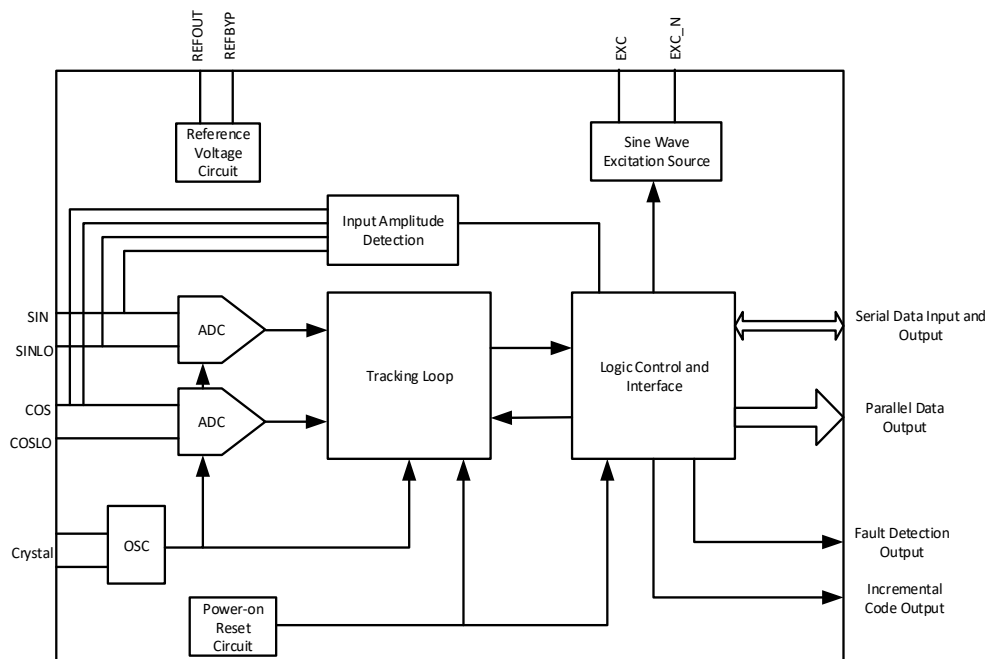
### APPLICATIONS

- Servo Motor Control
- Encoder Emulation
- Electric Power Steering
- Alternator
- Vehicle Motion Detection and Control

### PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5910PA	LQFP48	MS5910PA

### BLOCK DIAGRAM

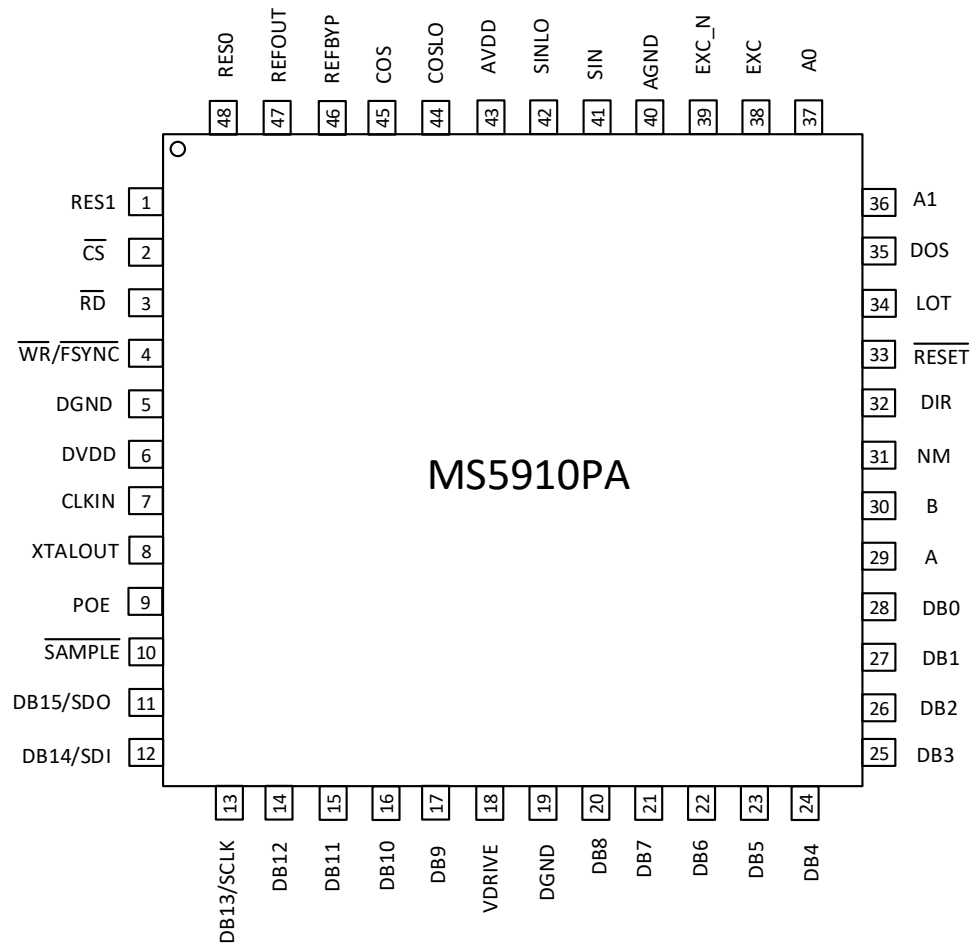


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## PIN CONFIGURATION



## PIN DESCRIPTION

Pin	Name	Type	Description
1	RES1	I	Resolution Configuration 1. Using RES1 and RES0 to configure the resolution rate of the MS5910PA.
2	$\overline{CS}$	I	Chip Select, Active-low Enable
3	$\overline{RD}$	I	Edge-triggered. When POE is equal to 1, frame synchronization signal from DB15 to DB0 and enabling signal output in parallel. When POE is equal to 0, the $\overline{RD}$ pin should keep in high level. When $\overline{CS}$ and $\overline{RD}$ are in low level, output buffer enable.
4	$\overline{WR}/\overline{FSYNC}$	I	Edge-triggered. When POE is equal to 1, frame synchronization signal from DB7 to DB0 and enabling signal output in parallel. When POE is equal to 0, frame synchronization signal and enabling signal are used as serial data bus. When $\overline{CS}$ and $\overline{WR}/\overline{FSYNC}$ are in low level, input buffer enable.
5	DGND	-	Digital Ground.
6	DVDD	-	Digital Power Supply. The 4.7 $\mu$ F and 0.01 $\mu$ F capacitors are recommended to be coupled to ground.
7	CLKIN	I	Clock Input. A crystal or oscillator can provide clock for the MS5910PA, and provide the single-ended clock for the CLKIN pin. The rated frequency range is from 6.144MHz to 10.24 MHz.
8	XTALOUT	O	Crystal Oscillator Output. When using a crystal or oscillator clock, the crystal should be applied to CLKIN and XTALOUT pins. When using a single-ended clock source, XTALOUT should not be in connection.
9	POE	I	Parallel Output Enable, Select Serial or Parallel Interface. 1: Parallel Interface; 0: Serial Interface.
10	$\overline{SAMPLE}$	I	Update Register. When $\overline{SAMPLE}$ is in falling edge, data are transferred from position and velocity integrators to the relevant register. The fault register is also updated.

Pin	Name	Type	Description
11	DB15/SDO	O	Data Output Bit 15/Serial Data Output. When POE is equal to 1, this pin is used as DB15. When POE is equal to 0, this pin is used as SDO.
12	DB14/SDI	O/I	Data Output Bit 14 /Serial Data Input Bus. When POE is equal to 1, this pin is used as DB14. When POE is equal to 0, this pin is used as SDI.
13	DB13/SCLK	O/I	Data Output Bit 13 /Serial Data Input Clock. When POE is equal to 1, this pin is used as DB13; When POE is equal to 0, this pin is used as SCLK.
14	DB12	O	Data Output Bit 12.
15	DB11	O	Data Output Bit 11.
16	DB10	O	Data Output Bit 10.
17	DB9	O	Data Output Bit 9.
18	VDRIVE	-	Logic Interface Power Supply. The 4.7 $\mu$ F and 0.01 $\mu$ F capacitors are recommended to be coupled to ground.
19	DGND	-	Digital Ground.
20	DB8	O	Data Output Bit 8.
21	DB7	I/O	Data Bit 7.
22	DB6	I/O	Data Bit 6.
23	DB5	I/O	Data Bit 5.
24	DB4	I/O	Data Bit 4.
25	DB3	I/O	Data Bit 3.
26	DB2	I/O	Data Bit 2.
27	DB1	I/O	Data Bit 1.
28	DB0	I/O	Data Bit 0.
29	A	O	Incremental Encoder Emulation Output A.
30	B	O	Incremental Encoder Emulation Output B.
31	NM	O	North Marker Incremental Encoder Emulation Output.
32	DIR	O	Rotation Direction. 1: Clockwise 0: Counter Clockwise
33	$\overline{\text{RESET}}$	I	Chip Reset Signal, Effective in Low Level.
34	LOT	O	Tracking Loss.

Pin	Name	Type	Description
35	DOS	O	Signal Degradation.
36	A1	I	Mode Configuration Pin 1. Using A1 and A0 to configure the MS5910PA mode.
37	A0	I	Mode Configuration Pin 0.
38	EXC	O	On-chip Integrated Excitation Signal Positive Output.
39	EXC_N	O	On-chip Integrated Excitation Signal Complementary Output.
40	AGND	-	Analog Ground.
41	SIN	I	Positive Analog Input of Differential Pair SIN/SINLO. Input range of differential pair is from 2.3Vp-p to 4.0Vp-p.
42	SINLO	I	Negative Analog Input of Differential Pair SIN/SINLO. Input range of differential pair is from 2.3Vp-p to 4.0Vp-p.
43	AVDD	-	Analog Power Supply. The 4.7 $\mu$ F and 0.01 $\mu$ F capacitors are recommended to be coupled to ground.
44	COSLO	I	Negative Analog Input of Differential Pair COS/COSLO. Input range of differential pair is from 2.3Vp-p to 4.0Vp-p.
45	COS	I	Positive Analog Input of Differential Pair COS/COSLO. Input range of differential pair is from 2.3Vp-p to 4.0Vp-p.
46	REFBYP	-	Reference Voltage Bypass. The 10 $\mu$ F and 0.01 $\mu$ F capacitors are recommended to be coupled to ground.
47	REFOUT	O	Reference Voltage.
48	RES0	I	Resolution Configuration Pin 0. Using RES1 and RES0 to configure the resolution rate of the MS5910PA.

## ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter		Range	Unit
Analog Power Supply Range	AVDD to AGND, DGND	-0.3 ~ +7.0	V
Digital Power Supply Range	DVDD to AGND, DGND	-0.3 ~ +7.0	V
Logic Interface Power Supply Range	VDRIVE to AGND, DGND	-0.3 ~ +7.0	V
Analog Power Supply to Digital Power Supply	AVDD to DVDD	-0.3 ~ +0.3	V
Analog Ground to Digital Ground	AGND to DGND	-0.3 ~ +0.3	V
Analog Input Voltage Range		-0.3 ~ AVDD+0.3	V
Logic Input Voltage Range		-0.3 ~ VDRIVE+0.3	V
Logic Output Voltage Range		-0.3 ~ VDRIVE+0.3	V
Analog Output Voltage Range		-0.3 ~ AVDD+0.3	V
Storage Temperature Range	T <sub>STG</sub>	-65 ~ 150	°C
Soldering Temperature(10s)		260	°C
ESD (HBM)	V <sub>ESD</sub>	±5000	V
Operating Temperature Range	T <sub>A</sub>	-40 ~ 125	°C

## ELECTRICAL CHARACTERISTICS

Unless otherwise noted, AVDD = DVDD = 5.0 V  $\pm$  5%, CLKIN = 8.192 MHz  $\pm$  25%, EXC Frequency = 10 kHz to 20 kHz (10 Bits), 6 kHz to 20 kHz (12 Bits), 3kHz to 12 kHz (14 Bits), 2 kHz to 10 kHz (16 Bits); T<sub>A</sub> = 25°C.

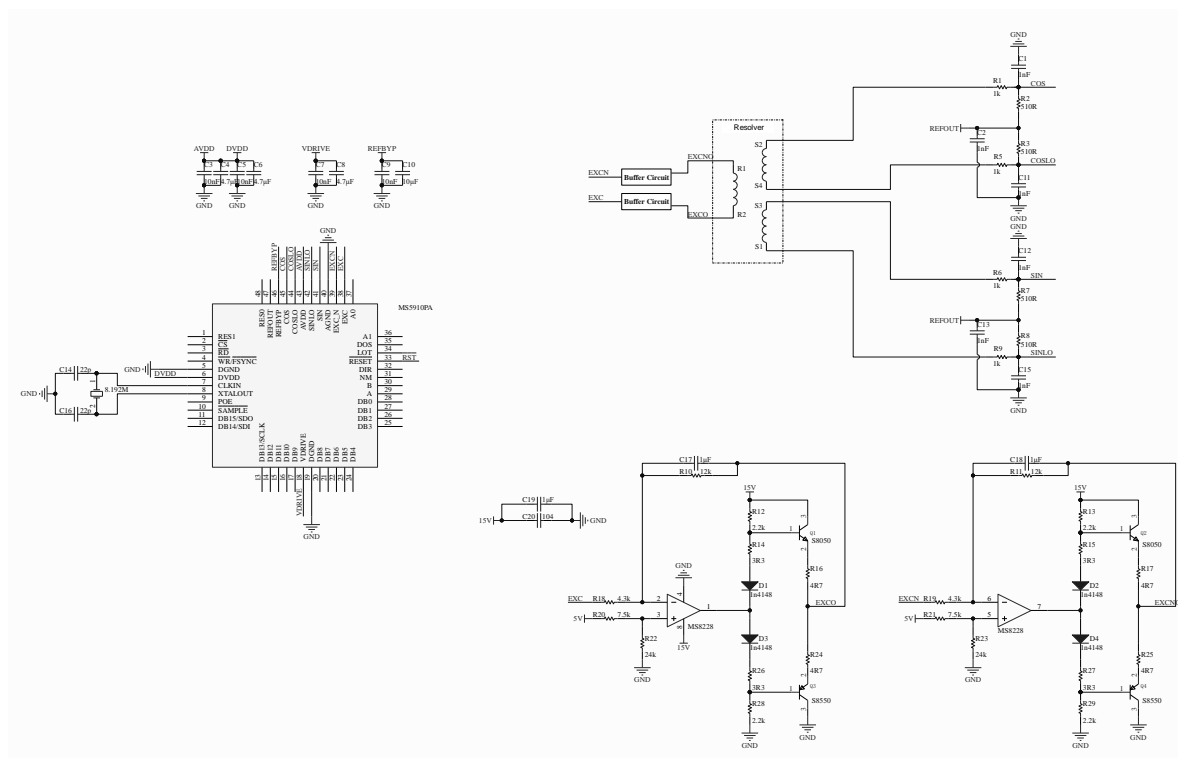
Parameter	Condition	Min	Typ	Max	Unit
Sine, Cosine Inputs					
Voltage Amplitude	Differential SIN to SINLO, COS to COSLO	2.3	3.15	4.0	Vp-p
Input Bias Current	V <sub>IN</sub> = 4.0 V p-p, CLKIN = 8.192MHz			14.2	μA
Input Impedance	V <sub>IN</sub> = 4.0 V p-p, CLKIN = 8.192MHz	280			kΩ
Phase Lock Range	Sine/Cosine Phase Offset from EXC, Control Register D3 = 0	-44		+44	Degree
Common-mode Rejection	10Hz to 1MHz, Control Register D4 = 0		±30		arc sec/V
Angular Accuracy					
Angular Accuracy			±2.5+1LSB	±4+1LSB	arc min
Resolution Rate	No Missing Codes	10,12,14,16			Bit
Integral Nonlinearity (INL)	10Bit			±2	LSB
	12Bit			±2	LSB
	14Bit			±4	LSB
	16Bit			±16	LSB
Differential Nonlinearity (DNL)			±1		LSB
Repeatability			±1		LSB
Velocity Outputs					
Velocity Accuracy	10Bit, Zero Acceleration		±0.44	±4	LSB
	12Bit, Zero Acceleration		±0.7	±4	LSB
	14Bit, Zero Acceleration		±2.2	±8	LSB
	16Bit, Zero Acceleration		±2.4	±32	LSB
Resolution Rate		9, 11, 13, 15			Bit
Dynamic Characteristics					
Bandwidth	10Bit, CLKIN = 8.192MHz	2900		5300	Hz
	12Bit, CLKIN = 8.192MHz	1200		2200	Hz
	14Bit, CLKIN = 8.192MHz	600		1200	Hz
	16Bit, CLKIN = 8.192MHz	125		275	Hz



Parameter	Condition	Min	Typ	Max	Unit
Tracking Rate	10Bit, CLKIN = 8.192MHz			2500	rps
	12Bit, CLKIN = 8.192MHz			1000	rps
	14Bit, CLKIN = 8.192MHz			500	rps
	16Bit, CLKIN = 8.192MHz			125	rps
	10Bit, CLKIN = 10.24MHz			3125	rps
	12Bit, CLKIN = 10.24MHz			1250	rps
	14Bit, CLKIN = 10.24MHz			625	rps
	16Bit, CLKIN = 10.24MHz			156.25	rps
Acceleration Error	10Bit, 50,000 rps2, CLKIN = 8.192MHz		30		arc min
	12Bit, 10,000 rps2, CLKIN = 8.192MHz		30		arc min
	14Bit, 2500 rps2, CLKIN = 8.192MHz		30		arc min
	16Bit, 125 rps2, CLKIN = 8.192MHz		30		arc min
Set-up Time 10° Step Input	10Bit, Settle to $\pm 2$ LSB, CLKIN = 8.192MHz		0.44		ms
	12Bit, Settle to $\pm 2$ LSB, CLKIN = 8.192MHz		2.16		ms
	14Bit, settle to $\pm 2$ LSB, CLKIN = 8.192MHz		7.15		ms
	16Bit, Settle to $\pm 2$ LSB, CLKIN = 8.192MHz		26.79		ms
Set-up Time 179° Step Input	10Bit, Settle to $\pm 2$ LSB, CLKIN = 8.192MHz		1.53		ms
	12Bit, Settle to $\pm 2$ LSB, CLKIN = 8.192MHz		5.32		ms
	14Bit, Settle to $\pm 2$ LSB, CLKIN = 8.192MHz		15.13		ms
	16Bit, Settle to $\pm 2$ LSB, CLKIN = 8.192MHz		40.2		ms
<b>EXC, EXC_N Outputs</b>					
Voltage	Load $\pm 100\mu A$ , Typical Differential Output (EXC to EXC_N) = 7.8Vp-p		3.9		Vp-p
Center Voltage			2.43		V
Frequency		2		20	kHz
DC Mismatch			7	30	mV
AC Mismatch			0	100	mV
Total Harmonic Distortion	First Five Harmonics		-53.98		dB

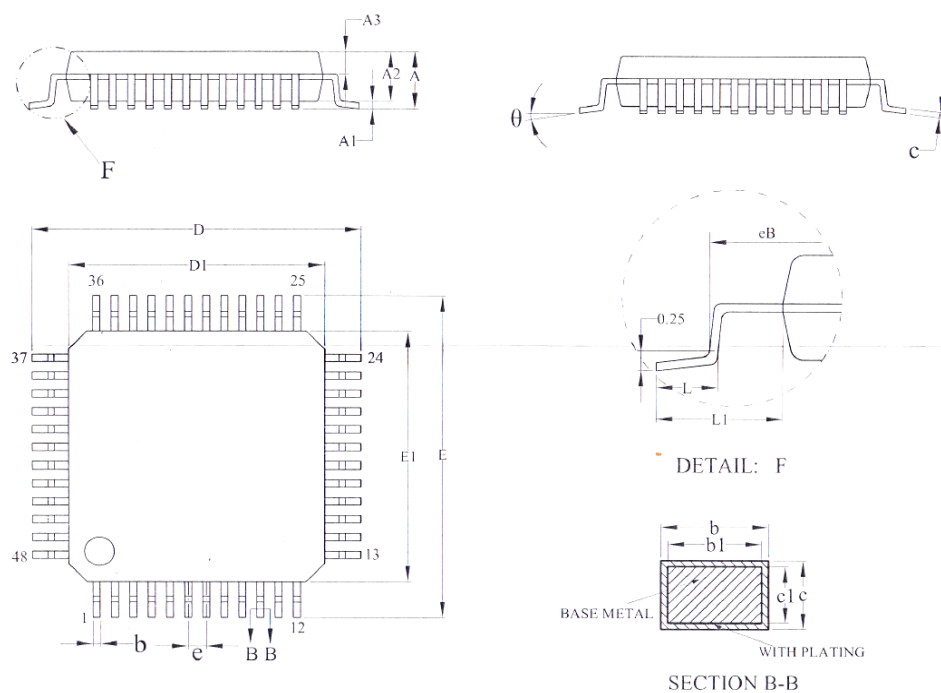
Parameter	Condition	Min	Typ	Max	Unit
<b>Reference Voltage Source</b>					
REFOUT	$\pm I_{OUT} = 100\mu A$	2.37	2.433	2.49	V
Temperature Drift			32.8		ppm/°C
PSRR			-67.95		dB
<b>CLKIN</b>					
Low-level Input Voltage ( $V_{IL}$ )				0.8	V
High-level Input Voltage ( $V_{IH}$ )		2.0			V
<b>Logic Inputs</b>					
Low-level Input Voltage ( $V_{IL}$ )	VDRIVE = 2.7V to 5.25V			0.75	V
	VDRIVE = 2.3V to 2.7V			0.7	
High-level Input Voltage ( $V_{IH}$ )	VDRIVE = 2.7V to 5.25V	2.2			V
	VDRIVE = 2.3V to 2.7V	1.9			
Low-level Input Current	$I_{IL}$ (Non Pull-up)			10	$\mu A$
Low-level Input Current	$I_{IL}$ (Pull-up)			70	$\mu A$
High-level Input Current		-10			$\mu A$
<b>Logic Outputs</b>					
Low-level Output Voltage ( $V_{OL}$ )				0.4	V
High-level Output Voltage ( $V_{OH}$ )	VDRIVE = 2.7 V to 5.25 V	2.4			V
	VDRIVE = 2.3 V to 2.7 V	2.0			V
High-level Three-state Leakage Current ( $I_{OZH}$ )		-10			$\mu A$
Low-level Three-state Leakage Current ( $I_{OZL}$ )				10	$\mu A$
<b>Power Supply</b>					
AVDD		4.5		5.5	V
DVDD		4.5		5.5	V
VDRIVE		2.3		5.5	V
<b>Power Dissipation</b>					
$I_{AVDD}$	CLKIN = 8.192MHz		8.25	12	mA
$I_{DVDD}$	CLKIN = 8.192MHz		14.4	20	mA
$I_{DRIVE}$	CLKIN = 8.192MHz		0.12	1	mA

## TYPICAL APPLICATION



## PACKAGE OUTLINE DIMENSIONS

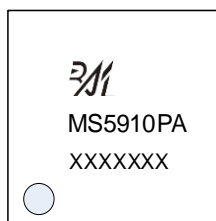
**LQFP48 (0707x1.4)**



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
$\theta$	0	-	7°

## MARKING and PACKAGING SPECIFICATION

### 1. Marking Drawing Description



Product Name: MS5910PA

Product Code: XXXXXXXX

### 2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

### 3. Packaging Specification

Device	Package	Piece/Plate	Plate/Box	Piece/Box	Box/Carton	Piece/Carton
MS5910PA	LQFP48	250	10	2500	4	10000

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5910PA	LQFP48	1000	1	1000	8	8000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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