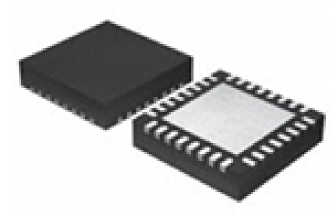
High-Precision Time-to-Digital Converter (TDC) for Laser Ranging

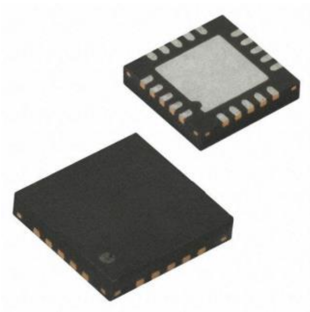
PRODUCT DESCRIPTION

The MS1002 is a high-precision time-to-converter (TDC) with higher precision and smaller package, suiting for low-cost time measurement applications.

The MS1002 has the dual-channel and multi-pulse sampling ability. In addition, it has high-speed SPI communication and various measurement modes, suiting for laser radar and laser ranging.



QFN32



QFN20

FEATURES

Measurement Range 1:

- Dual Channel, Minimum Resolution Rate: 70ps
- Measurement Range: 0-1.8μs
- Interval Pulse Resolution: 15ns. Each Channel can be Sampled for 4 Times.
- Measuring the Time Interval between Any 2 of 4 Samples.
- Trigger to Rising or/and Falling Edge Chosen by the Input Signal

Measurement Range 2:

- Single Channel, Minimum Resolution Rate: 70ps
- Measurement Range: 500ns-4ms@4MHz
- The Resolution of Interval Pulses is Two Calibration Clock Cycles and can be Sampled for 3 Times.
- Trigger to Rising or/and Falling Edge Chosen by the Input Signal
- 3 Denoising Windows Filter Each of the Three Samples

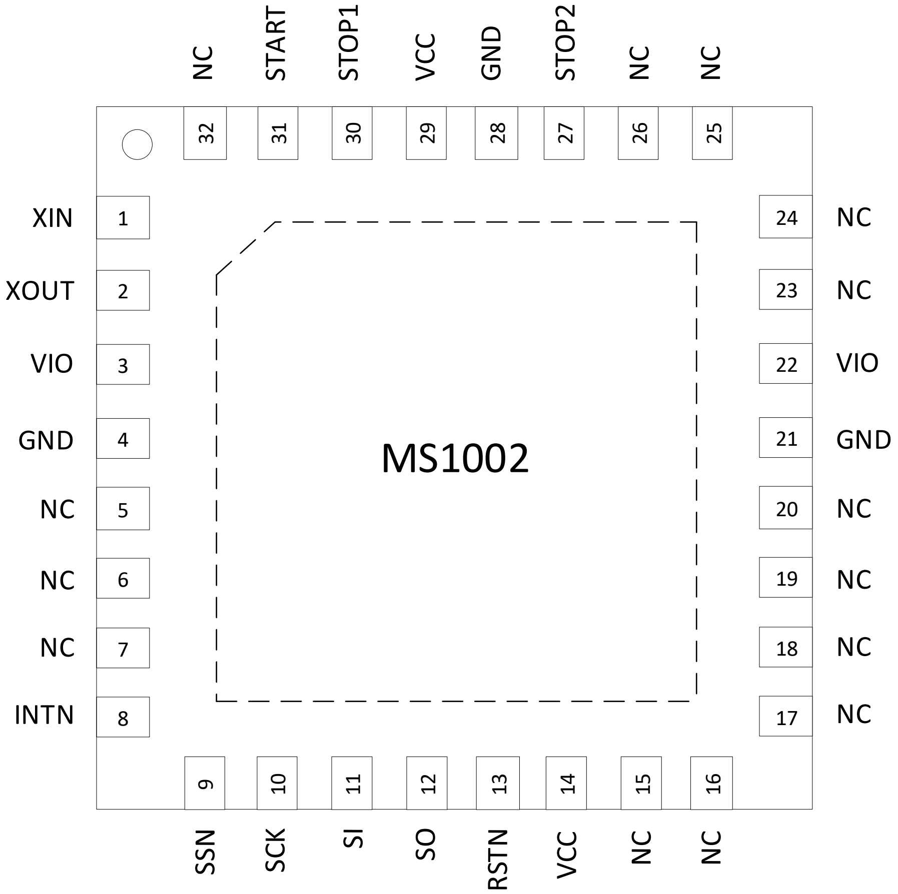
APPLICATIONS

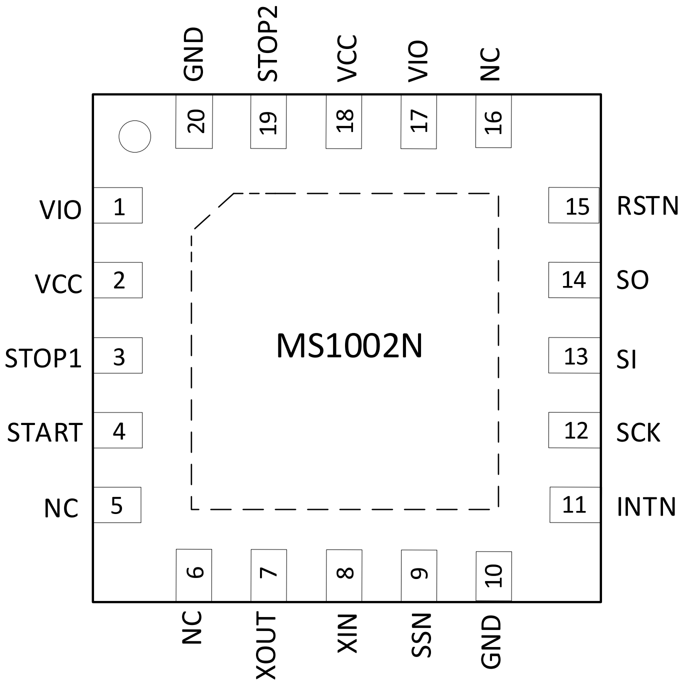
- Laser Radar
- Laser Ranging
- Pulse Measurement

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS1002	QFN32	MS1002
MS1002N	QFN20	MS1002N

PIN CONFIGUREATION

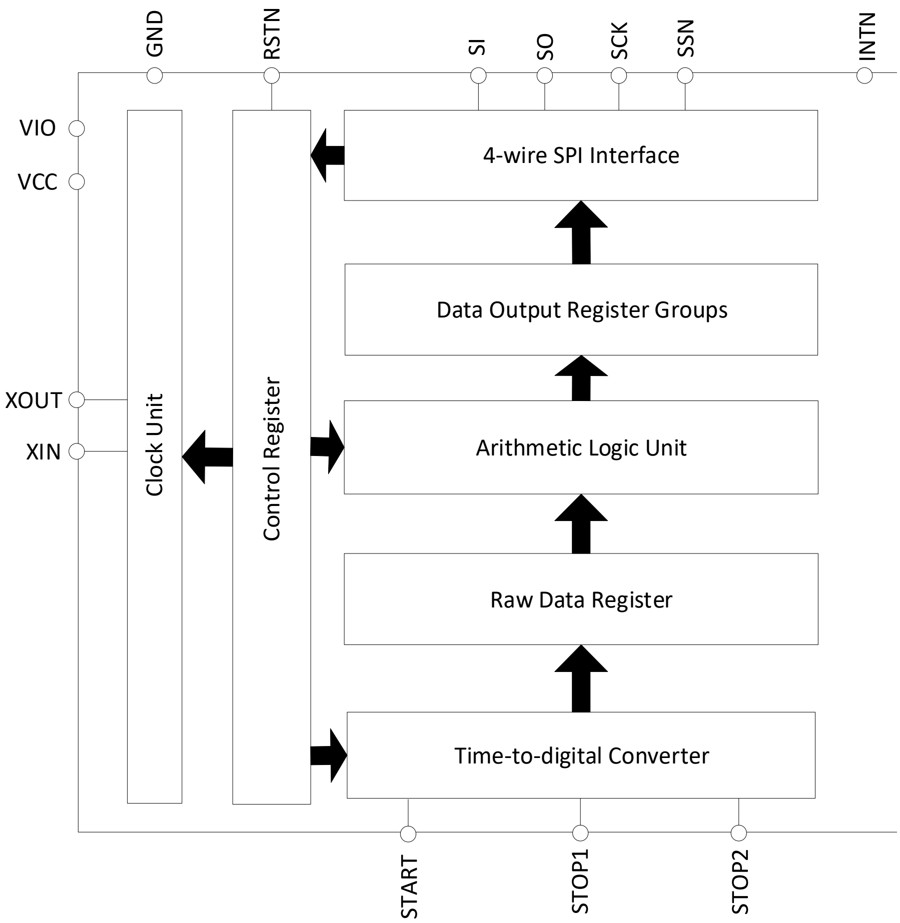




PIN DESCRIPTION

Pin		Name	Type	Description
MS1002	MS1002N			
4, 21, 28	10, 20	GND	-	Ground
3, 22	1, 17	VIO	-	Port Power
14, 29	2, 18	VCC	-	Core Power
5, 6, 7, 15, 16, 17, 18, 19, 20, 23, 24, 25, 26, 32	5, 6, 16	NC	-	Not Connection
1	8	XIN	I	High-speed Crystal Drive Input
2	7	XOUT	O	High-speed Crystal Drive Output
9	9	SSN	I	SPI Slave Select Interface, Effective in Low Level
10	12	SCK	I	SPI Clock Input Interface
11	13	SI	I	SPI Data Input Interface
12	14	SO	O	SPI Data Output Interface, High Impedance When SPI is Free
13	15	RSTN	I	System Reset Input, Effective in Low Level
8	11	INTN	O	Interrupt Flag, Effective in Low Level
27	19	STOP2	I	Stop Channel 2
30	3	STOP1	I	Stop Channel 1
31	4	START	I	Start Channel

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn’t represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Core Power Supply	V_{CC}	-0.3 ~ 4	V
I/O Power Supply	V_{IO}	-0.3 ~ 6	V
Output Current	I_{OUT}	30	mA
Storage Temperature	T_{STG}	-65 ~ 150	°C
ESD (HBM)	V_{ESD}	>4	kV

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted, the ambient temperature T_A = 25°C ±2°C。

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Core Power Supply[1]	V_{CC}	$V_{IO}>V_{CC}$	1.8		3.6	V
I/O Power Supply	V_{IO}		1.8		5.5	V
Normal Input Rising-edge Time	t_{ri}				50	ns
Normal Input Falling-edge Time	t_{fa}				50	ns
Operating Temperature	T_A		-40		125	°C

Note 1: including Crystal Pins XIN, XOUT.

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{IO} = V_{CC}= 3.0V, T_J = -40°C to +85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
4 MHz Crystal Current	I_{hs}	V_{CC}=V_{IO}= 3.6V		260		µA
Time Measurement Unit Current	I_{tmu}	Start When in Time Measurement		15		mA
Quiescent Current	I_{DDQ}	All Clocks Off@85°C		<0.1		µA
Input Leakage Current	I_L		-1		+1	µA
High-level Output Voltage	V_{OH}	I_{OH}=tbd mA, V_{IO}=Min	V_{IO}-0.4			V
Low-level Output Voltage	V_{OL}	I_{OL}=tbd mA, V_{IO}=Min			0.4	V
High-level Input Voltage	V_{IH}	LVTTL, V_{IO}= Max	2.0			V
Low-level Input Voltage	V_{IL}	LVTTL, V_{IO} = Min			0.8	V

Terminal Equivalent Capacitance

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Digital Input	C_{in}	When V_{CC} = V_{IO}, f = 1 MHz, T_A=25°C		10		pF
Digital Output	C_o			10		pF
Bidirectional	C_{io}			10		pF

Time Measurement Unit

VIO=VCC=3.0V, T_J=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Measurement Resolution Rate	LSB	V_{IO} = V_{CC} = 3.3 V		25 °C 3.3 V		ps
				70		
Standard Deviation	σ	V_{IO} = V_{CC} = 3.3 V T_A= 25°C		50		ps

Clock Oscillator

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-speed Crystal Reference Clock	Clk_{HS}		1	4	8	MHz
Oscillator Start-up Time with Ceramic Crystal	t_{oszst}			100		µs
Oscillator Start-up Time with Quartz Crystal	t_{oszst}			1		ms

FUNCTION DESCRIPTION

1. SPI Interface

The SPI interface of the MS1002 is compatible with 4-wire SPI, which needs a SerialSelectNot (SSN) signal and has no ability to operate in 3-wire SPI interface.

The falling edge of the SSN or the rising edge of the first SCK would reset the state of INTN pin (interrupt pin) .

Transition starts from the highest bit (MSB), finishes with the lowest bit (LSB) and completed in bytes. Data transmission can stop by sending a LOW-HIGH-LOW level to SSN after each byte.

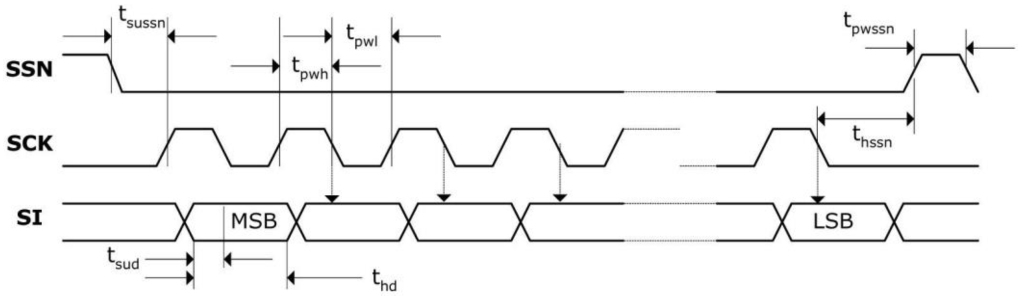


Figure 1. SPI Write

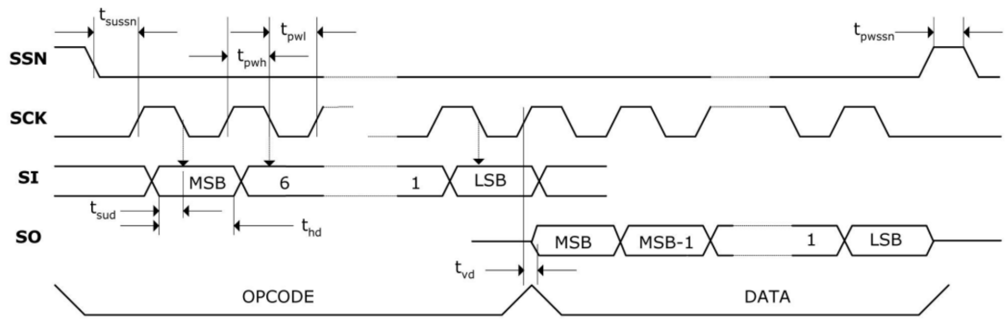


Figure 2. SPI Read

Parameter	Symbol	VIO=2.5V	VIO=3.3V	Unit
Serial Clock Frequency	f_{clk}	25(Max)	40(Max)	MHz
Serial Clock, High Pulse	t_{pwh}	20(Min)	12(Min)	ns
Serial Clock, Low Pulse	t_{pwl}	20(Min)	13(Min)	ns
SSN Enables to Valid Clock Edge	t_{sussn}	20(Min)	20(Min)	ns
SSN Pulse Width between Write Cycles	t_{pwssn}	25(Min)	25(Min)	ns
SSN Hold Time after SCK Falling-edge	t_{hssn}	15(Min)	15(Min)	ns
Data Valid to SCK Falling-edge Time	t_{sud}	5(Min)	5(Min)	ns
Data Hold Time after SCK Falling Edge	t_{hd}	5(Min)	5(Min)	ns
Time from SCK Rising Edge to Data Valid	t_{vd}	15(Min)	10(Min)	ns

2. System Reset Timing

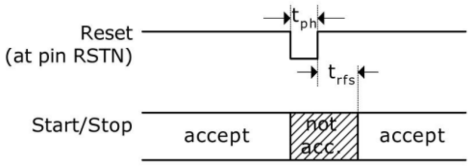


Figure 3. System Reset Timing

Parameter	Symbol	Min	Max	Unit
Reset Pulse Width	t_{ph}	30	--	ns
Time after Rising Edge of Reset Pulse before Pulses are Accepted	t_{rfs}	30	--	ns

3. Power Supply

To receive good measurement results, the power supply characteristics is very important. And the power supply should feature high capacitance and low inductance.

The MS1002 provides two pairs of power supply terminals:

VIO - I/O Power Supply

VCC - Core Power Supply

All of Ground pins should be connected to the ground plane of the printed circuit board. VIO and VCC can be provided by a battery or fixed linear voltage regulator. Do not use switched regulators to avoid disturbance caused by I/O power supply.

The time-to-digital converter can achieve good measurement results depending entirely on good power supply. The pulsed current is mainly used for the chip measurement, so a sufficient two-pass filter is very important:

VIO 47 µF (Minimum 22 µF)

VCC 100 µF (Minimum 22 µF)

The voltage is provided by an analog regulator. We recommend not to use the switched voltage regulators.

4. Opcode and Registers

4.1 Configuration Register

The MS1002 has 6 groups of 24-bit configuration registers.

Register 0 (REG0, Address: 0x80)

Bits	Def	Parameter	Description	Setting
23	0	n.c.	Keep the Default Values	
22	0			
21	1			
20	0			
19	0			
18	0			
17	1			
16	0			
15	0			
14	0			
13	0	ClkHSDiv	Set the Frequency Division Factor of CLKHS High-speed Reference Clock	0 = Non Frequency Division 1 = 2 Frequency Division 2 = 4 Frequency Division 3 = 4 Frequency Division
12	0			
11	0	START_CLKHS	Enable the High-speed Oscillator	0 = Oscillator off 1 = Oscillator on 2 = Set the Crystal Oscillator Start Time =640µs 3 = Set the Crystal Oscillator Start Time=1280µs
10	1			
9	1	n.c.	Keep the Default Values	
8	0			
7	0			
6	1			
5	1	CALIBRATE	Enable/Disable Calibration in ALU	0 = Calibration off (Only Allowed in Measurement Range 1) 1 = Calibration on (Recommended)
4	0	DisAutoCal	Enable/Disable Auto-calibration Run in TDC	0 = Auto-calibration after Measurement 1 = Auto-calibration Disabled

Bits	Def	Parameter	Description	Setting
3	1	MRange2	Select Measurement Range 2	0 = Measurement Range 1 1 = Measurement Range 2
2	0	NEG_STOP2	Inverted Stop Channel 2 Input	0 = Non-inverted Input Signal-Rising Edge 1 = Inverted Input Signal-Falling Edge
1	0	NEG_STOP1	Inverted Stop Channel 1 Input	0 = Non-inverted Input Signal-Rising Edge 1 = Inverted Input Signal-Falling Edge
0	0	NEG_START	Inverted Start Channel 1 Input	0 = Non-inverted Input Signal-Rising Edge 1 = Inverted Input Signal-Falling Edge

Register 1 (REG1, Address: 0x81)

<table>
<tr><th>Bits</th><th>Def</th><th>Parameter</th><th>Description</th><th colspan="2">Setting</th></tr>
<tr><td>23</td><td>0</td><td rowspan="4">HIT2</td><td rowspan="4">Define the Way for ALU Calculation Results:
MRange 1: HIT1 - HIT2
MRange 2: HIT2 - HIT1</td><td rowspan="8">MRange1:
0 = Start
1 = 1. Stop Ch1
2 = 2. Stop Ch1
3 = 3. Stop Ch1
4 = 4. Stop Ch1
5 = No Action
6 = Cal1 Ch1
7 = Cal2 Ch1
9 = 1. Stop Ch2
A = 2. Stop Ch2
B = 3. Stop Ch2
C = 4. Stop Ch2</td><td rowspan="4">MRange 2:
2 = 1. Stop Ch1
3 = 2. Stop Ch1
4 = 3. Stop Ch1</td></tr>
<tr><td>22</td><td>1</td></tr>
<tr><td>21</td><td>0</td></tr>
<tr><td>20</td><td>1</td></tr>
<tr><td>19</td><td>0</td><td rowspan="4">HIT1</td><td rowspan="4">Define the Way for ALU Calculation Results:
MRange 1: HIT1 - HIT2
MRange 2: HIT2 - HIT1</td><td rowspan="4">MRange 2:
1 = Start</td></tr>
<tr><td>18</td><td>1</td></tr>
<tr><td>17</td><td>0</td></tr>
<tr><td>16</td><td>1</td></tr>
<tr><td>15</td><td>0</td><td>EN_FAST_INIT</td><td>Enable Fast Initialization</td><td colspan="2">0 = Disabled
1 = Enabled</td></tr>
<tr><td>14</td><td>1</td><td></td><td>Keep the Default Value</td><td colspan="2"></td></tr>
<tr><td>13</td><td>0</td><td rowspan="3">HITIN2</td><td rowspan="3">Number of Expected Pulses on Stop Channel 2</td><td colspan="2" rowspan="6">0 = Stop Channel Disabled
1 = 1 Pulse
2 = 2 Pulses
3 = 3 Pulses
4 = 4 Pulses
5 to 7 = Not Permitted</td></tr>
<tr><td>12</td><td>0</td></tr>
<tr><td>11</td><td>0</td></tr>
<tr><td>10</td><td>0</td><td rowspan="3">HITIN1</td><td rowspan="3">Number of Expected Pulses on Stop Channel 1</td></tr>
<tr><td>9</td><td>0</td></tr>
<tr><td>8</td><td>0</td></tr>
</table>

Bits	Def	Parameter	Description	Setting
7	0	n.c.	Keep the Default Values	
6	0			
5	0			
4	0			
3	0			
2	0			
1	0			
0	0			

Register 2 (REG2, Address: 0x82)

Bits	Def	Parameter	Description	Setting
23	0	EN_INT[2:0]	Activate Different Interrupt Sources Wired by OR, Another Bit in the Register 6	Bit 23 = 1: Timeout Interrupt Trigger Bit
22	0			Bit 22 = 1: End Hits Interrupt Trigger Bit
21	1			Bit 21 = 1: ALU Interrupt Trigger Bit
20	0	RFEDGE2	Channel 2 Edge Sensitivity	0 = Rising or Falling Edge
19	0	RFEDGE1	Channel 1 Edge Sensitivity	1 = Rising and Falling Edge
18-0	0	DELVAL1	Delay for Stop Enable Pulse, Start Timing from the First Pulse of Start Channel, 14 Integer and 5 Fractional Digits in Multiples of Tref	DELVAL1 = 0 to 16383.96875

Register 3 (REG3, Address: 0x83)

Bits	Def	Parameter	Description	Setting
23	0	n.c.	Keep the Default Value	
22	0			
21	0	EN_ERR_VAL	Timeout Forces ALU to Write 0xFFFFFFFF into the Output Register	0 = Disabled 1 = Enabled
20	1	SEL_TIMO_MB2	Select Time Limit for Timeout in Measurement Range 2	0 = 64 µs 1 = 256 µs 2 = 1024 µs 3 = 4096 µs @ 4 MHz ClkHS
19	1			
18-0	0	DELVAL2	Delay for Stop Enable Pulse, Start Timing from the First Pulse of Start Channel, 14 Integer and 5 Fractional Digits in Multiples of Tref	DELVAL2 = 0 to 16383.96875

Register 4 (REG4, Address: 0x84)

Bits	Def	Parameter	Description	Setting
23-20	2	n.c.	Keep the Default Value	
19	0	n.c.	Keep the Default Value	
18-0	0	DELVAL3	Delay for Stop Enable Pulse, Start Timing from the First Pulse of Start Channel, 14 Integer and 5 Fractional Digits in Multiples of Tref	DELVAL3 = 0 to 16383.96875

Register 5 (REG5, Address: 0x85)

Bits	Def	Parameter	Description	Setting
23	0	n.c.	Keep the Default Value	
22	0			
21	0			
20	0	EN_STARTNOISE	Noise unit must be disabled. This bit must set 0.	1 = Noise Unit Enabled 0 = Noise Unit Disabled
19	0	DIS_PHASENOISE	Noise unit must be disabled.	1 = Phase Shift Unit Disabled
18-0	0	n.c.	Keep the Default Value	

4.2 Opcode

MSB							LSB	Description
1	0	0	0	0	ADR2	ADR1	ADR0	Write Data into Address ADR Register
1	0	1	1	0	ADR2	ADR1	ADR0	Read Data from Address ADR Register
0	1	1	1	0	0	0	0	Init
0	1	0	1	0	0	0	0	Power On Reset
0	0	0	0	0	0	0	1	Start_Cycle
0	0	0	0	0	0	1	1	Start_Cal_Resonator
0	0	0	0	0	1	0	0	Start_Cal_TDC

The transition starts from the highest bit (MSB)and finished with the lowest bit (LSB). After sending the last bit, the MS1002 transfers data into the specified registers or execute orders. It is impossible to write continuously. Each register must be addressed separately.

It is necessary to send the opcode firstly when reading data from the chip. At the first clock rising edge after sending the opcode, the MS1002 sends the MSB of specified address register to SO output. Each rising edge transfers next lower bit to the output.

4.3 Result Register

<table>
<tr><th>Add</th><th>Symbol</th><th>Bits</th><th colspan="8">Description</th></tr>
<tr><td>0</td><td>RES_0</td><td>32</td><td colspan="8">Measurement Result 1, Fixed Floating-point Number, 16 Integer and 16 Fractional Digits (2^{15}-2^{0},2^{-1}-2^{-16})</td></tr>
<tr><td>1</td><td>RES_1</td><td>32</td><td colspan="8">Measurement Result 2, Fixed Floating-point Number, 16 Integer and 16 Fractional Digits</td></tr>
<tr><td>2</td><td>RES_2</td><td>32</td><td colspan="8">Measurement Result 3, Fixed Floating-point Number, 16 Integer and 16 Fractional Digits</td></tr>
<tr><td>3</td><td>RES_3</td><td>32</td><td colspan="8">Measurement Result 4, Fixed Floating-point Number, 16 Integer and 16 Fractional Digits</td></tr>
<tr><td>4</td><td>STAT</td><td>16</td><td>15-13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8-6</td><td>5-3</td><td>2-0</td></tr>
<tr><td></td><td></td><td></td><td>No Meaning</td><td>No Meaning</td><td>No Meaning</td><td>Precounter Timeout</td><td>TDC Timeout</td><td>Number of Hits on Ch2</td><td>Number of Hits on Ch1</td><td>Result Register Pointer</td></tr>
<tr><td>5</td><td>REG_1</td><td>8</td><td colspan="8">Indicate the Highest 8 Bits of Write Register 1, Used for Testing Communication</td></tr>
</table>

The data structure and the distribution of result registers are determined by whether the operation modes and stored data are calibrated values.

The following points must be noted:

1. Negative values only in measurement range 1.
2. There are only positive values with unsigned number in measurement range 2.
3. Non-calibration measurement can only be carried out in measurement range 1.

When calibrated measurement is adopted in measurement range 1, the measured time interval should not exceed two calibrated clock cycles. If the measured time interval is bigger than two calibrated clock cycles, then ALU will overflow and write 0xFFFFFFFF into relevant result register.

a. Measurement Range 1, for Calibration (Calibrate = 1)

The measurement results are multiples of internal reference clock cycles. Internal reference clock is equal to external reference clock divided by DIV_CLKHS (DIV_CLKHS＝1,2,4). The calibration value is the 32-bit fixed-point number with 16 integer and 16 fractional digits. So a calibration value covers a result register. Serial output starts from the highest bit (2^{15}) and finishes with the lowest bit (2^{-16}). Data are in form of complements of 2.

Time = RES_X × Tref × 2ClkHSDiv = RES_X × Tref × N, with N = 1, 2 or 4

Time < 2 × Tref × 2ClkHSDiv

b． Measurement Range 1, Not for Calibration (Calibrate = 0)

Non-calibration values are the typical signed integers, which are stored as the 16-bit values in the high WORD unit of the result registers. The low WORD unit of the result registers are set to 0. The results represent the number of LSB, which are in form of complements of 2.

Time = RES_X × LSB = RES_X × 70 ps

c． Measurement Range 2

In measurement range 2, the MS1002 only supports calibration measurement. The measurement results are multiples of internal reference clock cycles. Internal reference clock is equal to external reference clock divided by DIV_CLKHS (DIV_CLKHS＝1,2,4). The calibration value is the 32-bit fixed-point number with 16 integer and 16 fractional digits. So a calibration value covers a result register. Serial output starts from the highest bit (2^{15}) and finishes with the lowest bit (2^{-16}). Data are in form of complements of 2.

Time = RES_X × Tref × 2ClkSDiv = RES_X × Tref × N, with N = 1, 2 or 4

4.4 Status Register

The MS1002 provides a 16-bit status register.

Bits	Name	Description	Value
10	Timeout Precounter	Indicate an Overflow of the 14-bit Precounter in Measurement Range 2	1 = Overflow
9	Timeout TDC	Indicate an Overflow of TDC	1 = Overflow
6-8	# of hits Ch 2	Indicate Number of Hits on Channel 2	
3-5	# of Hits Ch 1	Indicate Number of Hits on Channel 1	
0-2	Pointer Result-Register	Pointer to the Next Free Result Register Address	

5. Measurement Range 1

5.1 Description

a. Two Stop channels share a Start channel.

b. Minimum Resolution Rate:70ps

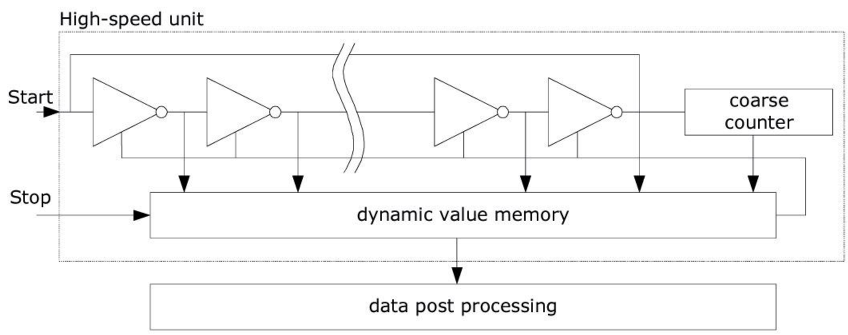
c. The Resolution of Interval Pulse Pair: 15ns

d. 4 Samplings for Each Stop Channel

e. Measurement Range: 2.0 ns -- 1.8 µs

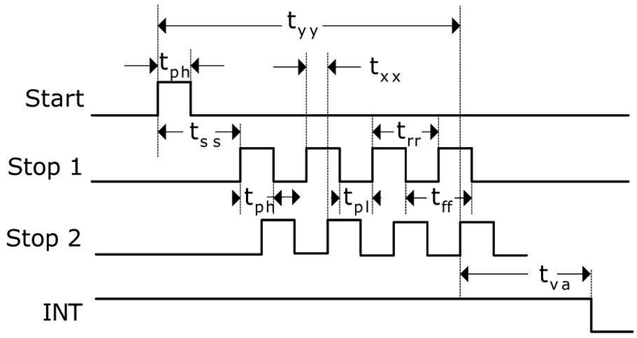
f. Each channel can be triggered by selecting rising/falling edge.

Digital TDC performs high-precision time interval measurement using propagation delays of signals through internal gate circuit. The following figure shows the main structure of measuring absolute-time TDC. The intelligent circuit structure and the special layout methods on the chip make it record the number of signals passing through the gate circuit precisely. The highest measurement precision that the chip can achieve is mainly determined by the shortest propagation delay.



The measurement unit is triggered by Start signal and stopped by receiving Stop signal. The time interval between Start signal and Stop signal can be calculated by the position of ring oscillator and the values of coarse counter. The measurement range is 20 bits.

At 3.3V and 25°C, the minimum resolution rate of the MS1002 is 70ps. RMS noise is about 50ps (0.7LSB). Temperature and voltage have great effect on the propagation delay time of the gate circuit. Usually, the error caused by temperature and voltage is compensated by calibration. During calibration, TDC measures 1 and 2 calibration clock cycles. The measurement range is limited by the size of the counter: tyy = BIN × 26224 ≈ 1.8 µs.

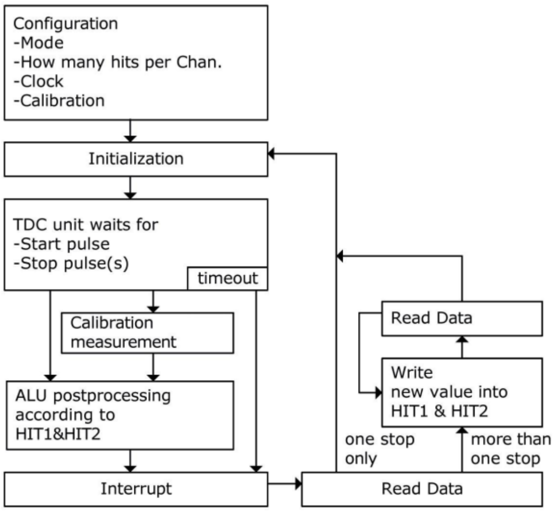


Symbol	Time	Description
tph	2.5 ns (min.)	Minimum Pulse Width
tpl	2.5 ns (min.)	Minimum Pulse Width
tss	3.5 ns ns (min) 1.8 µs (max.)	Start to Stop
trr	15 ns (typ.)	Rising Edge to Rising Edge
tff	15 ns (typ.)	
tva	Non-calibration: 560 ns Calibration: 4.6 µs	Time from the Last Pulse to Measurement Data Valid
txx	No Time Limit	
tyy	1.8 µs (max)	Maximum Measurement Range

Each input terminal can be set to be triggered to rising or/and falling edge separately. Trigger edges can be set through bit0-bit2 (NEG_START, NEG_STOP1, NEG_STOP2) of REG0 and bit19-bit20 (REFDGEx) of REG2.

5.2 Test Flow Chart

5.2.1 Flow Graphic



5.2.2 Setting

The MS1002 must be set before using it.

The main setting of measurement range 1:

a. Selecting Measurement Range 1: Setting Bit3 of REG0, MRange2 = 0.

b. Selecting Reference Clock

The bits10-bit11 of REG0 and START_CLKHS are used to switch high-speed clock.

The bits12-bit13 of REG0 and ClkHSDiv are used to set internal divider values (1, 2 or 4) of reference clock, which is very important for calibration measurement in measurement range 1. Because only when 2×Tref (internal clock) is larger than measured maximum time interval, ALU can operate normally. Otherwise, ALU output is 0xFFFFFFFF.

It also ensured that 2×Tref (internal clock) is less than 1.8μs to avoid timeout during calibration.

c. Setting the Number of Needed Hits

Users can set the number of hits that the MS1002 should measure in REG1, bits8-bit10(HITIN1) and bit11-bit13(HITIN2). Each channel can perform up to 4 measurements. The MS1002 measures until finishing the number of setting hits or occurring a timeout.

d. Calibration Selection

As the measurement resolution rate changes with temperature and voltage, the MS1002 ALU can calibrate the results internally. Setting Bit5(Calibrate) of REG0 to ”1” for calibration measurement, which is recommended.

For calibration, TDC measures 1 and 2 reference clock cycles. The two data are stored as Cal1 and Cal2.

There are two ways to update the calibration data: Cal1 and Cal2

◆ Sending Start_Cal_TDC via SPI interface to calibrate separately;

◆ Setting bit4(DisAutoCal) of REG0 to 1 to update automatically. Automatic updates are preferred in most applications.

e. Define ALU Data Processing

While each channel of TDC unit can perform up to 4 measurements, users can freely define which time interval between two signals ALU calculates, which can be set by bit16-bit19(HIT1) and bit20-bit23(HIT2) of REG1. The specific settings are:

1 = 1st Stop Ch1; 2 = 2nd Stop Ch1; 3 = 3rd Stop Ch1; 4 = 4th Stop Ch1;
9 = 1st Stop Ch2; A = 2nd Stop Ch2; B = 3rd Stop Ch2; C = 4th Stop Ch2;
0 = Start; 6 = Cal1 Ch1; 7 = Cal2 Ch1;

ALU Calculation Formula: Hit1 - Hit2.

For Example:

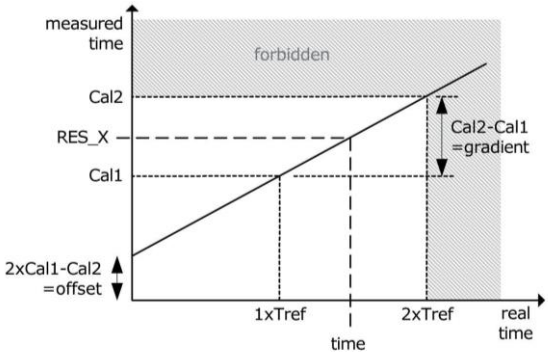
REG1 = 0x01xxxx ≡ 1st Stop Ch1 - Start
REG1 = 0x23xxxx ≡ 3rd Stop Ch2 - 2nd Stop Ch1
REG1 = 0x06xxxx ≡ Cal1

If calibration is adopted, then ALU will perform the full calibration calculation(except when reading the calibration values, ALU writes Cal1/Cal2 raw data into output register).

$$RES\_X=\frac{HIT1-HIT2}{Cal2-Cal1}$$

Cal2-Cal1 = gradient

Time = RES_X × Tref × 2ClkHSDiv = RES_X × Tref × N, N = 1, 2 or 4.



f. Selecting Input Trigger Method

By setting bit19-bit20(REFDGE1&FEDGE2) of REG2, users can select whether STOP inputs are triggered to rising edge/falling edge (RFEDGE=0) or to both rising and falling edges (RFEDGE=1). Users can set bit0-bit2(NEG_X) of REG0 to add an internal inverter to each input terminal (Start, Stop1 and Stop2). When RFEDGE = 0, rising edge will be triggered by NEG_X=0, falling edge will be triggered by NEG_X=1.

g. Interrupt

Interrupt pins (PIN8, INT) have different interrupt sources, which can be chosen from bits21-bit23(EN_INT) of REG2.

EN_INT = 0 No Interrupt Source
1 ALU Idle
2 the Reached Pre-set Number of Samples
4 Overflow of TDC Unit

If two or more interrupt sources are needed, OR can connect different options.

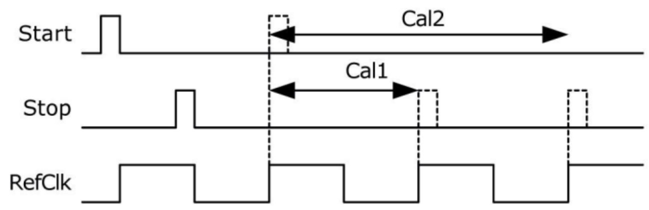
This setting will be further described later in this chapter. After setting, the users must send opcode "Init" to initialize the MS1002 to make TDC accept Start and Stop signals.

5.2.3 Measurement

After an initialization, TDC high-speed measurement unit operates after receiving Start pulse. It will not stop until reaching the set number of samples (maximum 4 on both channels in measurement range 1) or occurring an overflow (about 1.8μs in measurement range).

The time measurement raw data are stored in TDC. The bits3-bit8 of status register can show the number of samples.

If calibration is performed, TDC will measure 1 and 2 internal reference clock cycles (Tref /1, 2 or 4) after measuring the time interval. Calibration raw data (Cal1 and Cal2) are also stored in TDC.



5.2.4 Data Processing

At the end of measurement, ALU start to process data according to the setting of HIT1 and HIT2 and send the results to output register. Without calibration, ALU transfers 16-bit raw data to output register. With calibration, then ALU calculates according to the register setting and transfers 32-bit fixed floating-point number to output register.

Setting HIT1=HIT2=5 and switching off ALU.

The time ALU takes is determined by whether calibration is performed or not and the power supply.

	Non-calibration	Calibration
3.3V	220ns	1.8μs
2.5V	310ns	2.5μs
2.0V	580ns	4.6μs

Assumed that choosing ALU idle as the interrupt source (setting in REG2 and EN_INT). As long as there are readable data in the result register, the interrupt flag will be set, then the load pointer of the output register is increased by 1 and points to the next stored unit. The bit0-bit2 of status register can show the factual position of the load pointer.

5.2.5 Reading Data

Now the user can read data by sending the opcode 10110ADR. Continuing with 16 cycles(non-calibration data) or 32 cycles(calibration data), the MS1002 outputs from the highest valid bit.

a. Non-calibration Data Format:

Non-calibration data are the 16-bit signed integer in complements of 2.

1 BIN = uncalibrated gate delay time ≈ 70ps

Time = RES_X × 70ps

b. Calibration Data Format:

Calibration data are the 32-bit fixed floating-point number in complements of 2 and multiples of the reference clock:

Time = RES_X × Tref × N, N = 1, 2 or 4

The measured time interval can not exceed 2 × Tref × ClkHSDiv, or ALU will overflow and write 0xFFFFFFFF to output register.

ALU only allows one sampling calculation at a time. If there is more than one sampling, it is necessary to write new orders to HIT1/HIT2 to instruct ALU to calculate other samples. After writing an order to HIT1/HIT2, no further read or write operations can be performed to HIT1/HIT2 within 4.6µs (calibration value)or 580ns(non-calibration value)

For example:

```
configuration
...
write reg1=0x104400   '4 hits on channel 1, calculate
Hit1-Start
...
Initialize
...
While (Check interrupt flag)
write reg1=0x204400   calculate Hit2-Start
wait(4.6µs)
write reg1=0x304400   calculate Hit3-Start
wait(4.6µs)
write reg1=0x404400   calculate Hit4-Start
wait(4.6µs)
```

Now, all the sampling data are stored in register 0 to 3, the load pointer now points to register address 4.

At last, the MS1002 must send opcode “Init” to initialize again before the next measurement is performed to make TDC receive new Start and Stop signals.

6. Measurement Range 2

6.1 Description

a. Only a Stop Channel corresponding to Start Channel

b. Typical Resolution Rate: 50ps RMS

c. The Resolution Rate of Interval Pulse Pair: 2 × Tref

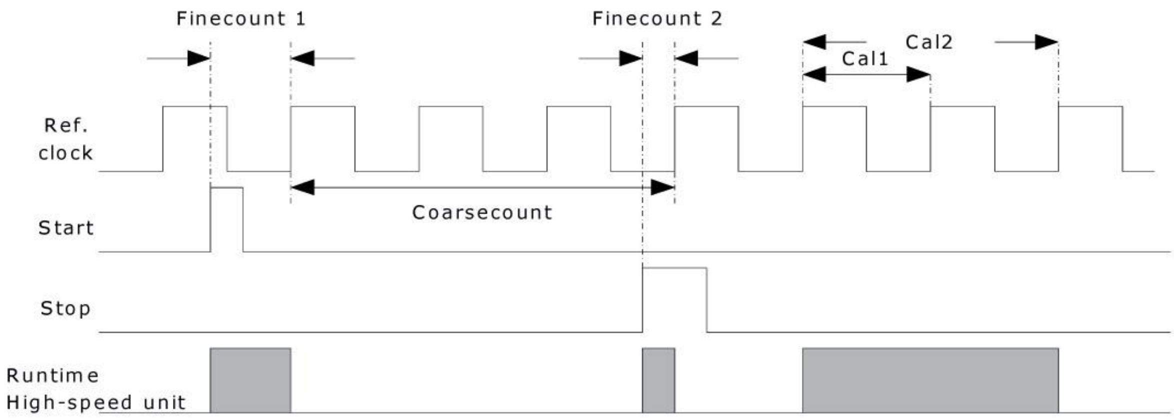
d. 3 Sampling Abilities

e. Measurement Range: 2 × Tref ~ 4ms@4MHz

f. Selectable Trigger to Rising/Falling Edge

g. Adjustable Window with 10ns Precision for Each Stop Signal Providing Accurate Stop Enabling

Digital TDC performs high-precision intervals using propagation delays of signals through internal gate circuit. (It can be seen in part five: measurement range 1). In measurement range 2, a pre-divider is used to extend the measured maximum interval. The resolution rate remains unchanged. In this mode, the high-speed unit of TDC do not measure the whole-time interval. It only measures the interval from START or STOP to the next rising edge of reference clock(fine-counts). Between two precise measurements, TDC counts reference clock cycles (coarse-count).



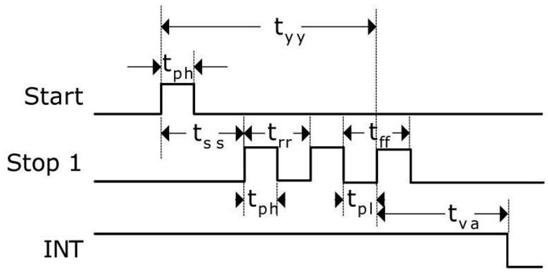
time = Tref x (Cc + (Fc1 - Fc2)/(Cal2 - Cal1)

At 3.3V and 25°C, the minimum resolution rate of the MS1002 is 70ps. RMS noise is about 50ps (0.7LSB). Temperature and voltage have great effect on the propagation delay time of the gate circuit. In measurement range 2, measurement results are the sum of precise and coarse measurement values. So it is necessary to calibrate in measurement range 2. During calibration, TDC measures 1 and 2 calibration clock cycles separately.

The measurement range is limited by the size of the counter: tyy = Tref $\times 2^{14}$= 4ms @ 4MHz

The interval between Start and Stop is calculated with a 26-bit measurement range.

	Time (Condition)	Description
tph	2.5 ns (min.)	Minimum Pulse Width
tpl	2.5 ns (min.)	Minimum Pulse Width
tss	2 × Tref	Start to Stop @ Dis_Phasenoise=1
tss	12 × Tref	Start to Stop @ Dis_Phasenoise=0
trr	2 × Tref	Rising Edge to Rising Edge
tff	2 × Tref	Falling Edge to Falling Edge
tva	4.6μs(max)	ALU Start to Data Valid
tyy	4ms (max) @ 4MHz	Maximum Measurement Range= 2^{14} × Tref

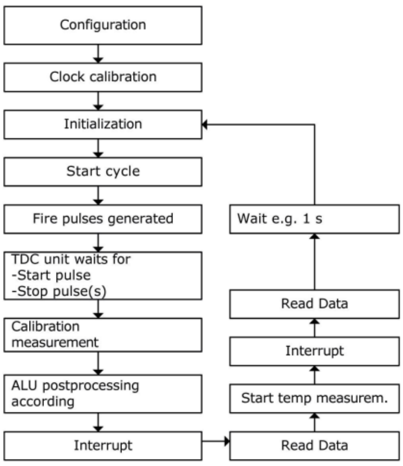


In Input circuit, each input terminal can be set to trigger to rising edge or falling edge. Selecting trigger edge by setting bit0-bit1 (NEG_START, NEG_STOP1) of REG0. Furthermore, all of START/STOP input terminals can be activated in high level.

Note: If interval between Start and Stop is less than minimum time limit tss, then TDC will ignore all the interval pulses less than tss.

6.2 Test Flow Chart

6.2.1 Flow Graphic



6.2.2 Setting

The MS1002 must be set before using it.

The main setting of measurement range 2:

a. Selecting Measurement Range 2: Setting Bit3 of REG0, MRange2 = 1.

b. Selecting Reference Clock:

The MS1002 in measurement range 2 needs a high-speed clock to perform Time interval measurement.

Setting Bit6 of REG0, When SelClkT=1, Selecting high-speed clock

Bit10-bit11 of REG0 and START_CLKHS are used to switch high-speed clock.

Bit12-bit13 of REG0 and ClkHSDiv are used to set internal divider values (1, 2 or 4). The selection has great effect on minimum time interval and maximum time interval.

Minimum Time Interval: $t_{min} = 2 \times T_{ref} \times 2^{ClkHSDiv}$

Maximum Time Interval: $t_{max} = 2^{14} \times T_{ref} \times 2^{ClkHSDiv}$

It must ensure that $2 \times T_{ref} \times 2^{ClkHSDiv}$ is less than 1.8μs. Otherwise ALU will overflow and output data 0xFFFFFFFF when in calibration.

c. Setting the Number of Needed Hits

Users can set the number of hits that the MS1002 measures in REG0 and bit8-bit10(HITIN1). In measurement range 2, channel 1 can perform up to 3 measurements. Because Start is also counted as a hit, the HITIN1 value is always one more than the set number of samples. The MS1002 measures until reaching the number of pre-set number of hits or occurring an overflow. REG0 and bit11-bit13(HITIN2) must be set to 0.

d. Calibration Selection

Calibration measurement is selected by setting bit5(Calibrate) of REG0 to 1. Calibration must be performed in measurement range 2.

TDC measures 1 and 2 reference clock cycles separately for calibration. These two data are stored as Cal1 and Cal2.

There are two ways to update calibration value Cal1 and Cal2：

◆Sending Start_Cal_TDC order via SPI interface to calibrate specially;

◆Setting bit4 (DisAutoCal)=1 of REG0 to update automatically. Automatic updates are preferred in most applications.

e. Define ALU Data Processing

Although TDC unit can measures 3 samples, ALU can only calculate one sample every time. Users can define which time interval between two pulses ALU measures, which can be set by bit16-bit19 (HIT1) of REG1 and bit20-bit23(HIT2). Because of the special measurement method in measurement range 2, Start pulse is processed as Stop pulse in TDC.

Reg1 = 0x21xxxx ≡ 1st Stop Ch1-Start

Reg1 = 0x31xxxx ≡ 2nd Stop Ch1-Start

Reg1 = 0x41xxxx ≡ 3rd Stop Ch1-Start

ALU calculates the time interval according to the following formula:

$$RES\_X = CoarseCount + \frac{(HIT1-HIT2)}{Cal2-Cal1}$$

$Time = RES\_X \times T_{ref} \times 2^{ClkHSDiv}$

f. Select Input Trigger Method

By setting bit19-bit20(REFDGE1 & FEDGE2) of REG2, users can select whether STOP inputs are triggered to rising edge/falling edge (RFEDGE=0) or to both rising and falling edges (RFEDGE=1). Users can set bit0-bit2(NEG_X) of REG0 to add an internal inverter to each input terminal (Start, Stop1 and Stop2). When RFEDGE = 0, rising edge will be triggered by NEG_X=0, falling edge will be triggered by NEG_X=1.

g. Interrupt

Interrupt pins (PIN8, INT) have different interrupt sources, which can be chosen from bits21-bit23(EN_INT) of REG2.

EN_INT= 0 No Interrupt Source
1 ALU Idle
2 the Reached Pre-set Number of Samples
3 Overflow of TDC Unit

OR can connect different options. This setting will be further described later in this chapter. After setting, the users must send opcode "Init" to initialize the MS1002 to make TDC accept Start and Stop signals.

6.2.3 Measurement

After initialization, TDC starts to operate from receiving the first pulse on Start channel until reaching the pre-set number of samples (maximum 3 samples on channel 1 in measurement range 2) or stopping operating when occurring the measurement overflow. The overflow time can be limited by setting bit19-bit20 (SEL_TIMO_MR2) of REG3 to select different reference clocks.

At 4MHz, the corresponding values are as follows:

SEL_TIMO_MR2 (@ 4 MHz, ClkHSDiv = 0)

= 0 = 64 µs

= 1 = 256 µs

= 2 = 1024 µs

= 3 = 4096 µs

At the end of time measurement, TDC measures two reference clock cycles for calibration.

6.2.4 Data Processing

At the end of measurement, ALU starts to process data according to the setting of HIT1 and HIT2 and send the result to output register. ALU calculates and transfers 32-bit fixed floating-point number to output register. Setting HIT1=HIT2=5, switching off ALU.

The time ALU takes is determined by the power supply:

3.3V	1.8µs
2.5V	2.5µs
2.0V	4.6µs

Assumed that choosing ALU idle as the interrupt source (setting in REG2 and EN_INT). As long as there are readable data in the result register, the interrupt flag will be set, then the load pointer of the output register is increased by 1 and points to the next stored unit. The bit0-bit2 of status register can show the factual position of the load pointer.

6.2.5 Reading Data

Now the users can read data by sending the opcode 10110ADR. Continuing with 32 cycles (calibration data), the MS1002 outputs from the highest valid bit.

32-bit fixed floating-point number in complements of 2 represents the time interval in reference clock cycles as the minimum unit.

$$Time=RES\_X \times T_{ref} \times 2^{ClkHSDiv}$$

ALU only allows one sample calculation every time. If more than one sample need to be measured, it is necessary to write new orders to HIT1/HIT2 to instruct ALU to calculate other samples. After writing an order to HIT1/HIT2, no further read or write operations can be performed to HIT1/HIT2 within 4.6μs (calibration value)

For example:

configuration

...

write reg1=0x214400 '3 hits on channel 1, calculate

Hit1-Start

...

Initialize

...

While (Check interrupt flag)

write reg1=0x314400 calculate Hit2-Start

wait(4.6μs)

write reg1=0x414400 calculate Hit3-Start

wait(4.6μs)

All sampling data are stored in output register 0 to 2, the load pointer now points to register address 3.

At last, the MS1002 must send opcode “Init” to initialize again to make TDC receive new Start and Stop signals.

6.3 Stop Masking

If any samplings can not be accepted, the MS1002 can set time-based masking windows to mask any one of 3 hits. The masking windows start from START signal, its precision is less than 10ns.

Internal enable unit is connected with external enable pins by the logic “AND”. When using the internal masking unit, the external enable pin must be set to 1. It can be set in DELVAL1, DELVAL2 and DELVAL3 of REG2-REG4:

◆DELVAL1 … DELVAL3 are the fixed floating-point numbers consisting of 14-bit integer and 5-bit fractional digits, in multiples of internal reference clock cycles.

Delaymin ＝DELVALX × Tref × ClkDivHS

◆The shortest masking time is 3 clock cycles.

◆Masking values must be in ascending order. Every masking values must be 3 clock cycles greater than the previous value.

◆If not all the registers are used, unneeded masking values must be set to 0.

For Example:

4 MHz Reference, ClkHSDiv = 1

DELVAL1 = ' h3200 The first pulse can be accepted 200 µs after start

(128000/32 × 250ns × 21 = 200 µs)

DELVAL2 = ' h3300 The second pulse can be accepted 204 µs after start

(13056/32 × 250ns × 21= 204 µs)

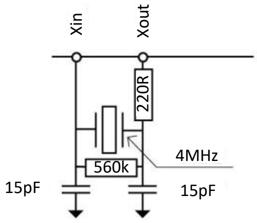
DELVAL1 = ' h3400 The third pulse can be accepted 208 µs after start

(13312/32 × 250ns × 21= 208 µs)

7. Special Function and Description

7.1 High-speed Oscillator

Usually, the MS1002 needs a 2MHz-8MHz high-speed clock for calibration. In measurement range 2, the MS1002 needs high-speed clock signal as a part of time measurement unit.



The average current when the oscillator is operating contiguously is 260µA.

Because oscillator is needed only in time measurement, the MS1002 can control the start time of oscillator automatically. In measurement, when TDC receives INIT opcode, it will be switched on high-speed clock automatically. It needs to be considered the delay resulted from oscillator processing time. It can be set in bit10-bit11(START_CLKHS) of REG0:

START_CLKHS = 0 Oscillator off

= 1 Oscillator on

= 2 The measurement is started with 640 µs delay

= 3 The measurement is started with 1280 µs delay

The delay time can be selected from 640 µs and 1280 µs, which can guarantee that the oscillator is ready before measurement is started. For ceramic oscillator, 640 µs is sufficient.

With this measurement method, average current consumption can be significantly reduced.

7.2 SPI Interface

Serial interface is compatible with 4-wire SPI interface. It needs SerialSelectNot (SSN) and can not be operated as 3-wire interface.

SSN Slave Selection

SCK - SPI Clock

SI - SPI Data Input

SO - SPI Data Output

MS1002 only supports the following SPI mode:

Clock Phase Bit =1

Clock Polarity Bit =0

Time limit is shown in the previous write timing and read timing. SSN needs to be set in high level. SSN should keep in high level for at least 50ns between each read/write sequence.

When resetting, SSN wire (SerialSelectNot) is high-level valid serial interface reset circuit. When SSN is in low level, different operations can be addressed, not depending on the status of interface before the reset.

7.3 Fast Initialization

In measurement 1, the MS1002 provides the fast initialization ability. Setting bit22 of REG3 (EN_FAST_INIT)= 1, the interrupt flag can initialize TDC automatically. So when reading out data, TDC is ready for the next measurement. This mode is only available in high-speed applications, which is very suitable for non-calibration with only one stop signal.

TYPICAL APPLICATIONS

With the development and improvement of laser ranging technology, it has been applied to electricity, water conservancy, communication, environment, architecture, geology, policing, firefighting, blasting, navigation, railway, counter-terrorism/military, agriculture, forestry, real-estate, leisure/outdoor activities and artificial intelligence. The MS1002 is suitable for pulse laser ranging known as laser time of flight ranging (TOF).

The features are as follows:

- High Measurement Precision

The minimum resolution rate of the MS1002 is 70ps, the precision in laser ranging applications is about 1cm.

- Far Measurement Distance

The MS1002 has two measurement. Measurement range 1 is from 0 to 270m, measurement range 2 is from 75m to 60 km.

- Fast Measurement Speed

The SPI communication frequency of the MS1002 is up to 40MHz and embedded with high-speed TDC and ALU, so its measurement speed is very fast. And it is suitable for radar scanning.

- High Measurement Stability

The MS1002 is embedded with noise suppression unit and clock automatic calibration unit, which have effect on laser ranging stability.

- Low Measurement Power Dissipation

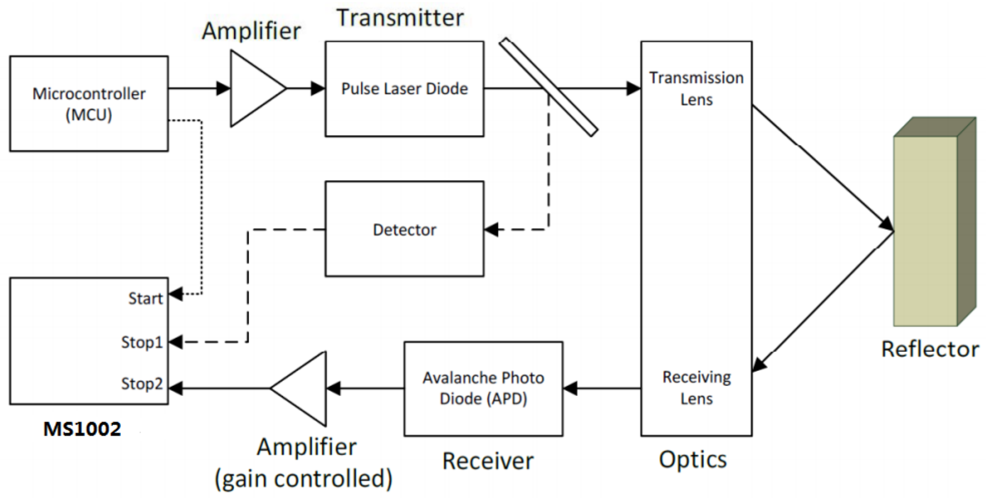
The MS1002 has two modes: operating mode and sleep mode. Operating mode current is about 250μA, sleep mode current is about 1μA, which is suitable for battery powered ranging products.

Typical Application

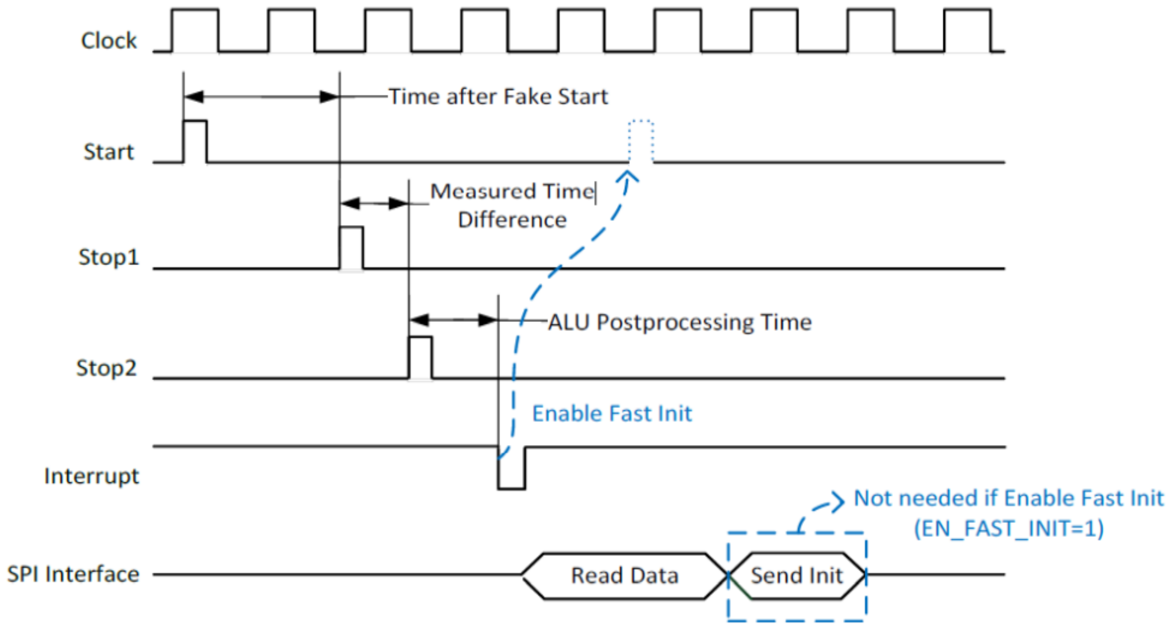
In laser ranging applications, the MS1002 can achieve three modes: short-distance non-calibration measurement, short-distance calibration measurement and far-distance calibration measurement. These three modes are described below:

a. Short-distance Non-calibration Measurement:

Short-distance non-calibration measurement is realized using a ring oscillator in measurement range 1. The measurement value is only relevant to TDC gate delay. Its advantages are fast measurement speed and dual-channel sampling. And disadvantages are that gate delay is affected by voltage and temperature, so the ability is relatively poor.



Short-distance Measurement Diagram



Short-distance Non-calibration Measurement Timing Diagram

Short-distance Non-calibration Measurement Register Configuration
REG0-REG2

Bits	REG0	Setting	REG1	Setting	REG2	Setting
23	n.c.	0	HIT2	0	EN_INT	0
22		0		0		1
21		0		0		1
20		0		0	RFEDGE2	0

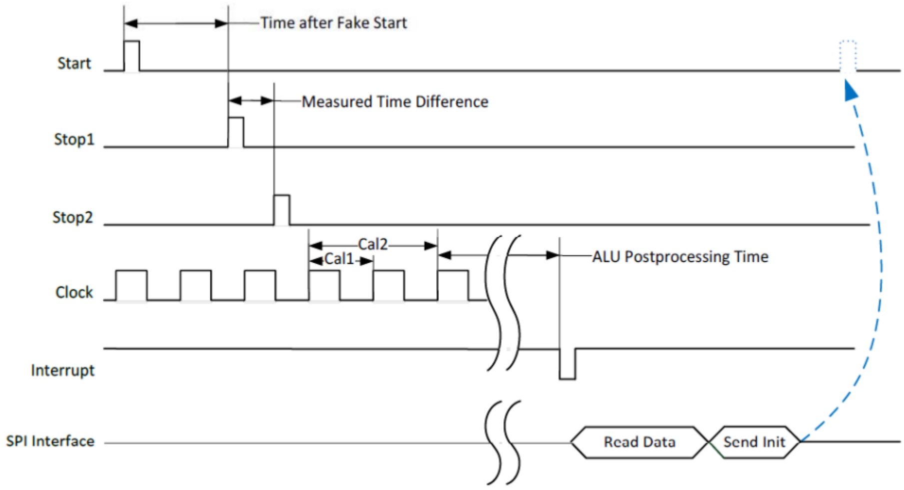
Bits	REG0	Setting	REG1	Setting	REG2	Setting
19	n.c.	0	HIT1	0	RFEDGE1	0
18		0		0	DELVAL1	0
17		0		0		0
16		0		1		0
15	n.c.	0	EN_FAST_INIT	0		0
14		0	s.c.	1		0
13	ClkHSDiv	0	HITIN2	0		0
12		0		0		0
11	START_ClkHS	0		0		0
10		1	HITIN1	0		0
9	n.c.	0		0		0
8	n.c.	0		1		0
7	n.c.	0	n.c.	0		0
6	n.c.	0	n.c.	0		0
5	Calibrate	0	n.c.	0		0
4	DisAutoCal	1	n.c.	0		0
3	MRange2	0	n.c.	0		0
2	NEG_STOP2	0	n.c.	0		0
1	NEG_STOP1	0	n.c.	0		0
0	NEG_START	0	n.c.	0		0

REG3-REG5

Bit	REG3	Setting	REG4	Setting	REG5	Setting
23	s.c.	0	s.c.	0	n.c.	0
22	s.c.	0	s.c.	0		0
21	EN_ERR_VAL	1	s.c.	1		0
20	SEL_TIMO_MR2	0	s.c.	0	EN_STARTNoise	0
19		0	s.c.	0	DIS_PhaseNoise	0
18	DELVAL2	0	DELVAL3	0	n.c.	0
17		0		0		0
16		0		0		0
15		0		0	n.c.	0
14		0		0		0
13		0		0		0
12		0		0		0
11		0		0		0
10		0		0		0
9		0		0		0
8		0		0		0
7		0		0		0
6		0		0		0
5		0		0		0
4		0		0		0
3		0		0		0
2		0		0		0
1		0		0		0
0		0		0		0

b. Short-distance Calibration Measurement

Short-distance calibration measurement is realized using the ring oscillator and high-speed calibration clock in measurement range 1. Calculate TDC values using ALU to be related to the high-speed clock and store them in the result registers. Its advantages are high measurement stability and dual-channel sampling and disadvantages are that the speed is relatively lower than non-calibration due to calibration and calculation.



Short-distance Calibration Measurement Timing Diagram

Short-distance Calibration Measurement Register Configuration

REG0-REG2

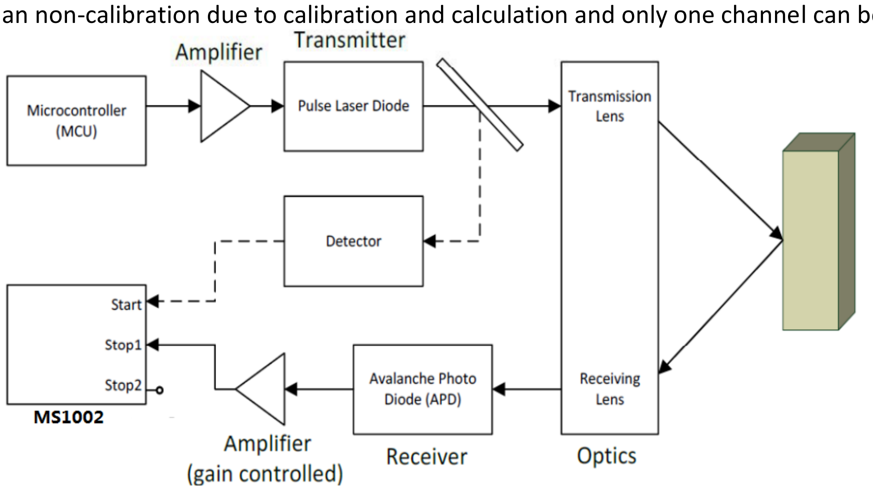
Bits	REG0	Setting	REG1	Setting	REG2	Setting
23	n.c.	0	HIT2	0	EN_INT	1
22		0		0		0
21		0		0		1
20		0		0	RFEDGE2	0
19	n.c.	0	HIT1	0	RFEDGE1	0
18		0		0	DELVAL1	0
17		0		0		0
16		0		1		0
15	n.c.	0	EN_FAST_INIT	0		0
14		0	s.c.	1		0
13	ClkHSDiv	0	HITIN2	0		0
12		0		0		0
11	START_ClkHS	0		0		0
10		1	HITIN1	0		0
9	n.c.	0		0		0
8	n.c.	0		1		0
7	n.c.	0	n.c.	0		0
6	n.c.	0	n.c.	0		0
5	Calibrate	1	n.c.	0		0
4	DisAutoCal	0	n.c.	0		0
3	MRange2	0	n.c.	0		0
2	NEG_STOP2	0	n.c.	0		0
1	NEG_STOP1	0	n.c.	0		0
0	NEG_START	0	n.c.	0		0

REG3-REG5

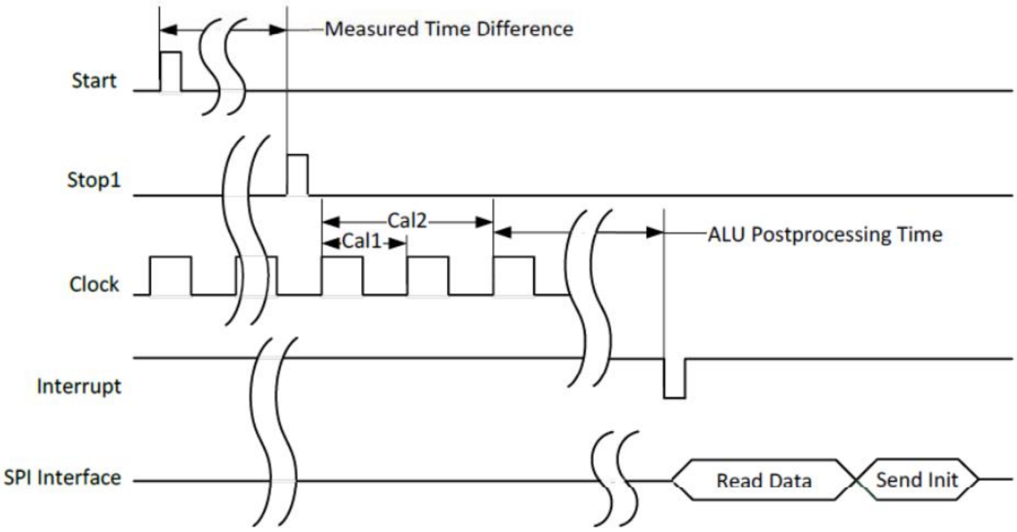
Bits	REG3	Setting	REG4	Setting	REG5	Setting
23	s.c.	0	s.c.	0	n.c.	0
22	s.c.	0	s.c.	0		0
21	EN_ERR_VAL	1	s.c.	1		0
20	SEL_TIMO_MR2	0	s.c.	0	EN_STARTNoise	0
19		0	s.c.	0	DIS_PhaseNoise	0
18	DELVAL2	0	DELVAL3	0	n.c.	0
17		0		0		0
16		0		0		0
15		0		0	n.c.	0
14		0		0		0
13		0		0		0
12		0		0		0
11		0		0		0
10		0		0		0
9		0		0		0
8		0		0		0
7		0		0		0
6		0		0		0
5		0		0		0
4		0		0		0
3		0		0		0
2		0		0		0
1		0		0		0
0		0		0		0

c. Far-distance Calibration Measurement

Far-distance calibration measurement is realized through measurement range 2. The measurement range 2 includes the precision counters and the coarse counters. The precision counters are realized through the ring oscillator and the high-speed calibration clock. The measurement results are stored in low 16 Bit of the result registers. The coarse counters are used to measure the number of frequency division clock cycles of the high-speed clock, whose measurement values are stored in high 16 Bit of the result registers. Its advantages are high measurement stability and far measurement distance. Its disadvantages are that the speed is lower than non-calibration due to calibration and calculation and only one channel can be sampled.



Far-distance Measurement Diagram



Far-distance Calibration Measurement Timing Diagram

Far-distance Calibration Measurement Register Configuration

REG0-REG2

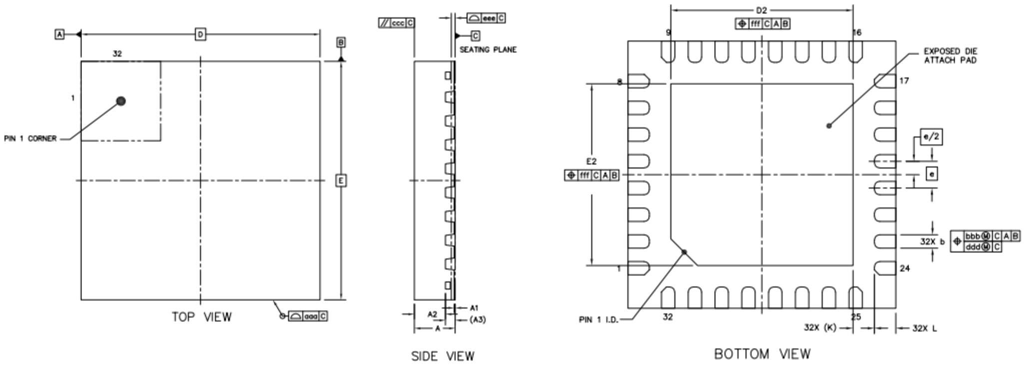
Bits	REG0	Setting	REG1	Setting	REG2	Setting
23		0		0		1
22	n.c.	0	HIT2	0	EN_INT	0
21		0		1		1
20		0		0	RFEDGE2	0
19		0		0	RFEDGE1	0
18	n.c.	0	HIT1	0		0
17		0		0		0
16		0		1		0
15	n.c.	0	EN_FAST_INIT	0		0
14		0	s.c.	1		0
13	ClkHSDiv	0		0		0
12		0	HITIN2	0		0
11	START_ClkHS	0		0		0
10		1		0		0
9	n.c.	0	HITIN1	1	DELVAL1	0
8	n.c.	0		0		0
7	n.c.	0	n.c.	0		0
6	n.c.	0	n.c.	0		0
5	Calibrate	1	n.c.	0		0
4	DisAutoCal	0	n.c.	0		0
3	MRange2	1	n.c.	0		0
2	NEG_STOP2	0	n.c.	0		0
1	NEG_STOP1	0	n.c.	0		0
0	NEG_START	0	n.c.	0		0

REG3-REG5

Bits	REG3	Setting	REG4	Setting	REG5	Setting
23	s.c.	0	s.c.	0	n.c.	0
22	s.c.	0	s.c.	0		0
21	EN_ERR_VAL	1	s.c.	1		0
20	SEL_TIMO_MR2	1	s.c.	0	EN_STARTNoise	0
19		1	s.c.	0	DIS_PhaseNoise	0
18	DELVAL2	0	DELVAL3	0	n.c.	0
17		0		0		0
16		0		0		0
15		0		0	n.c.	0
14		0		0		0
13		0		0		0
12		0		0		0
11		0		0		0
10		0		0		0
9		0		0		0
8		0		0		0
7		0		0		0
6		0		0		0
5		0		0		0
4		0		0		0
3		0		0		0
2		0		0		0
1		0		0		0
0		0		0		0

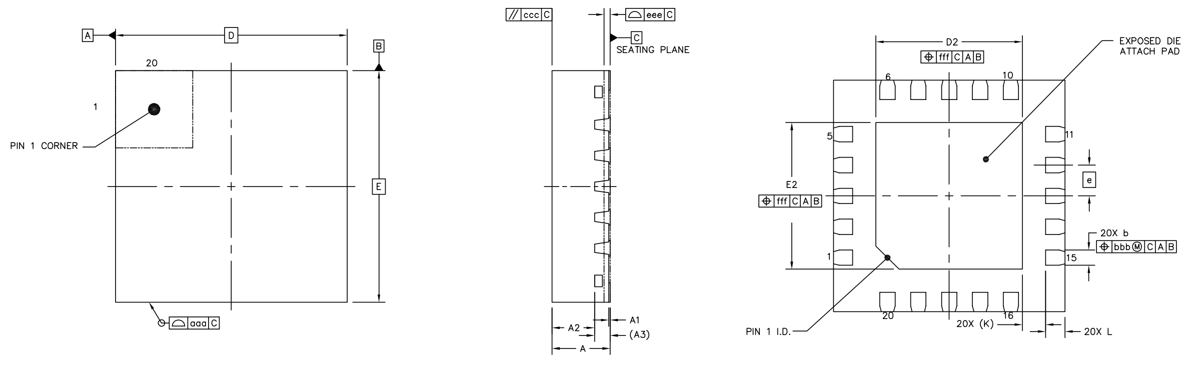
PACKAGE OUTLINE DIMENSIONS

QFN32



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	-	0.65	-
A3	0.203 REF		
b	0.2	0.25	0.3
D	5 BSC		
E	5 BSC		
e	0.5 BSC		
D2	3.3	3.4	3.5
E2	3.3	3.4	3.5
L	0.3	0.4	0.5
K	0.4 REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
ddd	0.05		
fff	0.1		

QFN20

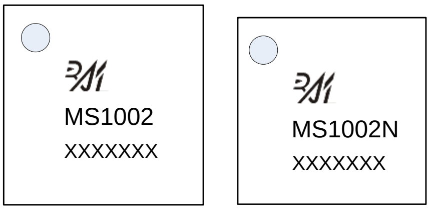


TOP VIEW　　SIDE VIEW　　BOTTOM VIEW

Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.15	0.2	0.25
D	3 BSC		
E	3 BSC		
e	0.4 BSC		
D2	1.8	1.9	2
E2	1.8	1.9	2
L	0.15	0.25	0.35
K	0.3 REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.07		
fff	0.1		

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name: MS1002, MS1002N

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS1002	QFN32	4000	1	4000	8	32000
MS1002N	QFN20	1000	8	8000	4	32000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1、The operator shall ground through the anti-static wristband.

2、The equipment shell must be grounded.

3、The tools used in the assembly process must be grounded.

4、Must use conductor packaging or anti-static materials packaging or transportation.

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