

## Low-voltage, 5V, Multi-channel Motor Driver

### FEATURES

- Two Stepper Motor Drivers, 1/1 Step to 1/256 Step Configurable, Maximum Operating Current 1A
- Selectable I<sup>2</sup>C or SPI Serial Bus Communication Control
- Instruction Cache Function, Motor Pre-stores the Next Order When Executing the Present One
- Integrated a DC Motor Driver, Maximum Operating Current 0.8A
- Built-in System Clock, Eliminating the Need for External Clock
- Software Low-power Mode, Hardware Low-power Mode
- QFN24 Package, QFN20 Package (Backside Heat Sink)

### APPLICATIONS

- Robot, Precision Industrial Equipment
- Oscillating Heat Press Machine
- Surveillance Camera
- PTZ

### PRODUCT DESCRIPTION

The MS32008N/MS32008N1 is a multi-channel motor driver chip, which includes two stepper motors and a DC motor driver; The maximum operating current of each motor driver is 1.0A; And two-phase four-wire and four-phase five-wire stepper motors are supported.

The MS32008N adopts selectable I<sup>2</sup>C or SPI serial bus control mode, which is compatible with 1.8V/3.3V/5V standard industrial interfaces.

The MS32008N1 adopts I<sup>2</sup>C communication mode, which is compatible with 1.8V/3.3V/5V standard industrial interfaces.

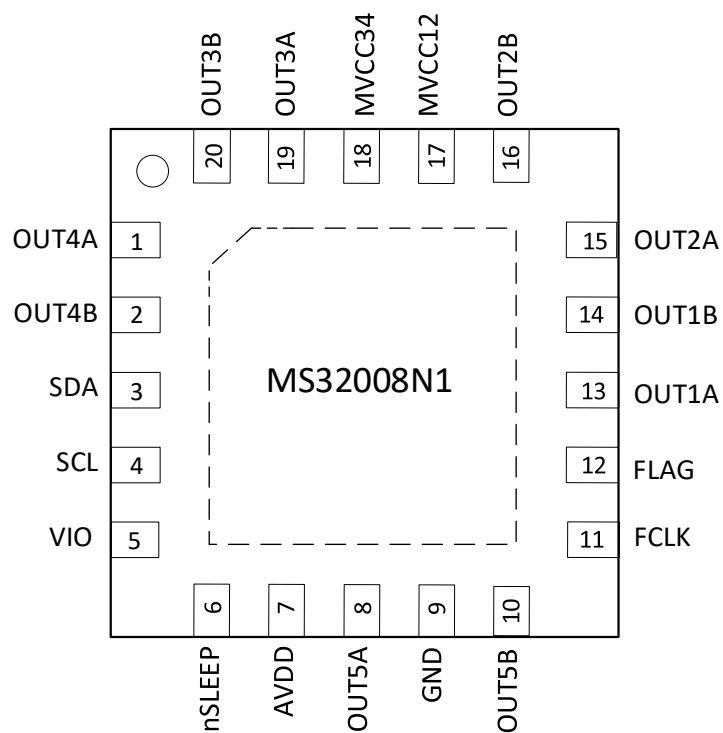
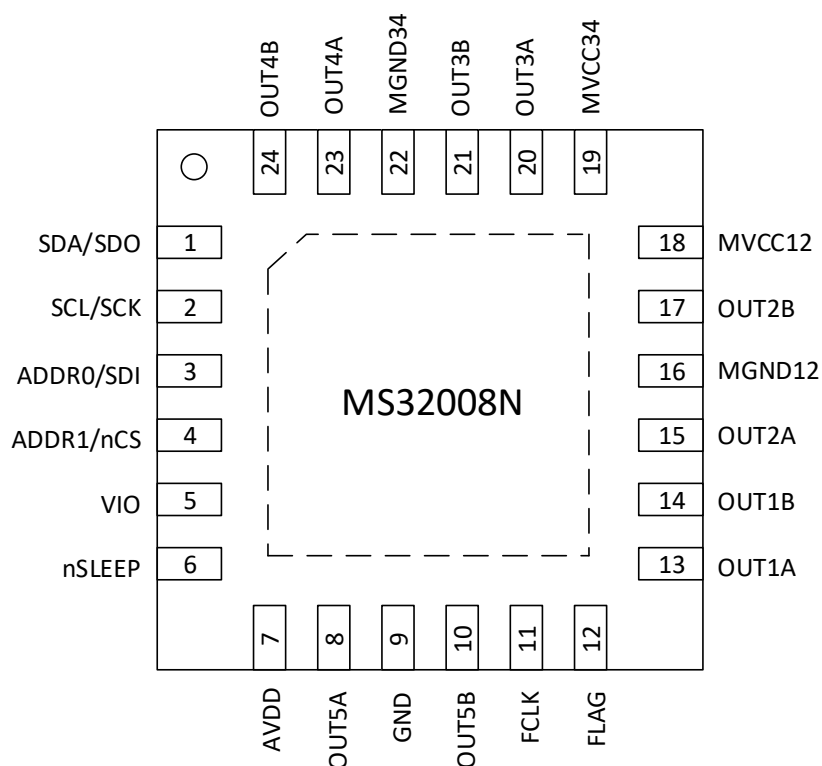
### PRODUCT SPECIFICATION

Part Number	Package	Marking
MS32008N	QFN24	MS32008N
MS32008N1	QFN20	32008N1

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## PIN CONFIGURATION



## PIN DESCRIPTION

### MS32008N

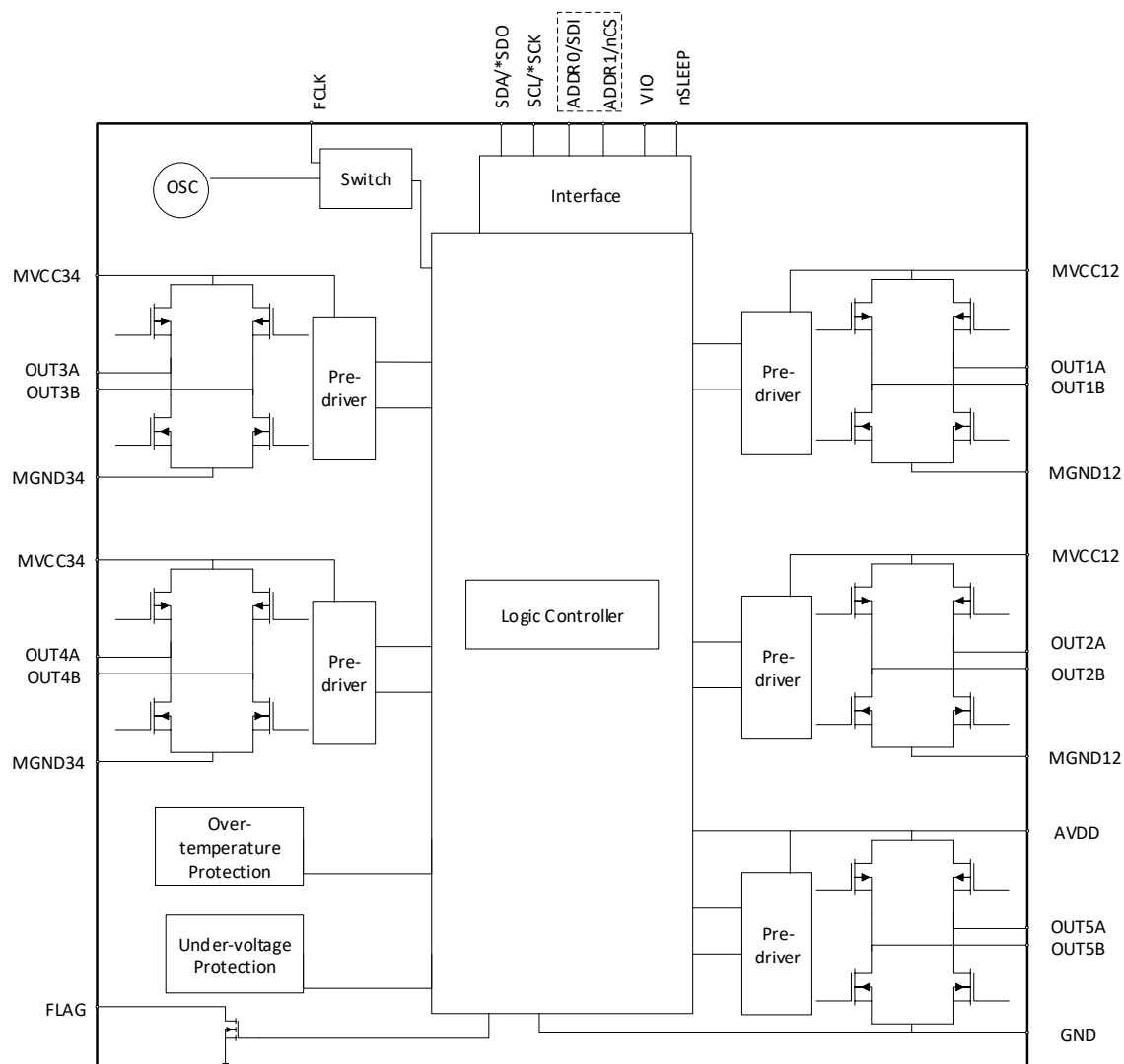
Pin	Name	Type	Description
1	SDA/SDO	IO	I <sup>2</sup> C Mode: I <sup>2</sup> C Data Input/ Output SPI Mode: SPI Data Output
2	SCL/SCK	I	I <sup>2</sup> C Mode: I <sup>2</sup> C Clock Input SPI Mode: SPI Clock Input
3	ADDR0/SDI	I	I <sup>2</sup> C Mode: Chip Address Select, Internal Pull-down SPI Mode: SPI Data Input
4	ADDR1/nCS	I	I <sup>2</sup> C Mode: Chip Address Select, Internal Pull-down SPI Mode: Chip Select, Active-low
5	VIO	-	Interface Power Supply
6	nSLEEP	I	Sleep Mode Control Pin
7	AVDD	-	Power Supply
8	OUT5A	O	DC Motor Channel Output
9	GND	-	Ground
10	OUT5B	O	DC Motor Channel Output
11	FCLK	I	Reference Clock Input, Internal clock can be used
12	FLAG	O	FLAG Indication Output
13	OUT1A	O	Stepper Motor Channel 1 Output
14	OUT1B	O	Stepper Motor Channel 1 Output
15	OUT2A	O	Stepper Motor Channel 2 Output
16	MGND12	-	Power Ground for Stepper Motor Channels 1, 2
17	OUT2B	O	Stepper Motor Channel 2 Output
18	MVCC12	-	5V Power Supply for Stepper Motor Channels 1, 2
19	MVCC34	-	5V Power Supply for Stepper Motor Channels 3,4
20	OUT3A	O	Stepper Motor Channel 3 Output
21	OUT3B	O	Stepper Motor Channel 3 Output
22	MGND34	-	Power Ground for Stepper Motor Channels 3, 4
23	OUT4A	O	Stepper Motor Channel 4 Output
24	OUT4B	O	Stepper Motor Channel 4 Output

## MS32008N1

Pin	Name	Type	Description
1	OUT4A	O	Stepper Motor Channel 4 Output
2	OUT4B	O	Stepper Motor Channel 4 Output
3	SDA	IO	I <sup>2</sup> C Data Input/ Output
4	SCL	I	I <sup>2</sup> C Clock Input
5	VIO	-	Interface Power Supply
6	nSLEEP	I	Sleep Mode Control Pin
7	AVDD	-	Power Supply
8	OUT5A	O	DC Motor Channel Output
9	GND	-	Ground
10	OUT5B	O	DC Motor Channel Output
11	FCLK	I	Reference Clock Input, Internal clock can be used
12	FLAG	O	FLAG Indication Output
13	OUT1A	O	Stepper Motor Channel 1 Output
14	OUT1B	O	Stepper Motor Channel 1 Output
15	OUT2A	O	Stepper Motor Channel 2 Output
16	OUT2B	O	Stepper Motor Channel 2 Output
17	MVCC12	-	5V Power Supply for Stepper Motor Channels 1, 2
18	MVCC34	-	5V Power Supply for Stepper Motor Channels 3,4
19	OUT3A	O	Stepper Motor Channel 3 Output
20	OUT3B	O	Stepper Motor Channel 3 Output

## BLOCK DIAGRAM

\* and dashed line box indication: only the MS32008N featured



## ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Motor Control Power Supply	V <sub>MVCC12</sub> V <sub>MVCC34</sub> V <sub>AVDD</sub>	-0.3 ~ +6	V
Interface, Logic Power Supply	V <sub>AVDD</sub> , V <sub>VIO</sub>	-0.3 ~ +6	V
Digital Input Voltage	V <sub>IN</sub>	-0.3 ~ V <sub>VIO</sub> + 0.3	V
FLAG Output Voltage	V <sub>FLAG</sub>	-0.3 ~ +6	V
H-bridge Driving Current of Stepper Motor Driver	I <sub>M1(1234)</sub>	±1.0	A/ch
H-bridge Driving Current of DC Motor Driver	I <sub>M2(5)</sub>	±0.8	A/ch
H-bridge Peak Current of Stepper Motor Driver	I <sub>M1(pulse1234)</sub>	±1.2	A/ch
H-bridge Peak Current of DC Motor Driver	I <sub>M2(pulse5)</sub>	±0.9	A/ch
Operating Temperature	T <sub>A</sub>	-40 ~ +125	°C
Storage Temperature	T <sub>STG</sub>	-65 ~ +150	°C
ESD (HBM)	V <sub>ESD</sub>	±6000	V

## ELECTRICAL CHARACTERISTICS

$V_{MVCC12}=V_{MVCC34}=5V$ ,  $V_{AVDD}=5V$ ,  $V_{VIO}=3.3V$ . Note: unless otherwise noted,  $T_A = 25^{\circ}C \pm 2^{\circ}C$ .

### Power Supply Range

Parameter	Symbol	Condition	Min	Typ	Max	Unit
MVCCX Drive Power Supply Range	$V_{MVCC}$		1.5	5	5.5	V
AVDD Logic Power Supply Range	$V_{AVDD}$		2.5	5	5.5	V
VIO Interface Power Supply Range	$V_{VIO}$		1.5		5.0	V

### Current Dissipation

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Dissipation in Quiescent Operation Mode	$I_{DDAVDD}$	nSLEEP=1,cmd_nRST=1, Standby=0	4	5.5	7	mA
Power Dissipation in Software Sleep Mode	$I_{AVDD\_SSTB}$	nSLEEP=1,cmd_nRST=0, Standby=1	11	17	23	$\mu A$
Power Dissipation in Hardware Sleep Mode	$I_{AVDD\_HSTB}$	nSLEEP=0			1	$\mu A$

### Digital Input and Output

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Voltage	$V_{IN(H)}$	SDA/SDO,SCL/SCK,ADDR0/SDI, ADDR1/nCS,nSLEEP,FCLK	$0.7 \times V_{VIO}$			V
low-level Input Voltage	$V_{IN(L)}$	SDA/SDO,SCL/SCK,ADDR0/SDI, ADDR1/nCS,nSLEEP,FCLK			$0.3 \times V_{VIO}$	V
FCLK Clock Input	$f_{CLK}$	External Clock Input Range	4		40	MHz
OSC Internal Clock	$f_{OSC}$	Internal Oscillator Clock		20		MHz
FLAG Saturation Voltage	$V_{FLAG}$	FLAG Low, 5mA Current			300	mV



**Stepper Motor Driver (Channel 1,2,3,4)(PTZ XY-axis Steering Control)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
H-bridge On-resistance	$R_{ON1234}$	$I_{OUT}=500mA$ , Upper Bridge and Lower Bridge		1.2		$\Omega$
Output Leakage Current	$I_{LEAK1234}$				1	$\mu A$

**DC Motor Driver (Channel 5) (IR-CUT)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
H-bridge On-resistance	$R_{ON5}$	$I_{OUT5}=500mA$ , Upper Bridge and Lower Bridge		1.5		$\Omega$
Output Leakage Current	$I_{LEAK5}$				1	$\mu A$

**Over-temperature Protection**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Temperature for Over-temperature Protection	$T_{TSD}$	Temperature Rising, Output Shutdown		160		$^{\circ}C$
Over-temperature Protection Hysteresis	$\Delta T_{TSD}$	Hysteresis Window		30		$^{\circ}C$

**Power Supply Monitor Circuit**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
AVDD Under-voltage	$V_{RSTON}$	Voltage Dropping, Output Shutdown		2.3		V
AVDD Under-voltage Hysteresis	$V_{RSTHYS}$			0.2		V

## FUNCTION DESCRIPTION

The MS32008N/MS32008N1 integrates two stepper motor drivers and one DC motor driver, which can be controlled via the I<sup>2</sup>C bus. The stepper motor controller can select step modes from full step to 1/256 step, generally used for X and Y-axis motion control of small PTZ. The DC motor control is also set through the I<sup>2</sup>C to control the motor's forward, reverse, braking, and free rotation states, which can be used for IR-cut control.

I<sup>2</sup>C(default) or SPI communication can be selected to use for the MS32008N, and the communication ports can be multiplexed; Only I<sup>2</sup>C communication can be used for the MS32008N1.

### I<sup>2</sup>C Mode

In I<sup>2</sup>C mode, SDA is a bidirectional data line. Data inputs or outputs through the SCL clock. For the MS32008N, the pins ADDR1 and ADDR0 form the 4th and 3rd bits (MSB...LSB) of 7-bit chip address according to the connected voltage levels.

Figures 1 and 2 show timing diagrams for a write cycle and a read cycle respectively. When the clock signal is high, a falling transition on SDA serves as the start condition. When the clock signal is high, a rising transition on SDA serves as the stop condition. All other transitions on SDA occur when the clock signal is low.

In the MS32008N/MS32008N1 communication, after the start condition, the first byte (ADDR) consisting of a 7-bit chip address and a 1-bit read/write (high for read, low for write) is sent to the MS32008N/MS32008N1. For the MS32008N, the first 3 bits of the 7-bit address are fixed as 001, and the last 2 bits are fixed as 00, with the 4th bit and 3rd bit matching the voltage level of the ADDR1 and ADDR0 pins. For the MS32008N1, the 7-bit address is fixed as 0010000. The least significant bit of the ADDR byte is the read/write bit. If it is a write operation, the next byte contains the register address pointer (MAP), which is used to select the register to be read or written. If it is a read operation, the content of the register addressed by MAP will be output. The MAP automatically increments, so the data of the registers will appear in sequence. Each byte is separated by an acknowledge bit (ACK). After each input byte is read, the MS32008N/MS32008N1 outputs an acknowledge bit, and after each byte transmission, the microcontroller sends an acknowledge bit to the MS32008N/MS32008N1.

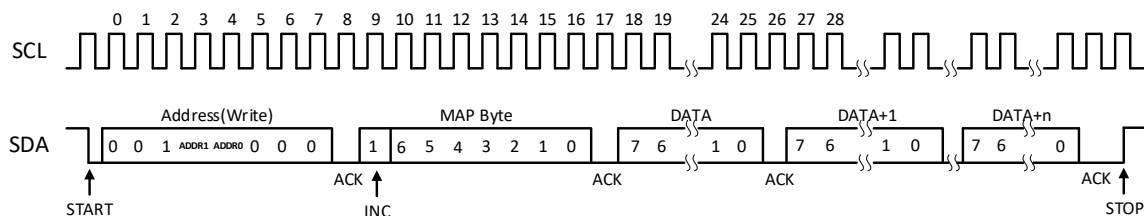


Figure 1. Control Port Timing, Write in I<sup>2</sup>C Slave Mode

\*For the MS32008N1, ADDR1 and ADDR0 in the figure are considered as 0, the same as the following figure.

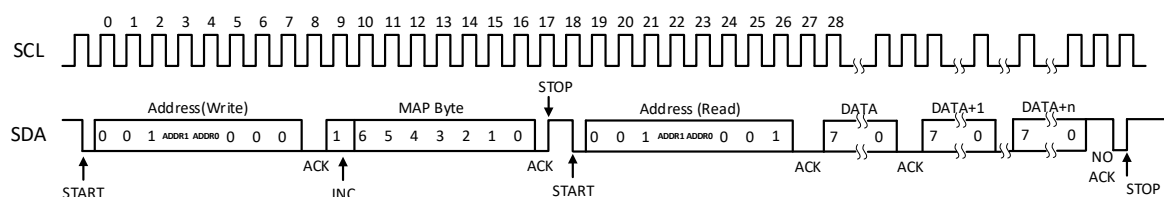


Figure 2. Control Port Timing, Read in I²C Slave Mode

Note that in the read operation, MAP cannot be set, so a terminated write operation is needed as a preamble. As shown in Figure 2, if a stop condition is sent after the acknowledge of MAP in a write operation, the write operation terminates.

### I²C Mode Timing Table

Input:  $V_{IO}=3.3V$ ,  $V_{AVDD}=5V$ ,  $C_L=20pF$

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	$f_{scl}$		400	kHz
Bus Free Time During Conversion	$t_{buf}$	1.3		$\mu s$
Hold Time for Start Condition (Before the First Clock Pulse)	$t_{hdst}$	0.6		$\mu s$
Low-level Clock Time	$t_{low}$	1.3		$\mu s$
High-level Clock Time	$t_{high}$	0.6		$\mu s$
Setup Time for Repeated Start Condition	$t_{sust}$	0.6		$\mu s$
Hold Time from SCL Falling Edge to SDA <sup>1</sup>	$t_{hdd}$		900	ns
Setup Time from SDA to SCL Rising Edge	$t_{sud}$	100		ns
SCL, SDA Rising Time	$t_{rc}, t_{rd}$		300	ns
SCL, SDA Falling Time	$t_{fc}, t_{fd}$		300	ns
Setup Time for Stop Condition	$t_{susp}$	0.6		$\mu s$
Delay from SCL Falling Edge to Acknowledge @SDA Pull-up Resistor 4.7k $\Omega$	$t_{ack}$	120	1000	ns

Note 1: Data must be held long time to bridge the conversion time  $t_{rc}$  of SCL.

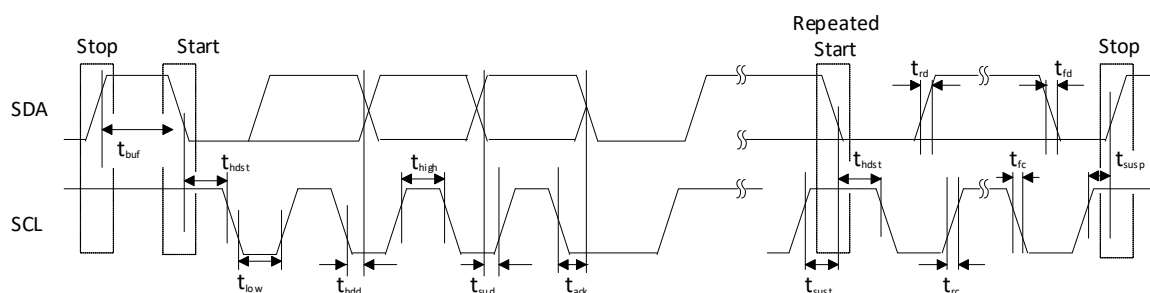


Figure 3. I²C Mode Timing

## SPI Mode

In SPI mode, nCS is the chip select signal for the MS32008N, SCK is the clock input pin (input from the microcontroller to the MS32008N), SDI is the data input pin, and SDO is the data output pin. Data is sampled at the rising edge of SCK and output at the falling edge. When the chip is powered on and not in low-power mode, a high-to-low transition on the ADDR1/nCS pin (nCS pulled low, chip select) will keep the chip in SPI communication mode before powered on.

Figure 4 shows the operation of the control port in SPI mode. When writing to a register, nCS is pulled low. The first 7 bits on SDI form the chip address and must be 0010000. The 8th bit is the read/write (R/W), with low level indicating write. The next 8 bits are the 8-bit register address pointer (MAP), which is the address of the register to be read or written. The next 8 bits are the data to be stored in the MAP specified register. In a write operation, the SDO output remains high-impedance. It is recommended to use a 4.7kΩ pull-up resistor on SDO.

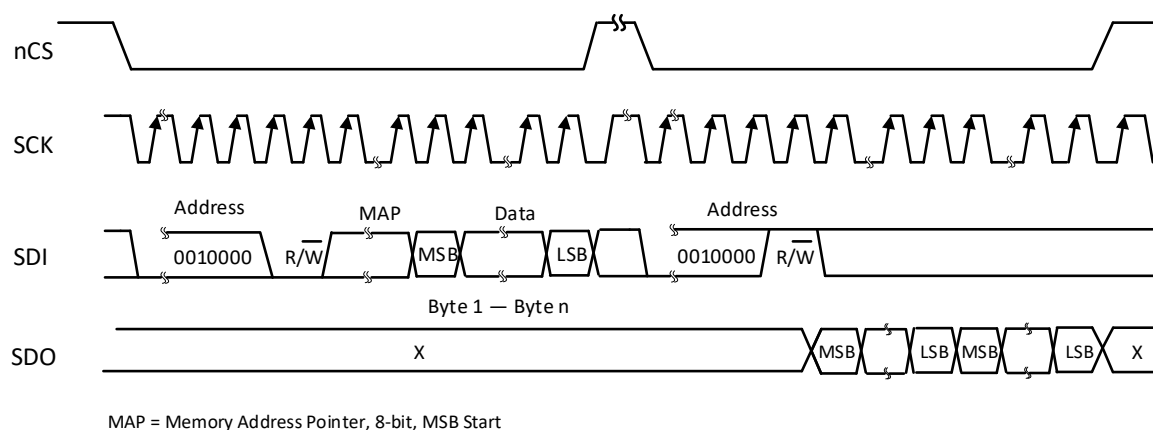


Figure 4. Control Port Timing, SPI Mode

SPI Control Mode: CPOL = 1, CPHA=1.

To read a register, MAP must be set to the correct address by performing a part of write cycle. After the MAP byte, nCS goes high. To start reading a register, nCS goes from high to low and sends the chip address and sets the read/write ( $R/\overline{W}$ ) to high. The falling edge of SCK will then output the most significant bit of the addressed register. MAP will automatically increment, so the data of the registers will appear in sequence.

## SPI Mode Timing Table

Input: logic 0 =  $V_{IN(L)}$ , logic 1 =  $V_{IN(H)}$ ;  $C_L = 20\text{pF}$ .

Parameter	Symbol	Min	Max	Unit
SCK Clock Frequency	$f_{sck}$	0	4.0	MHz
SCK Falling Edge to nCS Falling Edge	$t_{spi}$	500	-	ns
Transmission Interval for nCS High	$t_{csh}$	1.0	-	$\mu\text{s}$
nCS Falling Edge to SCK Falling Edge	$t_{css}$	20	-	ns

Parameter	Symbol	Min	Max	Unit
SCK Low-level Time	$t_{scl}$	66	-	ns
SCK High-level Time	$t_{sch}$	66	-	ns
Setup Time from SDI to SCK	$t_{dsu}$	40	-	ns
Hold Time from SCK Rising Edge to DATA <sup>1</sup>	$t_{dh}$	15	-	ns
Valid Time from SCK Falling Edge to SDO <sup>2</sup>	$t_{scdov}$	-	100	ns
Time from nCS Rising Edge to SDO Hi-Z@SDO Pull-up Resistor 4.7k $\Omega$	$t_{cscdo}$	100	-	ns
SDO Rising Time	$t_{r1}$	-	25	ns
SDO Falling Time	$t_{f1}$	-	25	ns
SCK, SDI Rising Time <sup>3</sup>	$t_{r2}$	-	100	ns
SCK, SDI Falling Time <sup>3</sup>	$t_{f2}$	-	100	ns

Note:

1. Data must be held long time to bridge the conversion time of SCK.
2. SDO should not be sampled during this period.
3.  $f_{sck} < 4\text{MHz}$ 。

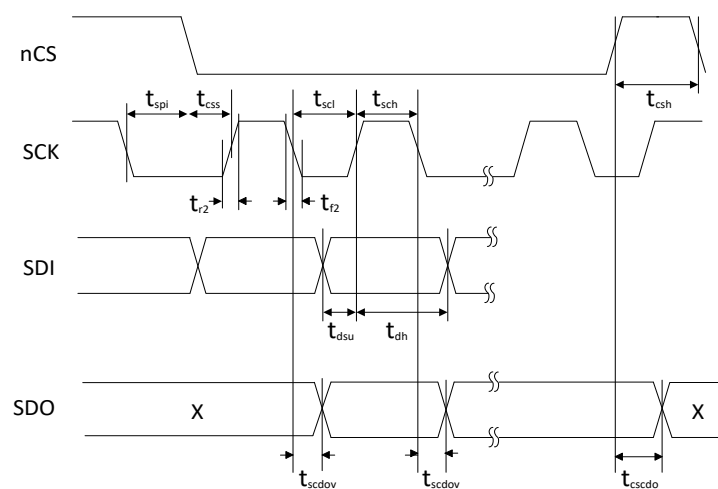


Figure 5. SPI Mode Timing

## Register Description

The word length of register address pointer (MAP) is 8 bits, including read and write control port addresses and an auto-increment control bit (MAP[7]). MAP[6:0] forms the address that can be read and written, and the 7thbit (INC) determines whether MAP[6:0] will increase automatically after each control port read or write. If INC=0, MAP[6:0] will not increase automatically; if INC=1, MAP[6:0] will increase automatically. The MAP bit is shown in figure 1 or figure 2.

The register table is as follows:

Type	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
Global and DC	00H	oscOFF	useExtClock	0	stm_fsw[2:0]			standby	cmd_nRST
	01H	ACH_confLoad	BCH_confLoad						
	02H	ACH_forceStop	BCH_forceStop						
	03H							DC_CTRL[1:0]	
	0DH	uvloClr	otsClr						
	0EH	watchEN	0	0	0	watchSel[3:0]			
	0FH	chipFlag[7:0](RO)							
Stepper A Channel Setting and Read	10H	ACH_motorType	ACH_pdEN	ACH_recordRev	ACH_lowDivLevel	0	0	0	0
	11H	ACH_msMode[3:0]				ACH_forceStopPos[1:0]		0	ACH_dir
	12H	ACH_freq[7:0]							
	13H	ACH_freq[15:8]							
	14H	ACH_pulse[7:0]							
	15H	ACH_pulse[15:8]							
	16H	ACH_amp[7:0]							
	1DH	0	0	0	0	ACH_Running(RO)	ACH_cacheBusy(RO)	ChipUVLO(RO)	ChipOTS(RO)
	1EH	ACH_pulseRecord[7:0]							
	1FH	ACH_pulseRecord[15:8]							

Stepper B Channel Setting and Read	20H	BCH_mot orType	BCH_pd EN	BCH_rec ordRev	BCH_low DivLevel	0	0	0	0
	21H	BCH_msMode[3:0]				BCH_forceStopPos [1:0]		0	BCH_dir
	22H	BCH_freq[7:0]							
	23H	BCH_freq[15:8]							
	24H	BCH_pulse[7:0]							
	25H	BCH_pulse[15:8]							
	26H	BCH_amp[7:0]							
	2DH	0	0	0	0	BCH_Ru nning (RO)	BCH_cac heBusy (RO)	ChipUV LO (RO)	ChipOTS (RO)
	2EH	BCH_pulseRecord[7:0]							
	2FH	BCH_pulseRecord[15:8]							

Note:

1. ACH\_ prefix responds to A channel stepper motor setting made up of OUT1A, OUT1B, OUT2A, OUT2B output ports.
2. BCH\_ prefix responds to B channel stepper motor setting made up of OUT3A, OUT3B, OUT4A, OUT4B output ports.
3. In the following text, XCH\_ prefix represents the channel A or B.
4. XCH\_msMode, XCH\_dir, XCH\_freq and XCH\_ pulse registers have cache registers, while other registers do not.
5. The data written to the register is determined after it is written to its address.

#### cmd\_nRST

Used for software reset.

D0	State
0	Reset (Initial State)
1	Non-reset State

When setting 0, logic controller is set to initial state. Before configuring other register, this bit must be set to 1.

#### useExtClk

Used for selecting system clock source.

D0	Clock Source
0	Use the Internal Oscillator Clock (Initial State)
1	Input from the FCLK Pin

When using the internal clock, the FCLK pin must be connected to GND.

### stm\_fsw

Used for selecting the stepper motor switching frequency.

$$f_{sw}(\text{kHz}) = 0.49 \times \text{SLOPE} \times \text{FCLK}(\text{MHz})$$

In the formula above, FCLK is the system clock frequency, SLOPE is a calculation parameter, configured as follows:

D2...D0	SLOPE
000	2
001	4
010	6
011	8
100	10
101	13
110	16
111	20

### standby

Used for power saving.

D0	State
0	Normal Operation
1	Instruction Power Saving Mode (Initial State)

When set to 1, output is set to HiZ, and parts of modules are disabled to reduce standby power consumption, achieving "instruction power saving".

### oscOFF

Used for disabling the internal clock generator

D0	Internal Clock State
0	Enable (Initial State)
1	Disable the Internal Clock Source

The internal clock source is disabled, the overall power consumption of the chip will be reduced.

### XCH\_confLoad

Used for loading stepper motor configuration items and enabling the motor.

D0	Enable
0	No (Initial State)
1	Load Motor Configuration and Operation (self-clearing)



Note:

1. After the stepper A, B channel configuration items are written, each of them is saved in interface module. Only when XCH\_confLoad is sent, all of registers in the interface module served as “a group of configurations” are loaded to logic controller, and applied to the corresponding channel.
2. After the register is written, it will be self-clearing. If the motor is static, it will be enabled according to the present configuration; if the motor is already enabled, the motor configuration is sent to cache register. It will be enabled automatically after the present configuration is completed.
3. The necessary conditions for stepper channel output are as follows:
  - ① cmd\_nRST soft reset is released, and not in standby mode
  - ② No undervoltage event occurs
  - ③ No overtemperature event occurs
  - ④ Corresponding bridge driver enable (XCH\_pdEN = 1)
  - ⑤ After configuring the operating parameters, sent XCH\_confLoad command

#### XCH\_forceStop

Used for forcing the stepper motor to stop immediately.

D0	Motor State
0	Normal Operation (Initial State)
1	Stop Immediately at the Present Position

Note:

1. When XCH\_forceStop is set to 1, sent XCH\_confLoad is invalid.
2. After XCH\_forceStop is set from 1 to 0, XCH\_confLoad can be sent directly to enable the motor according to the original configuration, or XCH\_msMode, XCH\_freq, XCH\_dir, XCH\_pulse, etc. can be used to update registers. The updated configuration will be applied to the corresponding channel after XCH\_confLoad is sent.

#### DC\_CTRL

Used for setting the DC motor drive state.

D1	D0	Drive State
0	0	Hi-Z (Initial State)
0	1	Forward
1	0	Reverse
1	1	Brake

The necessary conditions for DC channel output:

1. cmd\_nRST soft reset is released, and not in standby mode
2. No undervoltage event occurs
3. No overtemperature event occurs
4. DC\_CTRL register is not set to 00.

### uvloClr

Used for clearing under-voltage event cache.

D0	Function
0	No Operation (Initial State)
1	Clear Under-voltage Event Cache (Self-clearing)

When reading the RO bit in under-voltage event is 1, writing 1 to uvloClr, if there is no under-voltage event, read the under-voltage event RO bit again to 0. This register will be self-clearing after writing.

### otsClr

Used for clearing over-temperature event cache.

D0	Function
0	No Operation (Initial State)
1	Clear Over-temperature Event Cache (Self-clearing)

When reading the RO bit in over-temperature event is 1, writing 1 to otsClr, if there is no over-temperature event, read the over-temperature event RO bit again to 0. This register will be self-clearing after writing.

### watchEN

Used for enabling watch output.

D0	FLAG Output Signal
0	Operation State Indication (Initial State)
1	Watch Output

Operation state indication. The FLAG pin is open-drain output. High-level output is default after pulled up.

When any of the following occurs:

1. A group of configurations completes operation.
2. An under-voltage event occurs.
3. An over-temperature event occurs.

At this time, a low-level pulse signal with the width of t will output on the FLAG pin to notify the main controller. The pulse width t is calculated as follows:

$$t(\mu s) = 127 \div FCLK(MHz)$$

### watchSel

Select the signal to be watched for FLAG output.

D3...D0	FLAG Output Signal
0000	A channel FG (a 1/4 stepper responds to one rising edge and one falling edge)
0001	Reserved
0010	Equal to ACH_Running, low-level when channel A motor is enabled

D3...D0	FLAG Output Signal
0011	Equal to ACH_cacheBusy, low-level when the instruction cache is in channel A
0100	channel B FG (a 1/4 stepper responds to one rising edge and one falling edge)
0101	Reserved
0110	Equal to BCH_Running, low-level when channel B motor is enabled
0111	Equal to BCH_cacheBusy, low-level when the instruction cache is in channel B
1000	/
1001	/
1010	/
1011	/
1100	Reserved
1101	Real-time over-temperature signal
1110	Real-time under-voltage signal
1111	System clock 400 division, measured frequency is (FCLK×2.5) kHz, square wave of 50% duty cycle

### chipFlag(RO)

Read-only register, indicating chip version, the MS32008N/MS32008N1 will read 0x08

### XCH\_motorType

Used for selecting the stepper motor driver type for channel A/B.

D0	Driver Type
0	2-phase 4-wire (Initial State)
1	4-phase 5-wire

Note:

1. 4-phase 5-wire motors are only used in level-drive mode(XCH\_lowDivLevel=1) and low subdivision.
2. Low subdivision refers to 1/1 division and 1/2 division.

### XCH\_pdEN (Power Driver Enable)

Used for enabling bridge driver.

D0	Bridge Driver State
0	Disable (Initial State)
1	Enable

When the bridge driver is disabled, the output of the stepper module for the corresponding channel is paused, output is in Hi-Z state. However, commands or cached commands can still be received.

### XCH\_recordRev

Used for changing the counter counting polarity.

D0	Counter Counting Way
0	Forward Increment, Reverse Decrement (Initial State)
1	Forward Decrement, Reverse Increment

### XCH\_lowDivLevel

Used for setting the drive mode for low subdivision

D0	Drive Mode in Subdivision
0	PWM (Initial State)
1	Llevel

Note:

1. Low subdivision refers to 1/1 division and 1/2 division.
2. In low subdivision and level-drive mode(XCH\_lowDivLevel=1), XCH\_amp is not valid.

### xCH\_msMode (Subdivision Mode)

Used for setting the motor subdivision mode

D3...D0	Drive Mode
0000	1/256 Step (Initial State)
0001	1/128 Step

D3...D0	Drive Mode
0010	1/64 step
0011	1/32 step
0100	1/16 step
0101	1/8 step
0110	1/4 step
0111	1/2 step
1000	Full step

Note: When changing the subdivision mode, do not set the number of Pulse to 0.

#### XCH\_dir

Used for setting the rotation direction.

D0	Direction
0	CW (Forward, Initial State)
1	CCW (Reverse)

#### XCH\_forceStopPos

Used for controlling the stopping position when forced to stop.

D1...D0	Motor State
00	1-4 Phase Position(Initial State)
01	1-2 Phase Position
10	2-Phase Position
11	1-Phase Position

Note:

1. operated in 1/2 step, forceStopPos [1:0] is set to "00", equal to "01".
2. Operated in full step, forceStopPos [1:0] is set to "00" "01" "11", equal to "10".

#### XCH\_freq

Used for setting the motor operation pulse frequency.

D15...D0	Pulse Frequency
< 0x007F	Prohibited (Initial State: all 0)
0x00FF	FCLK / (255 × 16)pps
~	~
0xFFFF	FCLK / (65535 × 16)pps

Note:

1. The initial state only exists after the reset signal is released, do not set XCH\_freq to the prohibited range.
2. FCLK is the clock frequency provided to the main logic (MHz).

For example: XCH\_freq = 0x02EE.

Pulse frequency(pps) =(FCLK × 10<sup>6</sup>) / (750 × 16).

### XCH\_pulse

Used for setting the number of 1/4 step of motor operation

D15...D0	The Number of 1/4 Step
0x0000	0
0x00FF	255
~	~
0xFFFF	65535

Note:

1. D0 is invalid in 1/2 subdivision drive mode, and D1...D0 is invalid in full-step drive mode.
2. Motor shift = step angle × resolution × step number, the MS32008N/MS32008N1 resolution is 1/4.

For example: step angle is 0.9°, set ACH\_pulse = 0x0640 , then channel A motor operates: 0.9 × 1/4 × 1600 = 360°

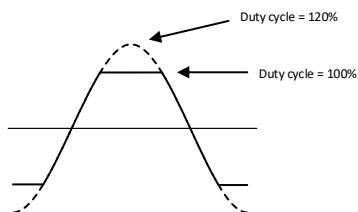
### XCH\_amp

Used for adjusting the maximum output duty cycle, effective immediately. The table below shows the values needed for each subdivision mode when the maximum output duty cycle is 100% (corresponding to 100% current output).

Subdivision Mode	D7...D0
1/1、1/2、1/32-1/256 Subdivision	0x82
1/16 Subdivision	0x83
1/8 Subdivision	0x84
1/4 Subdivision	0x8B

The duty cycle takes effect immediately after writing to the corresponding register. The PWM duty cycle controls the operating current amplitude. Since the PWM duty cycle cannot exceed 100%, there will be a clipping phenomenon when configuring a current amplitude >100%. Configure different current amplitudes in proportion, with a maximum support of 140%.

Example 1: When the subdivision mode is 1/1, 1/2, 1/32-1/256, configure XCH\_amp=130(0x82)×1.2=156(0x9C), output amplitude is 120%. And the waveform of the target current for the corresponding channel is as follows:



Example 2: Configure different current amplitudes in proportion. In 1/1, 1/2, 1/32-1/256 subdivision modes, configure  $XCH\_amp=130(0x82) \times 0.5=65(0x41)$ , current amplitude is 50%. In 1/8 subdivision mode, configure  $XCH\_amp=132(0x84) \times 0.5=66(0x42)$ , current amplitude is 50%.

#### XCH\_Running(RO)

Used for indicating that a stepper motor in a certain channel is operated, read-only.

D0	State
0	Disable (Initial State)
1	Enable

#### XCH\_cacheBusy(RO)

Used for indicating that cache is occupied in a certain channel, read-only.

D0	State
0	No Occupied (Initial State)
1	Occupied

#### chipUVLO(RO)

Used for indicating that under-voltage event occurs, read only

D0	State
0	No Occur (Initial State)
1	Occur

#### chipOTS(RO)

Used for indicating that over-temperature event occurs, read only

D0	State
0	No Occur (Initial State)
1	Occur

#### XCH\_pulseRecord

XCH\_pulseRecord is used for recording the number of 1/4 pulses that have been operated for the corresponding channel, default value is 0x0000. When XCH\_recordRev=0 (initial state), when operating XCH\_dir=0 configuration for positive counting (increment), and XCH\_dir=1 configuration for reverse

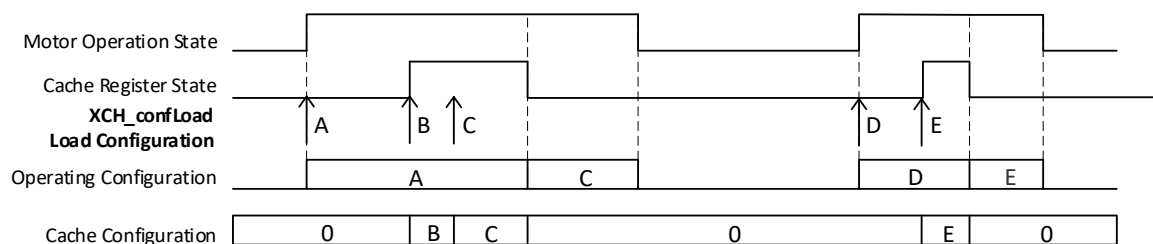
counting (decrement), counting full 0xFFFF then continues to count up to return to 0x0000, 0x0000 continues to count down to 0xFFFF. Note that after the counter overflows, it will not provide pulse indication from the FLAG pin.

Taking channel A as an example, writing data directly to ACH\_pulseRecord (0x1E, 0x1F address) can change the present record value. The present record value of channel A will change after writing to the 0x1F address (writing only to 0x1E will not change, but writing to 0x1E address will be retained, and it will take effect after the next write to 0x1F address). Channel B is the same.

When the bridge driver is disabled (XCH\_pdEN=0 or over-temperature event occurs), the number of 1/4 pulses operated will not be recorded.

### Cache Function

Each stepper channel of the MS32008N/MS32008N1 has one group of cache registers, which can store the configuration loaded during motor operation, and the motor will continue to operate with the cached configuration after the present configuration is completed.



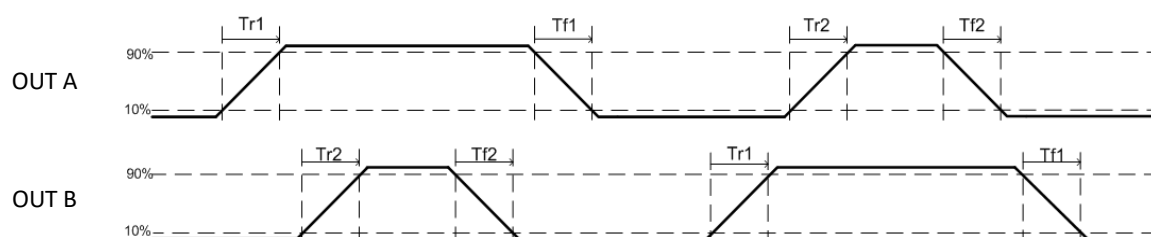
The operation configuration of the stepper motor (XCH\_msMode, XCH\_freq, XCH\_dir, XCH\_pulse) is determined after writing to XCH\_confLoad. When the present configuration is operated, the reloaded configuration will be cached in the cache register, and after the present configuration is completed, the cached configuration will be continued. The cached configuration can still receive new loaded configurations when it is still in the cache, and the new input configuration will cover the original configuration.



**Timing Table 3**

Default condition:  $T_A=25^{\circ}\text{C}$ ,  $V_{VIO} = 3.3\text{V}$ ,  $V_{AVDD}=5\text{V}$ ,  $V_{MVCC} = 5\text{V}$ , load resistor is  $16\Omega$ .

Parameter	Symbol	Typ
<1 ~ 5ch Constant Voltage Output Module>		
Rising Time 1	Tr1	5ns
Rising Time 2	Tr2	5ns
Falling Time 1	Tf1	5ns
Falling Time 2	Tf2	5ns



### Power-saving Mode Function Description

The MS32008N/MS32008N1 has 2 power saving ways to reduce power dissipation:

Power Saving Mode	Function Description
nSLEEP Pin Mode	Through the external nSLEEP pin, set to low level or open circuit to realize full chip shutdown to achieve power saving, with current less than $1\mu\text{A}$ in this mode.
Instruction Mode	Set standby to 1, disable the drive module, etc., and only retain the internal communication module and part of the power management module. In this mode, when there is no clock signal input to the FCLK pin, the power consumption is less than $50\mu\text{A}$ ; when oscOff is set to 1, the internal oscillator is also disabled.

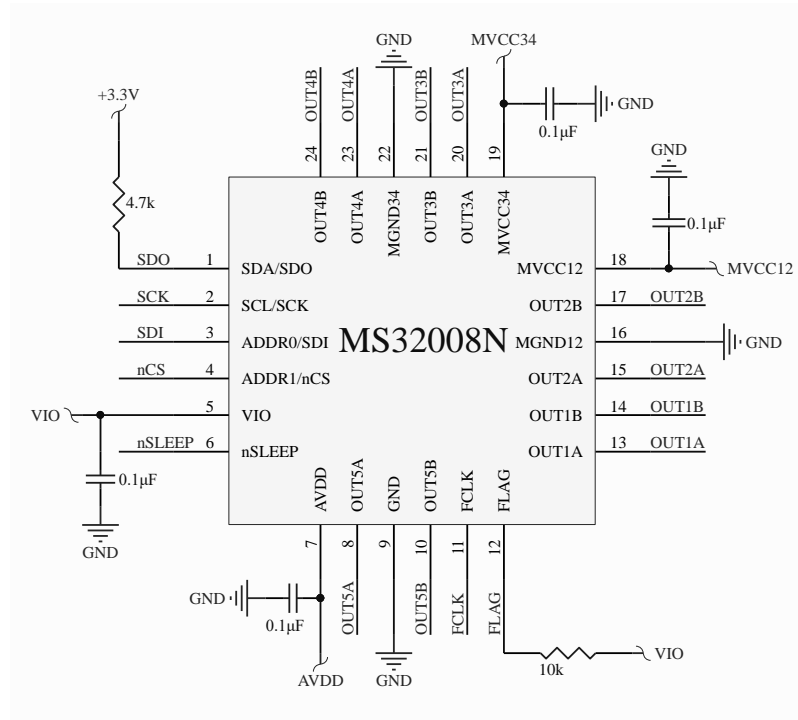
### Protection Function

The MS32008N/MS32008N1 integrates multiple protections: under-voltage protection, over-temperature protection.

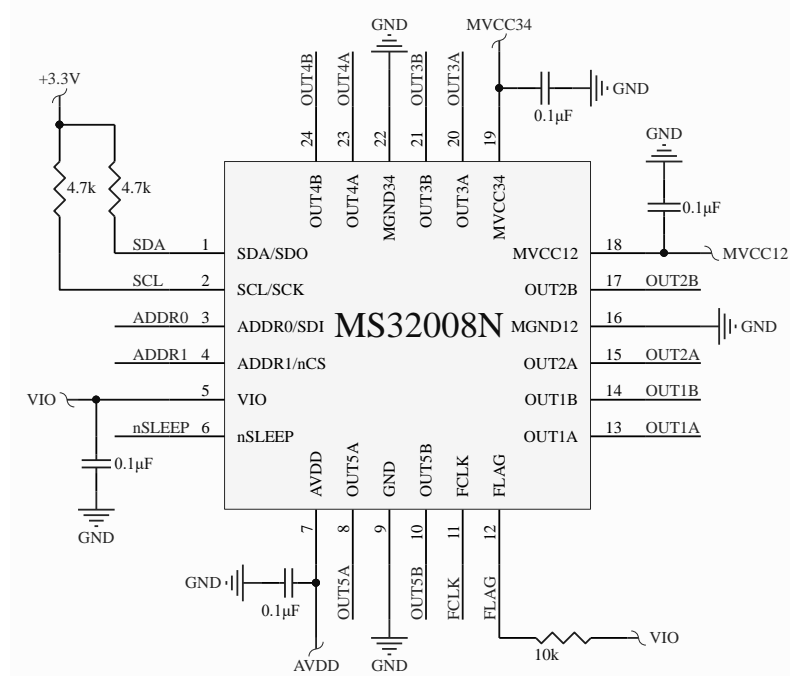
Protection	Function Description
Under-voltage Protection	When the AVDD power supply voltage is lower than $2.3\text{V}$ , the chip is in under-voltage protection, the chip will disable the output; if the under-voltage protection events occur, under-voltage event cache can be read from $1\text{DH}<1>$ or $2\text{DH}<1>$ .
Over-temperature Protection	When the chip temperature exceeds $160^{\circ}\text{C}$ , the chip will disable the output, the step counter will stop counting until the temperature drops below $130^{\circ}\text{C}$ to resume operation; If the over-temperature protection occurs, over-temperature event cache can be read from $1\text{DH}<0>$ or $2\text{DH}<0>$ .

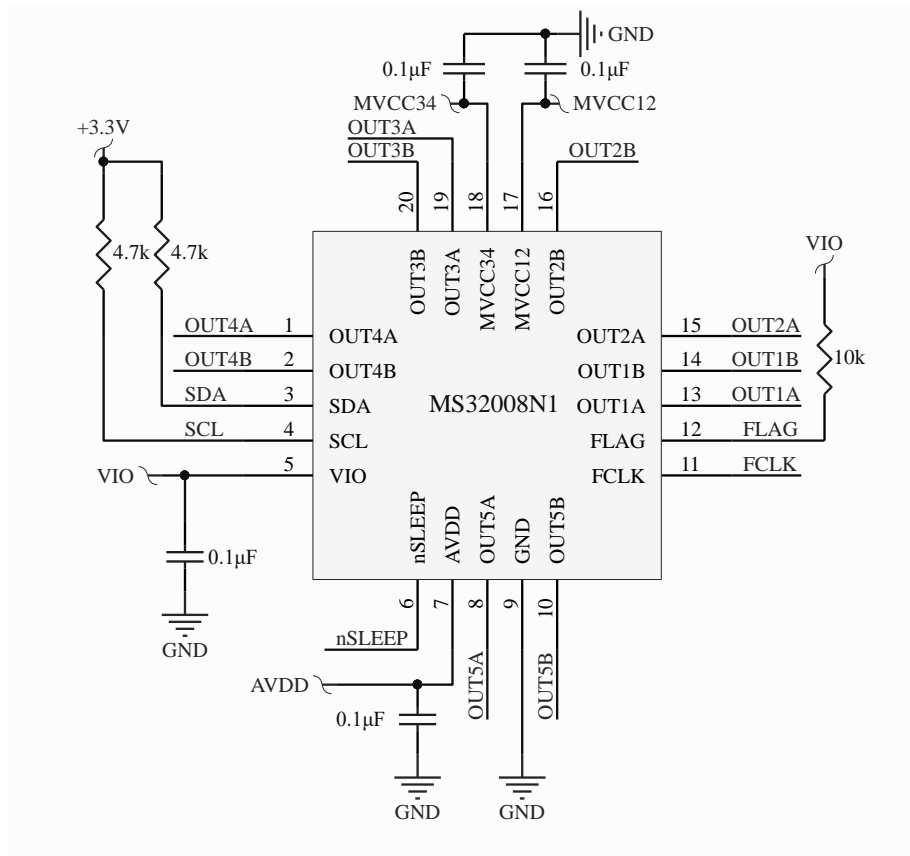
## TYPICAL APPLICATION

### SPI Mode Application

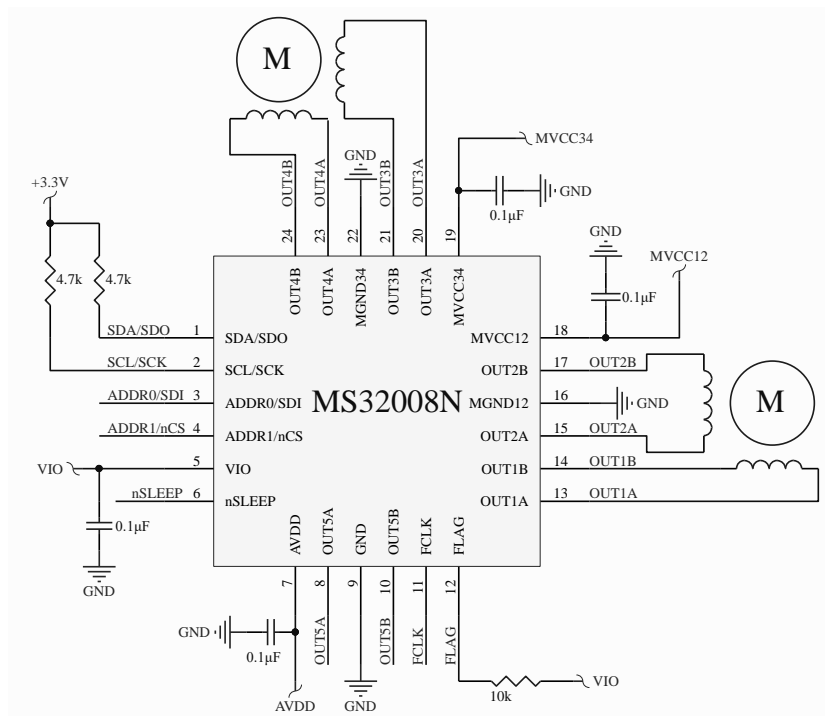


### I<sup>2</sup>C Mode Application

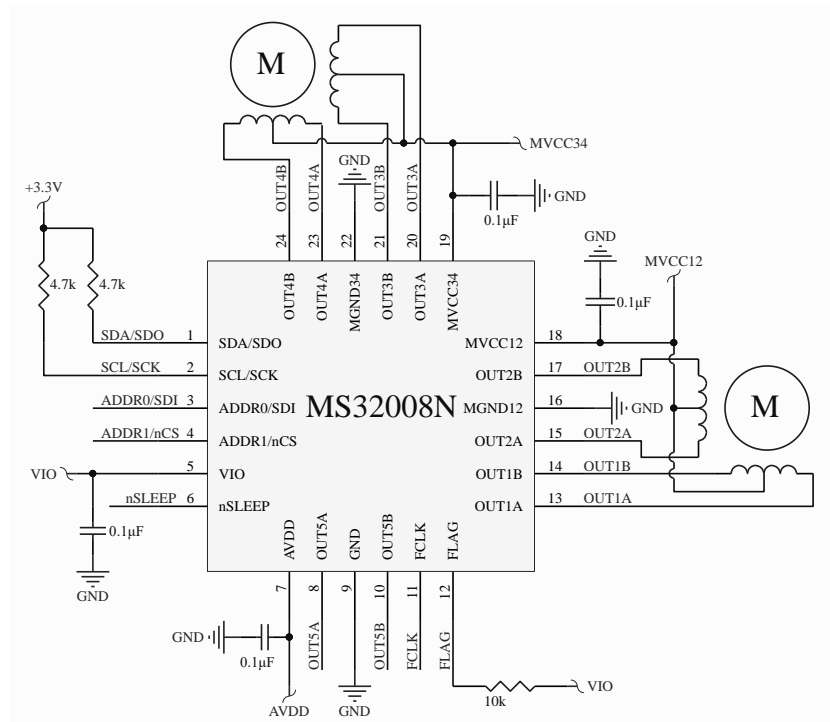




### Two-phase Four-wire Mode Application



### Four-phase Five-wire Mode Application

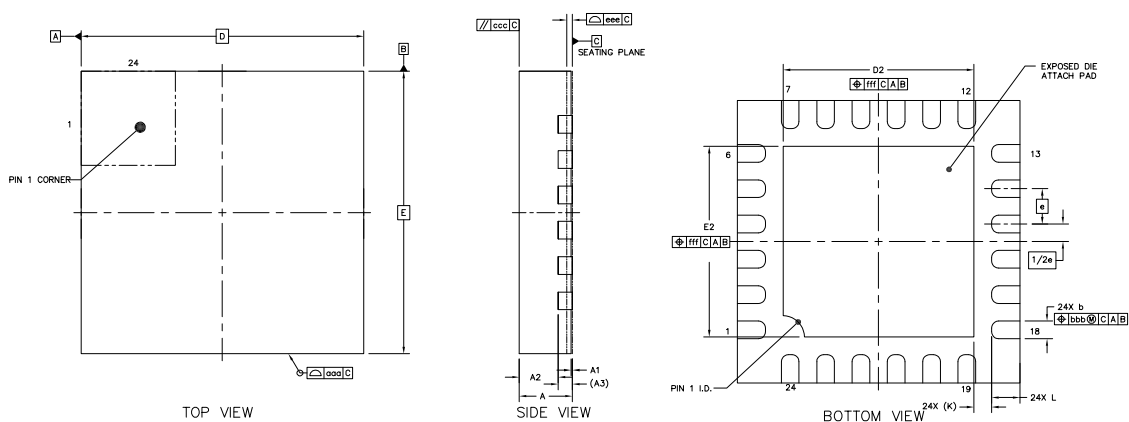


Note:

1. The MS32008N/MS32008N1 is featured with a backside heat sink, which must be connected to the ground.
2. All the input voltage should not exceed the absolute ratings.
3. The voltage range on the nSLEEP pin should be less than or equal to VIO.
4. When the MS32008N replaces the MS32006 and the MS32007 by PIN TO PIN, please note that pin6 nSLEEP interface level should be matched with VIO supply, which cannot exceed VIO.

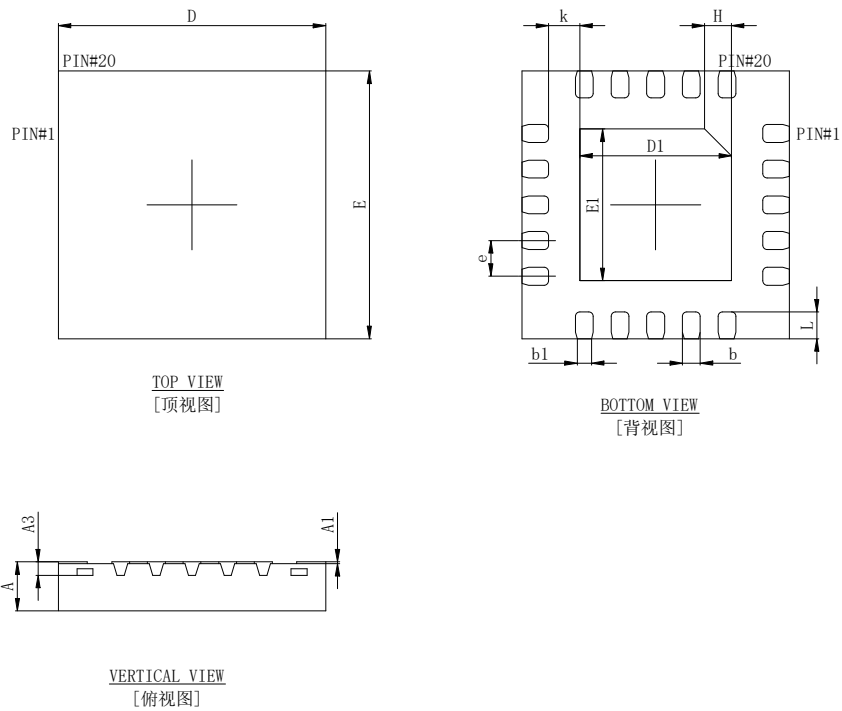
# PACKAGE OUTLINE DIMENSIONS

QFN24



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203REF		
b	0.2	0.25	0.3
D	4BSC		
E	4BSC		
e	0.5BSC		
D2	2.6	2.7	2.8
E2	2.6	2.7	2.8
L	0.3	0.4	0.5
K	0.2MIN		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		

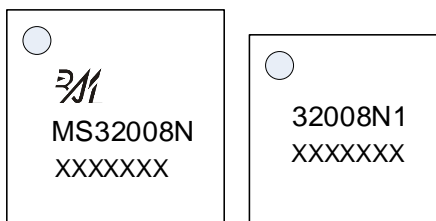
## QFN20



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.500	0.550	0.600
A1	0.000	0.020	0.050
A3	0.152REF		
b	0.150	0.200	0.250
b1	0.160REF		
D	2.900	3.000	3.100
E	2.900	3.000	3.100
e	0.400BSC		
D1	1.600	1.700	1.800
E1	1.600	1.700	1.800
L	0.200	0.300	0.400
k	0.350REF		
H	0.300REF		

## MARKING and PACKAGING SPECIFICATION

### 1. Marking Drawing Description



Product Name: MS32008N, 32008N1

Product Code: XXXXXXX

### 2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

### 3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS32008N	QFN24	4000	1	4000	8	32000
MS32008N1	QFN20	4000	1	4000	8	32000

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  - The process of improving product is endless. And our company would sincerely provide more excellent product for customer.
-



**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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