

## 24bit, 192kHz Dual Channel Digital to Analog Converter

### PRODUCT DESCRIPTION

The MS4344 is a stereo digital-to-analog converter, which contains interpolation filter, a multi-bit modulator and output analog filter. The MS4344 supports most of audio data formats. It is based on a fourth order multi-bit  $\Delta$ - $\Sigma$  modulator. With a linear analog low-pass filter. The MS4344 can automatically adjust the sample rate between 2kHz and 200kHz by detecting signal frequency and master clock frequency. The MS4344 can operate at 3.3V and 5V. These features make it ideal for wireless devices such as DVD player & recorder and digital communication device.

The MS4344 is available in MSOP10 package.



MSOP10

### FEATURES

- Muti-bit  $\Delta$ - $\Sigma$  Modulator
- 24bit D/A Converter
- Automatic Detection of Signal Frequency up to 192kHz
- DR: 110dB
- THD: 0.003%
- Low Clock Jitter Sensitivity
- 3.3V or 5V Operating Voltage
- Linear Filter Output
- MSOP10 Package

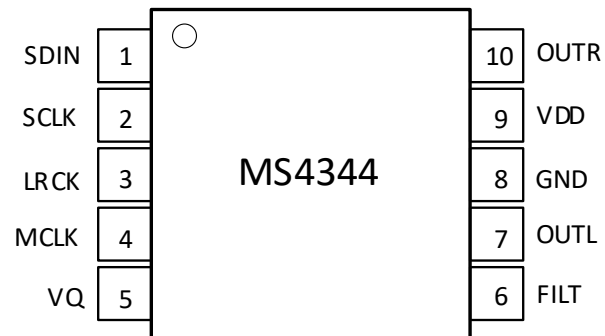
### APPLICATIONS

- Digital Communication Device
- Car Audio System
- DVD Audio System

### PRODUCT SPECIFICATION

Part Number	Package	Marking
MS4344	MSOP10	MS4344

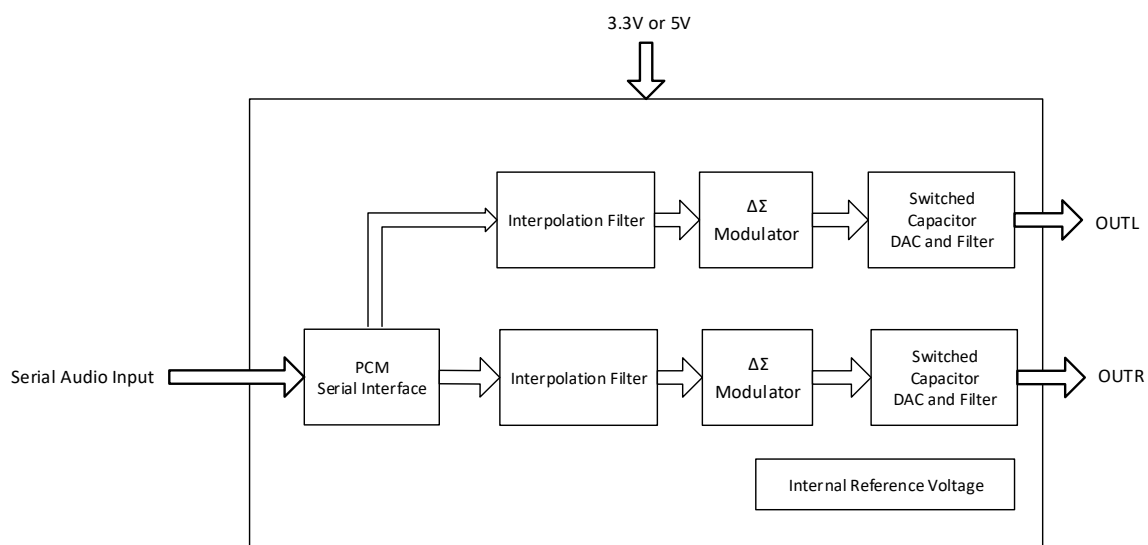
## PIN CONFIGURATION



## PIN DESCRIPTION

Pin	Name	Type	Description
1	SDIN	I	Serial Audio Data Input
2	SCLK	I	External Serial Clock Input
3	LRCK	I	Left or Right Clock
4	MCLK	I	Master Clock
5	VQ	IO	DC Voltage
6	FILT	IO	Positive Reference Voltage
7	OUTL	O	Left Channel Analog Output
8	GND	-	Ground
9	VDD	-	Analog Power
10	OUTR	O	Right Channel Analog Output

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	$V_{DD}$	-0.3 ~ 7	V
Input Current	$I_{IN}$	-10 ~ +10	mA
Digital Input Voltage	$V_{IND}$	-0.3 ~ $V_{DD}+0.3$	V
Operating Temperature	$T_A$	-40 ~ 125	°C
Storage Temperature	$T_{STG}$	-65 ~ 150	°C

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	$V_{DD}$	3.0		5.5	V

## ELECTRICAL CHARACTERISTICS

### DAC Analog Characteristics

$T_A = 25^{\circ}\text{C}$ , Full-scale Output Sinusoidal Signal, 997Hz,  $f_s=48/96/192\text{kHz}$ ;  $R_L=3\text{k}\Omega$ ,  $C_L=10\text{pF}$ , Test Bandwidth 10Hz to 20kHz.

Parameter			3.3V			Unit
			Min	Typ	Max	
DR	24 bit	A-weighted	100	102		dB
THD	24 bit	0dB		0.003	0.01	%
		-60dB		0.3		%

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Channel Isolation (1kHz)			95	100		dB
<b>DC Accuracy</b>						
Channel-to-Channel Gain Mismatch				0.1	0.2	dB
<b>Analog Output</b>						
Full-scale Output Voltage			$0.63 \times V_{DD}$	$0.66 \times V_{DD}$	$0.69 \times V_{DD}$	V <sub>pp</sub>
Quiescent Voltage	$V_Q$			$0.5 \times V_{DD}$		V <sub>DC</sub>
Maximum DC Current from OUT	$I_{OUTmax}$			3.3		mA
Maximum Current draw from V <sub>Q</sub>	$I_{Qmax}$			1		mA
Maximum Resistive Load	$R_L$			1		k $\Omega$
Maximum Capacitive Load	$C_L$			1000		pF
Output Impedance	$Z_{OUT}$			110		$\Omega$

### Filter Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
<b>Single-Speed Mode</b>						
PassBand	to -0.1 dB corner				0.35	$f_s$
	to -3 dB corner				0.4992	$f_s$
Frequency Response from 40Hz to 15kHz			-0.07		+0.55	dB
StopBand			0.54			$f_s$
StopBand Attenuation			55			dB
Group Delay		$t_{GD}$		10/ $f_s$		s

Parameter		Symbol	Min	Typ	Max	Unit
<b>Double-Speed Mode</b>						
PassBand	to -0.1 dB corner		0		0.22	$f_s$
	to -3 dB corner		0		0.501	$f_s$
Frequency Response from 40Hz to 15kHz			-0.02		+0.2	dB
StopBand			0.54			$f_s$
StopBand Attenuation			55			dB
Group Delay		$t_{GD}$		$5/f_s$		s
<b>Quad-Speed Mode</b>						
PassBand	to -0.1 dB corner		0		0.11	$f_s$
	to -3 dB corner		0		0.469	$f_s$
Frequency Response from 40Hz to 15kHz			-0.01		+0.1	dB
StopBand			0.54			$f_s$
StopBand Attenuation			55			dB
Group Delay		$t_{GD}$		$2.5/f_s$		s

#### Digital Input Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Input High-Level Voltage	$V_{IH}$	$0.7 \times V_{DD}$			V
Input Low-Level Voltage	$V_{IL}$			0.6	V
Input Leakage Current	$I_{in}$		0.02		$\mu A$
Input Capacitance			3	8	pF

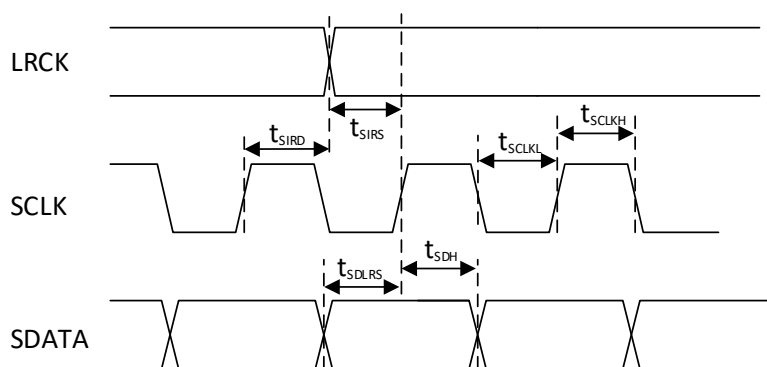
#### Power Dissipation

Parameters		Symbol	3.3V			Unit
			Min	Typ	Max	
Power Supply Current	Normal Operation	$I_A$		16	25	mA
	Power Down state	$I_A$		100		$\mu A$
Power Supply Rejection Ratio	1kHz	PSRR		70		dB
	60Hz	PSRR		50		dB

### Switching Characteristics (Serial Interface)

Parameters		Symbol	Min	Typ	Max	Unit
MCLK Frequency			2		50	MHz
MCLK Duty Cycle			45		55	%
Input Sample Rate (MCLK/LRCK)	256x,384x,1024x	$f_s$	8		50	kHz
	256x,384x		84		134	kHz
	512x,768x		42		67	kHz
	1152x		30		34	kHz
	128x,192x		50		100	kHz
	64x,96x		100		200	kHz
	128x,192x		168		200	kHz
LRCK Duty Cycle			45	50	55	%
SCLK Pulse Width Low		$t_{SCLKL}$	20			ns
SCLK Pulse Width High		$t_{SCLKH}$	20			ns
SCLK Duty Cycle			45	50	55	%
SCLK Rising Edge to LRCK Edge Delay		$t_{SLRD}$	20			ns
SCLK Rising Edge to LRCK Edge Setup Time		$t_{SLRS}$	20			ns
SDIN Valid to SCLK Rising Edge Setup Time		$t_{SDLRS}$	20			ns
SCLK Rising Edge to SDIN Hold Time		$t_{SDH}$	20			ns

### External Serial Interface Input Timing



## FUNCTIONAL DESCRIPTION

The MS4344 receives standard audio sampling frequency, including 48, 44.1, 32kHz in QSM mode, 96, 88.2, 64kHz in DSM mode, 192, 176.4, 128kHz in SSM mode. Audio data is entered through serial input data terminal (SDIN). LRCK determines the channel of the current input data. A serial clock is a clock where audio data enters the input data cache.

### Master Clock

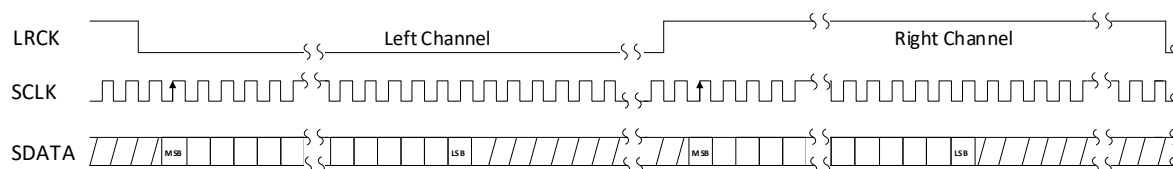
The MCLK/LRCK ratio must be an integer, as shown in table1 below. The frequency of LRCK is equal to the frequency  $f_s$  of input data for each channel. The ratio of MCLK to LRCK and the speed mode are decided during initialization by calculating the number of MCLK cycles and the value of MCLK within one LRCK period. A built-in divider will produce a proper clock. The following table lists some of the audio sampling frequencies, along with the corresponding MCLK and LRCK frequencies. Note that although there is no phase requirement, the LRCK and MCLK must be synchronized.

Table 1. Clock Frequencies

Mode	LRCK	MCLK(MHz)					
	(kHz)	128x	256x	384x	512x	768x	1024x
QSM	32	-	8.192	12.288	16.384	24.576	32.768
	44.1	5.6448	11.2896	16.9344	22.5792	33.868	45.158
	48	6.144	12.288	18.432	24.576	36.864	49.152
DSM	64	8.192	16.384	24.576	32.768	49.152	-
	88.2	11.2896	22.5792	33.868	45.1584	-	-
	96	12.288	24.576	36.864	49.152	-	-
SSM	128	24.576	32.768	49.152	-	-	-
	176.4	22.5792	45.1584	-	-	-	-
	192	24.576	49.152	-	-	-	-

### Serial Input Clock

When 16 rising edge pulses are detected continuously on SCLK terminal during one LRCK cycle, an external serial input clock is entered.



I<sup>2</sup>S, up to 24-bit data Data, Valid on the rising edge of SCLK

Data Format (I<sup>2</sup>S)

### Initialization and Power-Down

When system is initially powered up, it enters the power-down state. At this time, the interpolation filter and  $\Delta$ - $\Sigma$  modulator are reset. The internal reference voltage, digital-to-analog converter, switched-capacitor filter, and low-pass filter are shut down until system detects MCLK and LRCK clocks. Once MCLK and LRCK are detected, system starts to calculate the ratio of MCLK to LRCK, then powers up the internal reference voltage, and finally powers up the digital-to-analog converter, the switched-capacitor filter, and outputs the quiescent voltage VQ.

### Power Up

The DC level on the output terminal is provided by the VQ pin, which is low-level when system is initially powered up. After MCLK is applied, VQ generates a normal DC voltage. The start-up time is 400ms when a 10 $\mu$ F capacitor terminated to VQ pin.

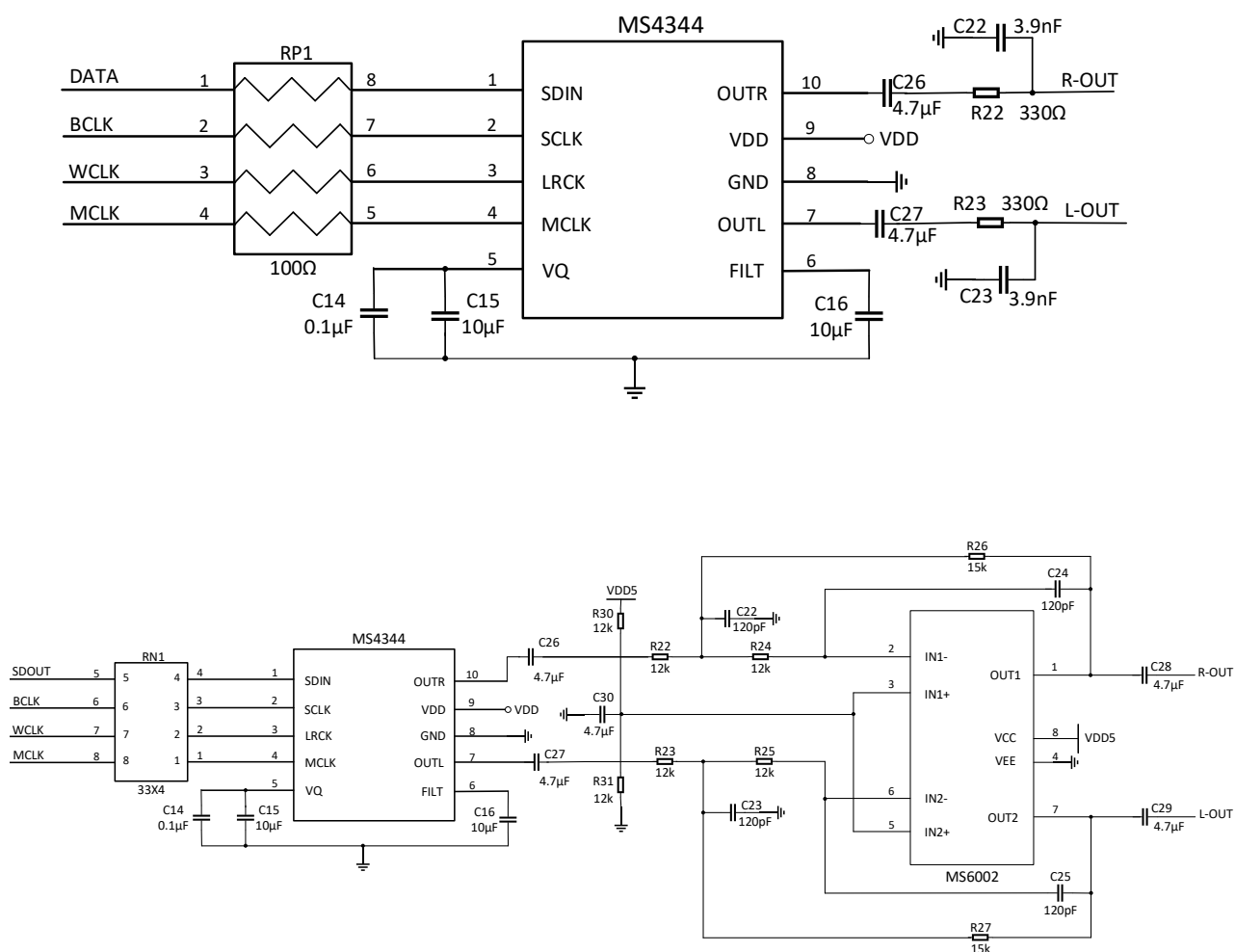
### Power Down

To prevent transient pulses on the output terminal during power down, a 10 $\mu$ F capacitor is connected to the VQ pin.

### Ground and Power Supply Decouple

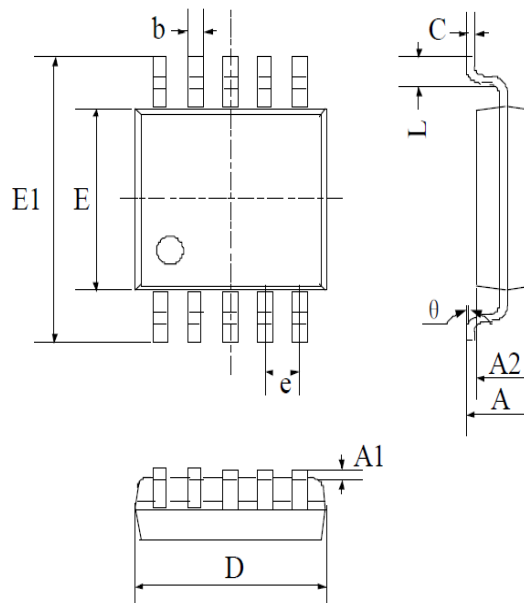
Be careful with the connection of ground and power to achieve ideal performance. For best performance, the decoupling and filter capacitors must be placed as close as possible to the chip.

## TYPICAL APPLICATION



# PACKAGE OUTLINE DIMENSIONS

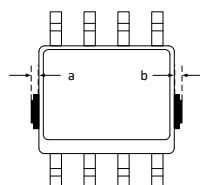
## MSOP10



Symbol	Dimensions in Millimeters	
	Min	Max
A	0.800	1.200
A1	0.000	0.200
A2	0.760	0.970
b	0.30 TYP	
c	0.152 TYP	
D	2.900	3.100
e	0.50 TYP	
E	2.900	3.100
E1	4.700	5.100
L	0.410	0.650
θ	0°	6°

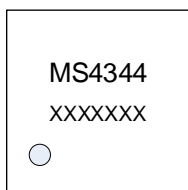
Note: In addition to the package size, a and b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.



## MARKING and PACKAGING SPECIFICATION

### 1. Marking Drawing Description



Product Name: MS4344

Product Code: XXXXXXX

### 2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

### 3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS4344	MSOP10	3000	1	3000	8	24000

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**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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