LVDS Quad CMOS Receiver

PRODUCT DESCRIPTION

The MS90C032/MS90C032T is a low power dissipation, high data rate, quad CMOS differential LVDS signal receiver. The main function is receiving low voltage (350mV) differential signals and translating them to CMOS (compatible with TTL) output voltage. The MS90C032/MS90C032T also supports input open-circuit, short-circuit, fault biasing and tri-state functions. The MS90C032 is available in SOP16 package and the MS90C032T is available in TSSOP16 package.

The MS90C032/MS90C032T and the MS90C031 driver can provide high-speed point-to-point interface applications.

SOP16

TSSOP16

FEATURES

- More than 155.5Mbps (77.7MHz) Switch Frequency
- Low Power Dissipation
- the Maximum 600ps Channel Propagation Delay Difference
- the Maximum 6.0ns Propagation Delay
- Support Input Open-circuit State
- Support Input Short-circuit and Fault Biasing
- Compatible with IEEE 1596.3 SCI LVDS, ANSI Standard
- Compatible with TIA/EIA-644 LVDS Standard
- Apply to SMD5962-95834 Standard
- SOP16, TSSOP16 Package

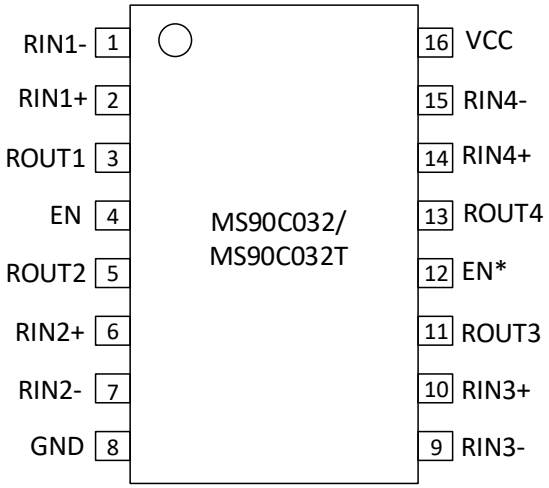
APPLICATIONS

- Flat Panel Display Interface
- High-speed Data Communication
- Monitor Camera

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS90C032	SOP16	MS90C032
MS90C032T	TSSOP16	MS90C032T

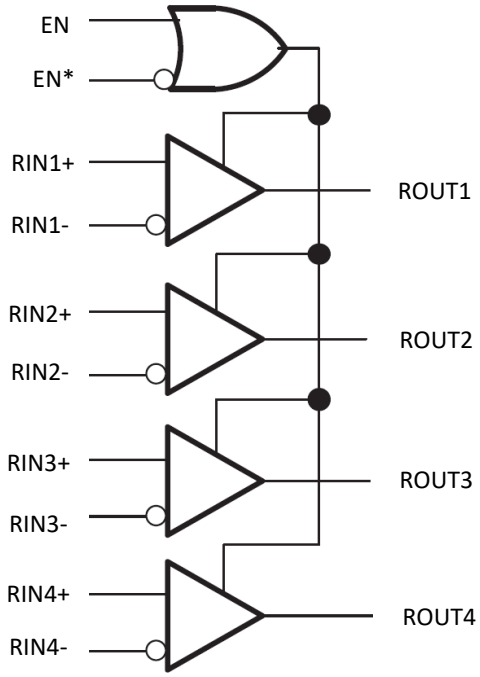
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	RIN1-	I	Channel 1 Negative Input
2	RIN1+	I	Channel 1 Positive Input
3	ROUT1	O	Channel 1 Signal Output
4	EN	I	Enable Positive Input
5	ROUT2	O	Channel 2 Signal Output
6	RIN2+	I	Channel 2 Positive Input
7	RIN2-	I	Channel 2 Negative Input
8	GND	-	Ground
9	RIN3-	I	Channel 3 Negative Input
10	RIN3+	I	Channel 3 Positive Input
11	ROUT3	O	Channel 3 Signal Output
12	EN*	I	Enable Negative Input
13	ROUT4	O	Channel 4 Signal Output
14	RIN4+	I	Channel 4 Positive Input
15	RIN4-	I	Channel 4 Negative Input
16	VCC	-	Power Supply

BLOCK DIAGRAM



Function Table

Enable		Input	Output
EN	EN*	(RIN+)-(RIN-)	Rout
L	H	X	Z
Other Condition		VID ≥0.1V	H
		VID ≤-0.1V	L
		Other	H

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VCC	-0.3 ~ 6	V
Input Voltage	RIN+, RIN−	-0.3 ~ VCC+0.3	V
	EN,EN*	-0.3 ~ VCC+0.3	V
Output Voltage	Rout	-0.3 ~ VCC+0.3	V
Maximum Junction Temperature		+150	°C
Storage Temperature	T_{stg}	-60 ~ 150	°C
ESD (HBM)		≥ 3500	V
ESD (EIAJ)		≥ 250	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	VCC	2.5	5	5.5	V
Input Voltage		GND		2.4	V
Operating Temperature		-40	25	125	°C

ELECTRICAL CHARACTERISTICS

All in the power supply and operating temperature ranges, see Note 1.

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Differential Input High Threshold Voltage	V_{TH}	Vcm=+1.2V				+100	mV
Differential Input Low Threshold Voltage	V_{TL}			-100			mV
Input Current	I_{IN}	Vin=2.4V	VCC=5.0V	-10	±1	+10	μA
		Vin=0V		-10	±1	+10	μA
		Vin=2.4V	VCC=3.3V	-10	±1	+10	μA
		Vin=0V		-10	±1	+10	μA
Output High Voltage	V_{OH}	I_{OH} = −0.4mA, VID = +200 mV,VCC=5.0V		3.8	4.9		V
		I_{OH} = −0.4mA, Input terminal, VCC=5.0V		3.8	4.9		V
		I_{OH} = −0.4mA, VID = +200 mV, VCC=3.3V		3	3.2		V
		I_{OH} = −0.4mA, Input terminal, VCC=3.3V		3	3.2		V
Output Low Voltage	V_{OL}	I_{OL} = 2mA, VID = −200mV,VCC=5.0V			0.07	0.3	V
		I_{OL} = 2mA, VID = −200mV,VCC=3.3V			0.08	0.3	V
Output Short-circuit Current [6]	I_{OS}	Enabled, Vout = 0V, VCC=5.0V		-100	-60	-15	mA
		Enabled, Vout = 0V, VCC=3.3V		-100	-25	-15	mA
Output Tri-state Current	I_{OZ}	VCC=5.0V, Disabled, Vout = 0V or VCC		-10	±1	+10	μA
		VCC=3.3V, Disabled, Vout = 0V or VCC		-10	0	+10	μA
Input High Voltage	V_{IH}	VCC=5.0V	EN	2.0			V
		VCC=3.3V	EN*	1.5			V
Input Low Voltage	V_{IL}	VCC=5.0V	EN			0.8	V
		VCC=3.3V	EN*			0.7	V
Input Current	I_I	VCC=5.0V	EN	-10	±1	+10	μA
		VCC=3.3V	EN*	-10	±1	+10	μA

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Input Clamp Voltage	V_{CL}	I_{CL} = −18mA, VCC=5.0V	EN	-1.5	-0.8		V
		I_{CL} = −18mA, VCC=3.3V	EN*	-1.5	-0.8		V
No-load Operating Current	I_{CC}	EN, EN* = VCC or GND, Input open-circuit, VCC=5.0V	VCC		3.5	10	mA
		EN, EN* = VCC or GND, Input open-circuit, VCC=3.3V	VCC		3	10	mA
No-load Static Current	I_{CCZ}	EN = GND, EN* = VCC, Input open-circuit, VCC=5.0V	VCC		3.7	10	mA
		EN = GND, EN* = VCC, Input open-circuit, VCC=3.3V	VCC		3	10	mA

Switch Characteristic 1

VCC = +5.0V, TA = +25°C, Note 2, 3 ,4, 7

Parameter		Symbol	Condition	Min	Typ	Max	Unit
High to Low Propagation Delay		t_{PHLD}	CL=5pF, VID=200mV (Figure 1 and Figure 2)	1.50	3.40	5.0	ns
Low to High Propagation Delay		t_{PLHD}		1.50	3.48	5.0	ns
Delay Difference | t_{PHLD}−t_{PLHD} |		t_{SKD}		0	80	600	ps
Channel Propagation Delay Difference		t_{SK1}		0	0.6	1.0	ns
Rise Time		t_{TLH}			0.5	2.0	ns
Fall Time		t_{THL}			0.5	2.0	ns
Propagation Delay	High to Hi-Z	t_{PHZ}	CL=10pF, RL=2kΩ (Figure 3 and Figure 4)		10	15	ns
	Low to Hi-Z	t_{PLZ}			10	15	ns
	Hi-Z to High	t_{PZH}			4	10	ns
	Hi-Z to Low	t_{PZL}			4	10	ns

Switch Characteristic 2

VCC = +5.0V±10%, TA = -40 to +85°C, Note 2, 3, 4, 5, 7

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High to Low Propagation Delay	t_{PHLD}	CL=5pF, VID=200mV (Figure 1 and Figure 2)	1.0	3.40	6.0	ns
Low to High Propagation Delay	t_{PLHD}		1.0	3.48	6.0	ns
Propagation Delay Difference | t_{PHLD}−t_{PLHD} |	t_{SKD}		0	0.08	1.2	ns

Channel Propagation Delay Difference		t_{SK1}		0	0.6	1.5	ns
Chip Propagation Delay Difference		t_{SK2}				5.0	ns
Rise Time		t_{TLH}			0.5	2.5	ns
Fall Time		t_{THL}			0.5	2.5	ns
Propagation Delay	High to Hi-Z	t_{PHZ}	CL=10pF, RL=2kΩ (Figure 3 and Figure 4)		10	20	ns
	Low to Hi-Z	t_{PLZ}			10	20	ns
	Hi-Z to High	t_{PZH}			4	15	ns
	Hi-Z to Low	t_{PZL}			4	15	ns

Note:

1. The current flowing into device is defined as positive current. The current flowing out of device is defined as negative current. The voltage values shown in table are all relative to ground.

2. All typical values are measured at VCC =+5.0V, TA=+25°C.

3. The waveforms of test circuit are: for input LVDS signal, f=1MHz,ZO=50Ω,tr and tf (0%–100%)≤ 1ns; For enable signals, EN and EN*, tr and tf≤6ns.

4. Channel propagation delay difference is the propagation delay difference between differential channels for the same one input signal.

5. Chip propagation delay difference is the propagation delay difference between differential chips for the same one input signal.

6. Output short-circuit current (I_{OS}), the value is magnitude and minus is current direction. In order to ensure operating in maximum junction temperature, only one channel output is shorted at a time.

7. Load capacitance includes probe and soldering capacitance.

Test Circuit

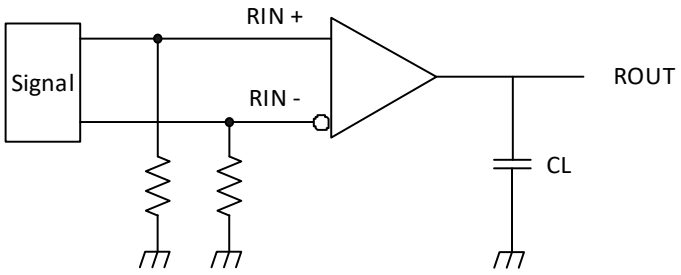


Figure 1. Propagation Delay and Edge Transition Time Test Circuit

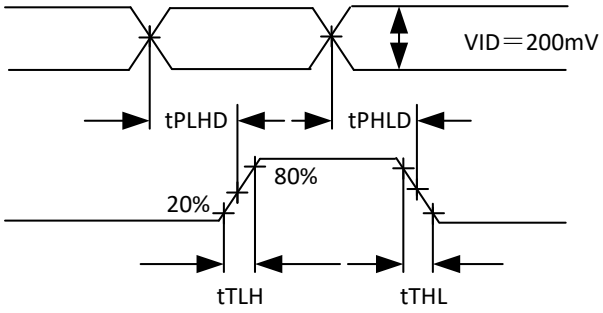


Figure 2. Propagation Delay and Edge Transition Time Waveforms

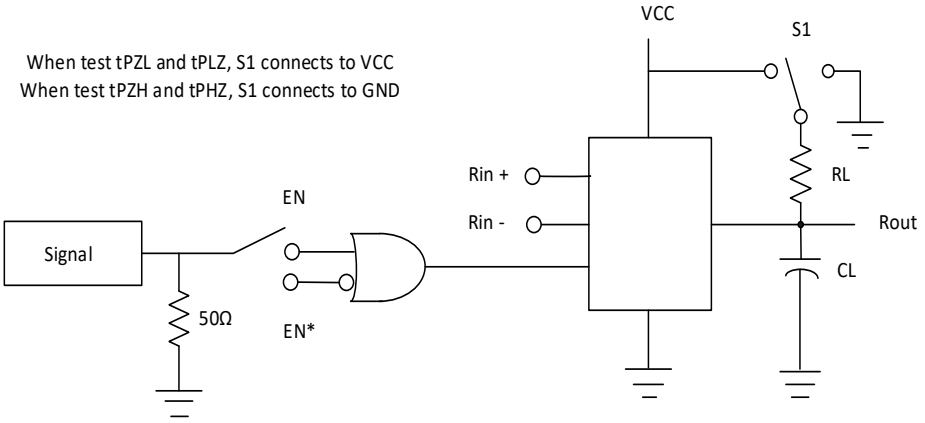


Figure 3. Tri-state Delay Test Circuit

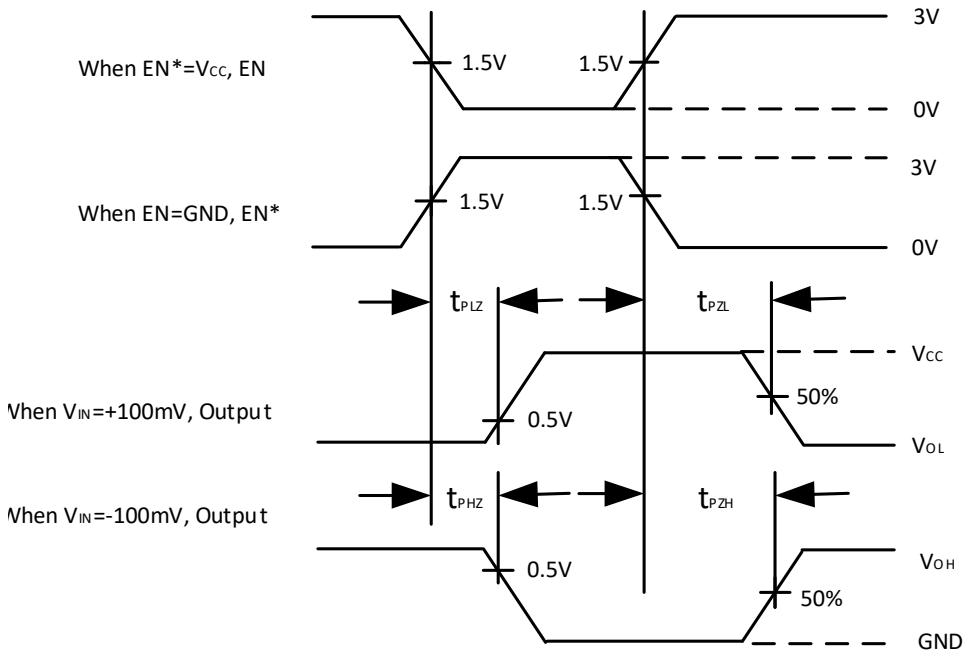
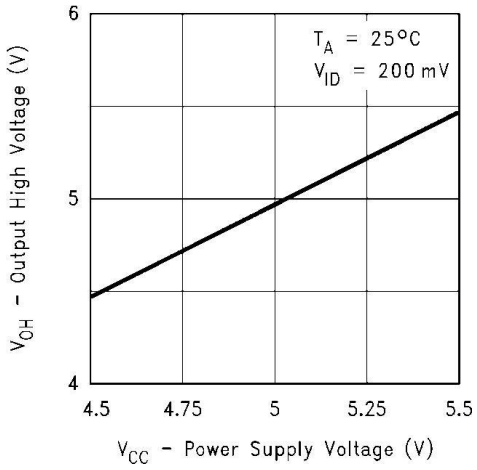
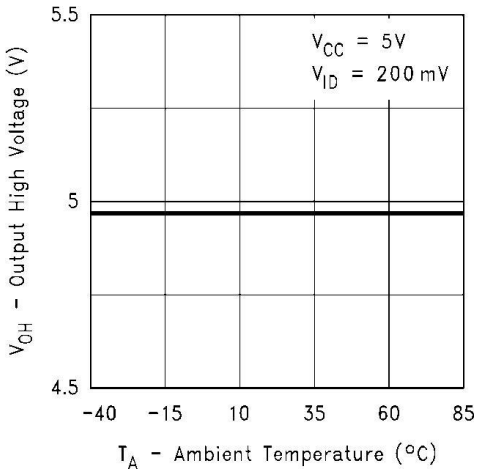


Figure 4. Tri-state Propagation Waveforms

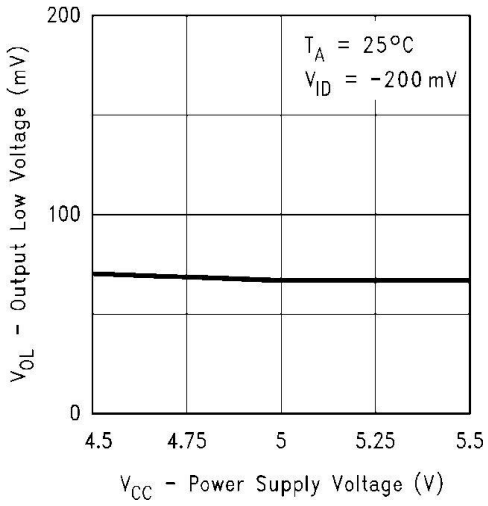
TYPICAL CHARACTERISTICS CURVES



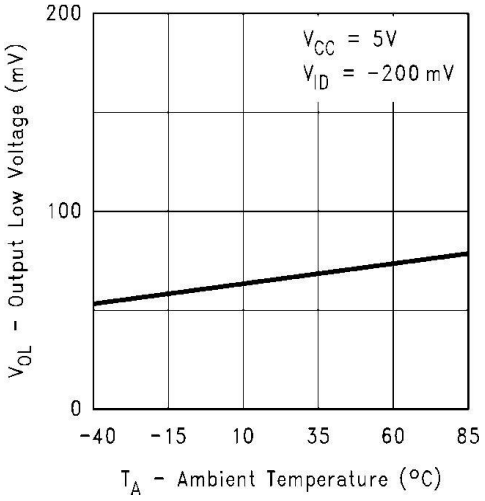
Output High Voltage VS. Power Supply



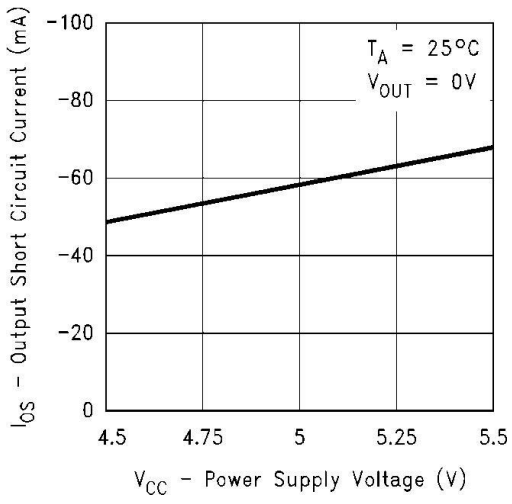
Output High Voltage VS. Temperature



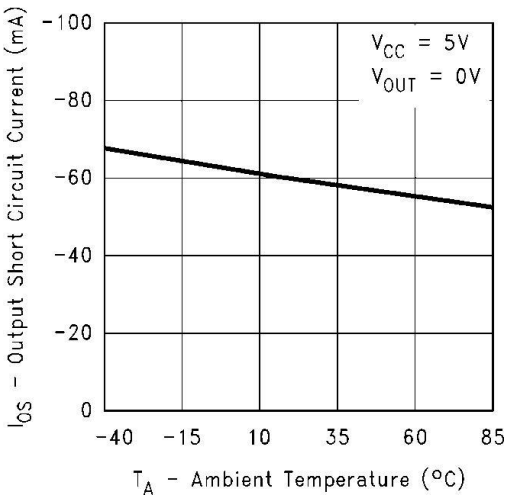
Output Low Voltage VS. Power Supply



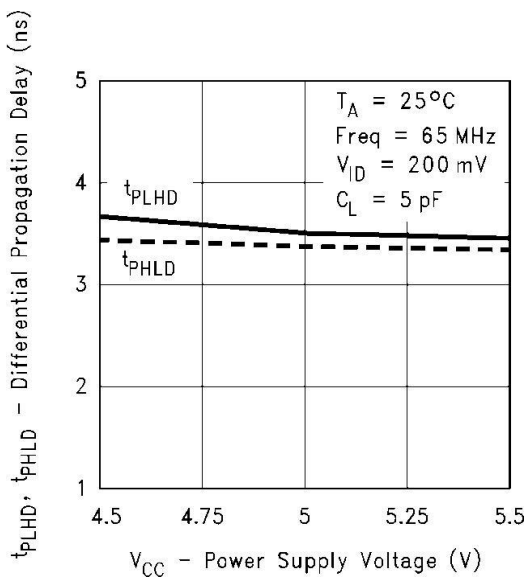
Output Low Voltage VS. Temperature



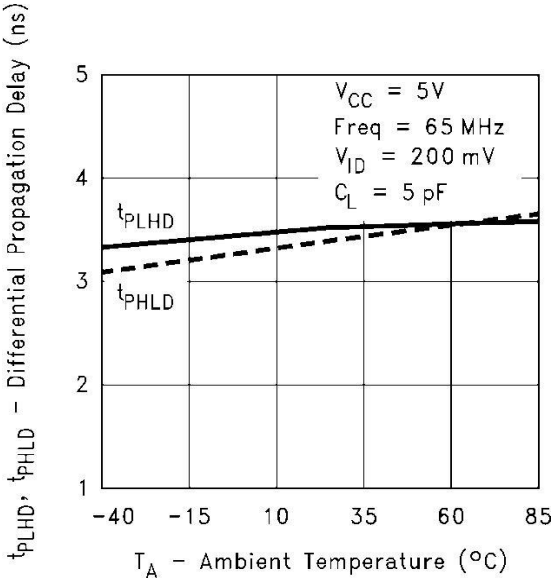
Output Short-circuit Current VS. Power Supply



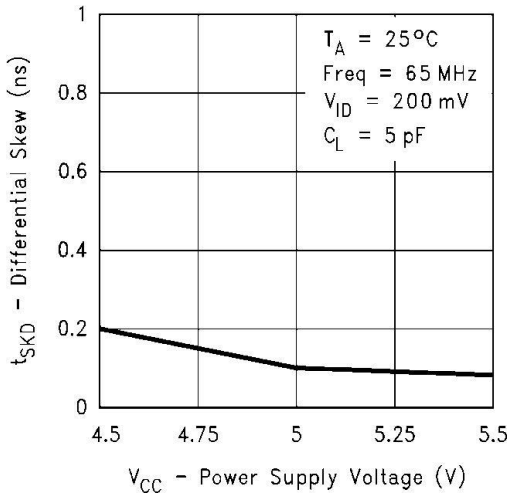
Output Short-circuit Current VS. Temperature



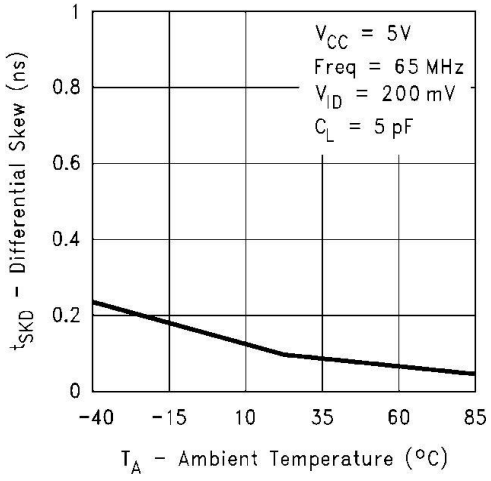
Differential Propagation Delay VS. Power Supply



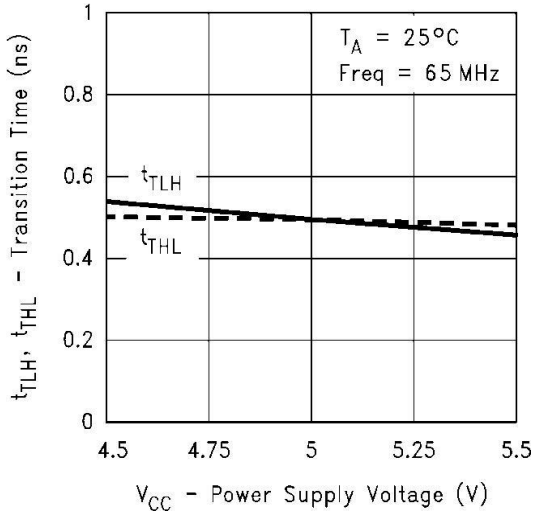
Differential Propagation Delay VS. Temperature



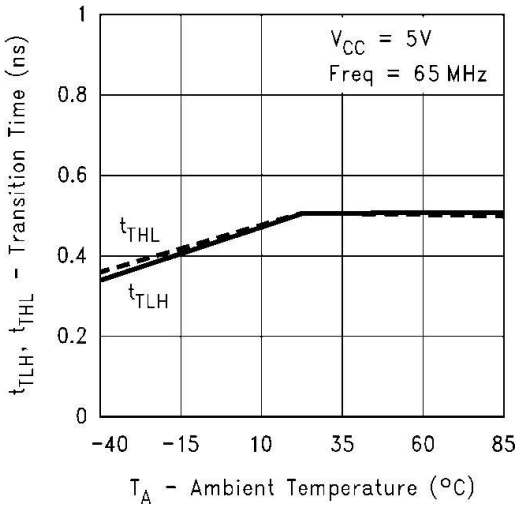
Differential Skew VS. Power Supply



Differential Skew VS. Temperature



Transition Time VS. Power Supply



Transition Time VS. Temperature

TYPICAL APPLICATION DIAGRAM

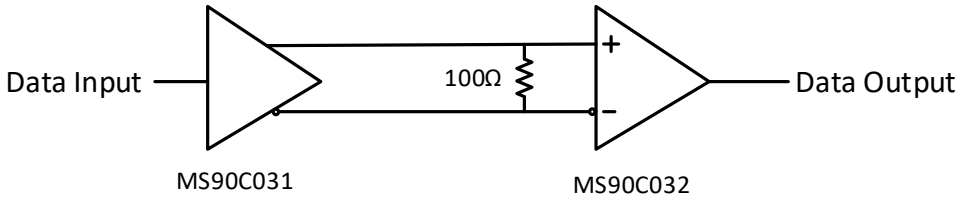


Figure 5. Typical Application Diagram

LVDS driver and receiver are mainly applied to simple point-to-point structure as shown in Figure 5. The structure provides a clean transmission channel for high-speed data rate signal. Transmission media can be twisted-pair, cable and PCB trace. The impedance of typical transmission media is less than 100Ω. In order to match the impedance of transmission media, 100Ω terminal resistor can be connected on differential input terminals. And it should be as close to the input terminal of the device as possible. The terminal resistor converts the current signal to voltage signal, thus to provide for the MS90C032/MS90C032T. For other structures, such as multi-receiver, it should be considered that the impedance match of mid connector and cable interface and noise margin.

The MS90C032/MS90C032T can detect differential LVDS signal, the magnitude of which ranges from 100mV to ±1V and the common-mode point of which is near 1.2V. The input voltage range of differential input terminals is 0V to 2.4V. If exceed the voltage range, ESD protection circuit may be triggered and then clamp the bus voltage.

Receiver Fail-safe State: the LVDS receiver, the MS90C032/MS90C032T is a high-peed, high-gain device, which can magnify the differential low-voltage signal (20mV) as CMOS logic level. Due to the high gain, the effect of noise magnitude on input terminal must be considered. Internal circuit sets protection circuit to make output high-level for receiver fail-safe state, input open-circuit, short-circuit and fault biasing.

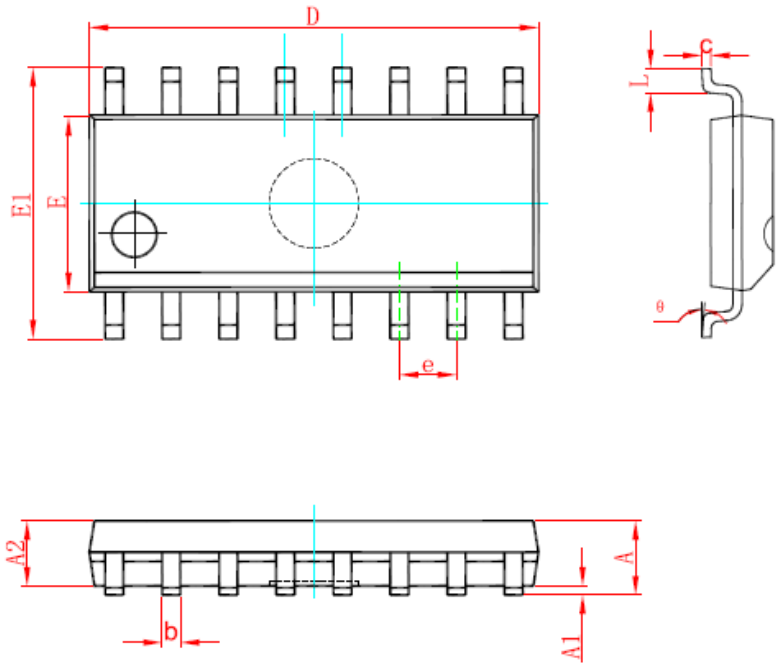
1. Input Open-circuit: The MS90C032/MS90C032T is quad receiver. When only one channel is used, the input terminals of other channels should be in open-circuit state.

2. Input Terminated: When LVDS driver is in tri-state or power-down state, the input termianl of the MS90C032/MS90C032T is equivalent to 100Ω resistor shorted. And the output is high-level at this time; When driver is open, bus cable is floating and considered as antenna with capturing noise. And noise voltage would appear on receiver input terminal. When the noise magnitude is more than 10mV, receiver will translate noise to logic level. Therefore, in order to translate noise to common-mode signal, it is recommended to use balanced transmission media, such as twisted pair cable.

3. Input Shorted Directly: When the input terminal of receiver is directly shorted, output is still high-level. This is only applicable to the condition where there is no external common-mode level.

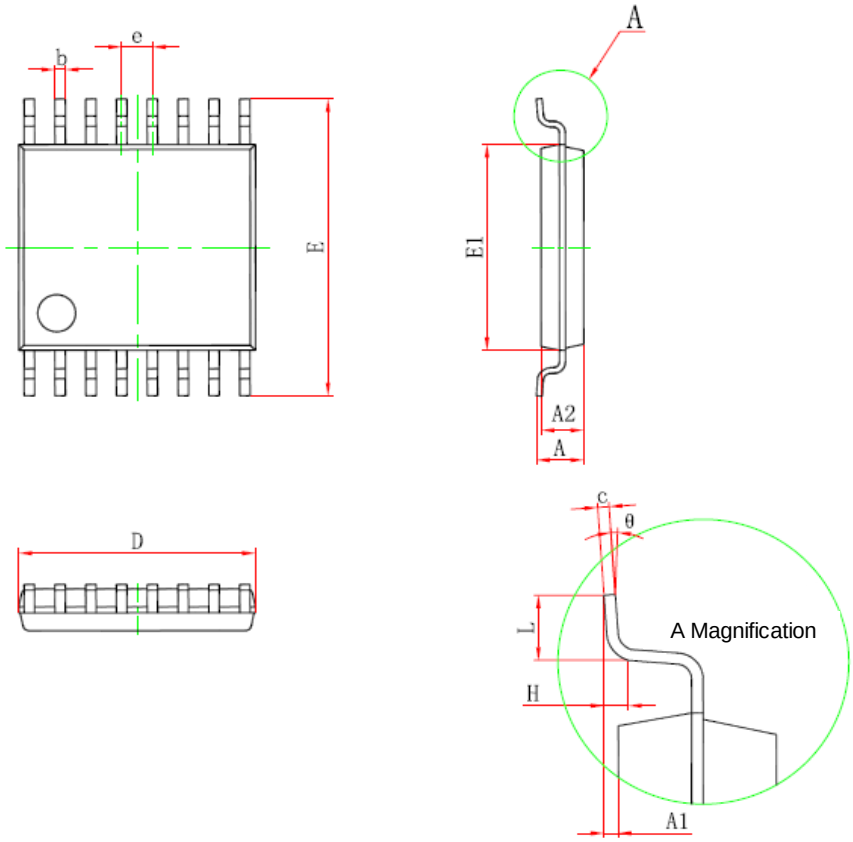
PACKAGE OUTLINE DIMENSIONS

SOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

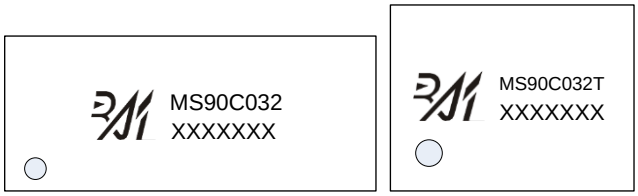
TSSOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.246	0.258
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	4.300	4.500	0.169	0.177
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.400	1.270	0.016	0.050
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name : MS90C032, MS90C032T

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS90C032	SOP16	2500	1	2500	8	20000
MS90C032T	TSSOP16	3000	1	3000	8	24000

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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