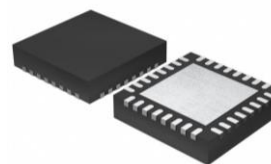


## 24-bit, 192kHz, Asynchronous Sample Rate Converter with Integrated Digital Audio Receiving Interface

### PRODUCT DESCRIPTION

The MS8422N is a 24-bit and high-performance asynchronous sampling rate converter, which integrates digital audio interface receiver and supports IEC60958, S/PDIF, EIAJ CP1201 and AES3 interface standards. The audio data inputs from audio interface receiver or three-wire serial audio input port and outputs from 2 three-wire serial audio output ports. In software or hardware mode, the MS8422N can be controlled by the control port.



QFN32

### FEATURES

- SPI or I<sup>2</sup>C Software Mode and Stand-alone Hardware Mode
- Flexible 3-wire Digital Serial Audio Input Port
- Two Serial Audio Outputs with Independent Data Path Selection
- All Serial Audio Ports Support Master-slave Mode
- Time Division Multiplexing Mode(TDM)
- 4 General Purpose Outputs(GPO)
- +3.3V Analog Supply Voltage(VA)
- +1.8V-5.0V Digital Interface Voltage(VL)
- IEC60958, S/PDIF, EIAJ CP1201 and AES3 Protocols Compatible
- 28kHz to 216kHz Sampling Frequency Range
- 2:1 Differential AES3 or 4:1 S/PDIF Input Multiplexer
- Low Jitter Clock Recovery
- No External PLL Filter Required
- Selectable and Automatic Clock Switching
- On-chip Channel State Data Buffer
- Automatically Detect Compressed Input Audio Data Streams
- Decode CD Q Sub-Code
- 140dB Dynamic Range
- -120 dB THD+N

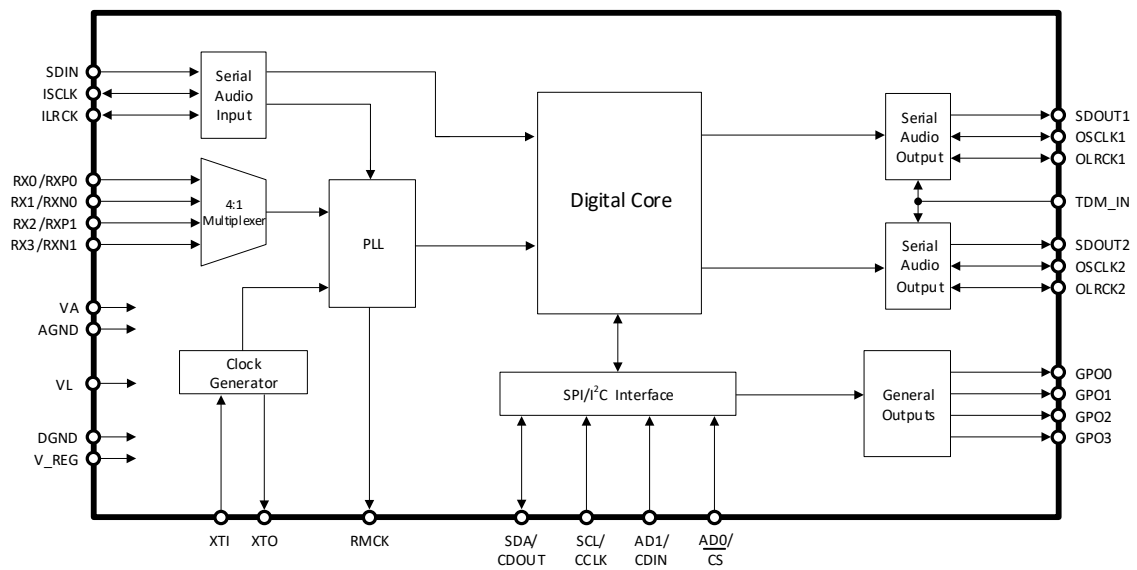
### APPLICATIONS

- Digital Recording System
- Digital Mixing Console
- High-performance Analog-to-digital Converter
- Digital Audio Processor

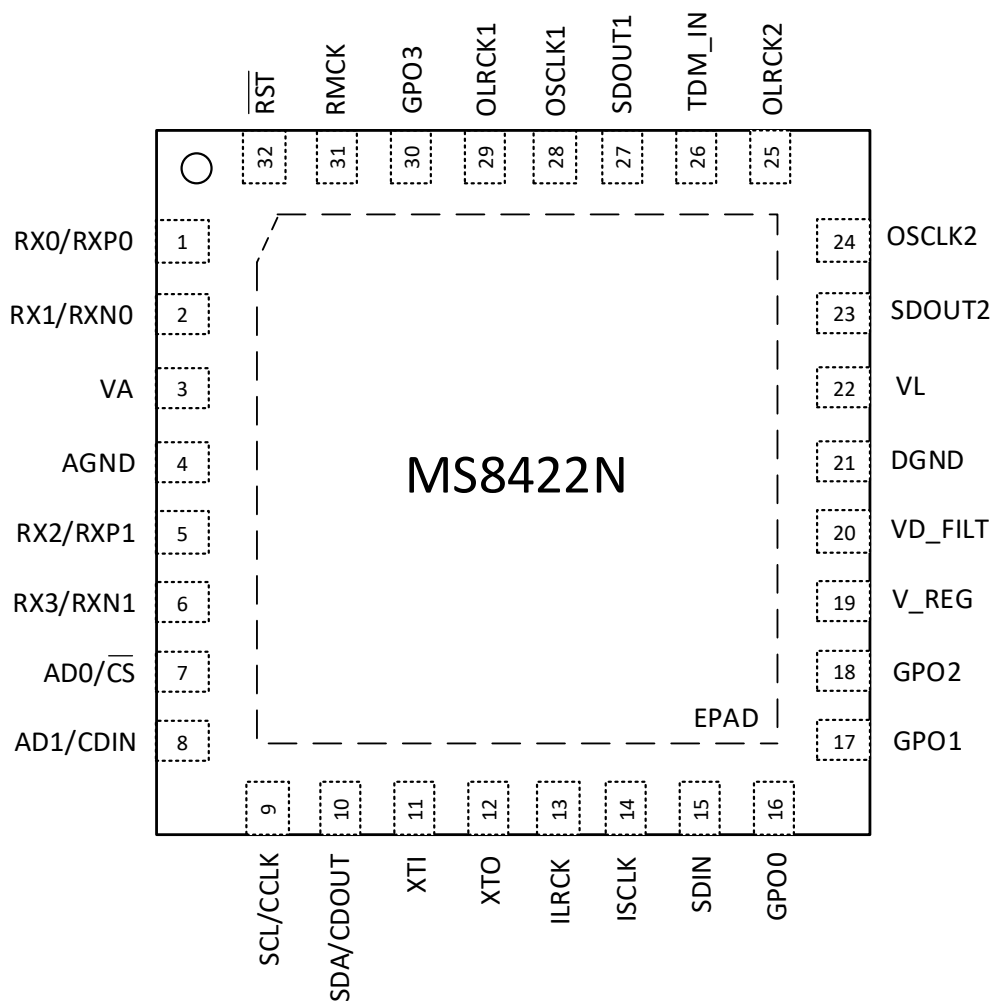
### PRODUCT SPECIFICATION

Part Number	Package	Marking
MS8422N	QFN32	MS8422N

## BLOCK DIAGRAM



## PIN CONFIGURATION-SOFTWARE MODE

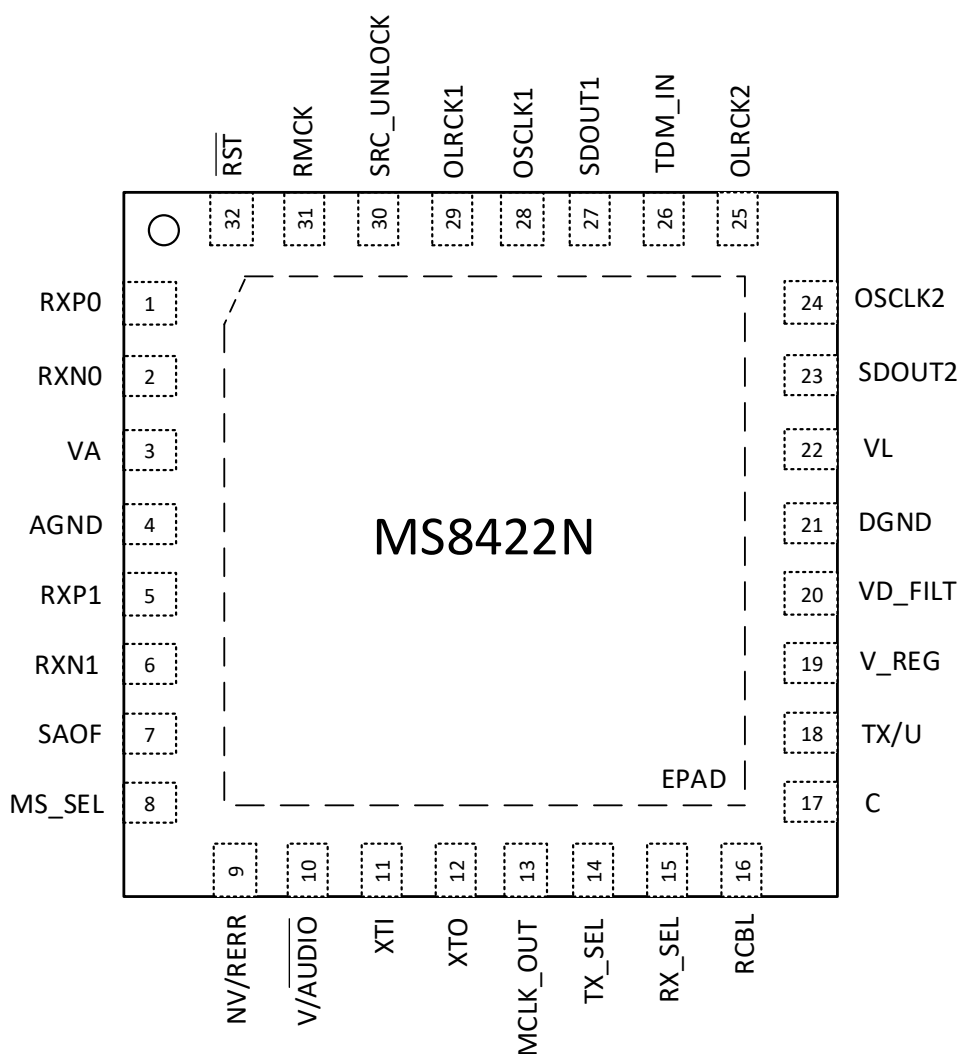


## PIN DESCRIPTION-SOFTWARE MODE

Pin	Name	Type	Description
1 2 5 6	RX[3:0], RXP/RXN[1:0]	I	AES3/SPDIF Input. Single-ended or differential receiver. Input AES3 or S/PDIF encoded digital data. RX[3:0] contains single-ended multiplexer. RXP[1:0] contains non-inverting inputs of the differential input multiplexer. And RXN[1:0] contains inverting inputs of the differential input multiplexer.
3	VA	I	Analog Power Supply, Typically +3.3V. The power supply noise should be as small as possible, because power noise will directly affect the jitter performance of the recovered clock.
4	AGND	-	Analog Ground, The Ground of the Analog Circuit inside the Chip. The AGND and the DGND must be connected to the same ground.
7	AD0/ $\overline{CS}$	I	Address Bit 0 (I <sup>2</sup> C)/Chip Select(SPI). A falling edge on this pin makes the MS8422N in SPI mode after reset. If there is no falling edge, the MS8422N defaults to I <sup>2</sup> C mode. In I <sup>2</sup> C mode, AD0 is the chip address pin. In SPI mode, $\overline{CS}$ is used to enable the SPI digital interface . See "Control Port Description" for more details.
8	AD1/CDIN	I	Address Bit 1 (I <sup>2</sup> C)/Serial Control Data Input(SPI). In I <sup>2</sup> C mode, AD1 is the chip address pin. In SPI mode, CDIN is the data input pin of the SPI interface.
9	SCL/CCLK	I	Digital Interface Clock. Serial control interface clock.
10	SDA/CDOUT	I/O	Serial Data I/O (I <sup>2</sup> C)/Data Output(SPI). In I <sup>2</sup> C mode, SDA is I <sup>2</sup> C data line. In SPI mode, CDOUT is data output pin of SPI interface.
11	XTI	I	Crystal/Oscillator Input Crystal or Digital Clock as the Master Clock Input.
12	XTO	O	Crystal Output. Master Clock Output.
13	ILRCK	I/O	Serial Audio Input Left/Right Clock, Word Clock of Audio Data on the SDIN Pin.
14	ISCLK	I/O	Serial Audio Input Bit Clock, Serial Bit Clock of Audio Data on the SDIN Pin.
15	SDIN	I	Serial Audio Input Data Terminal, Audio Data Serial Input Pin.

Pin	Name	Type	Description
16 17 18 30	GPO[3:0]	O	Configurable General Purpose Outputs. In I <sup>2</sup> C mode, connecting a 20kΩ pull-up resistor on the GPO2 pin to VL will set AD2 chip address bit to 1, otherwise AD2 will be 0.
19	V_REG	I	Core, Register Power Supply Input, Typically +3.3V。
20	VD_FILT	O	Regulator Voltage Output. A 10μF capacitor must be connected to the digital ground. It cannot be used as an external voltage source.
21	DGND	I	Digital Logic and I/O Ground. The AGND and DGND must be connected to the same ground.
22	VL	I	Logic Input/Output Power Supply. Typical values are +1.8V, +2.5V, +3.3V.
23	SDOUT2	O	Serial Audio Output 2 Data Terminal, Audio Data Serial Output 2 Pin.
24	OSCLK2	I/O	Serial Audio Output 2 Bit Clock, Serial Bit Clock of Audio Data on the SDOUT2.
25	OLRCK2	I/O	Serial Audio Output 2 Left/Right Clock, Word Rate Clock of Audio Data on the SDOUT2.
26	TDM_IN	I	TDM Serial Audio Input, Serial Audio Data Input. It must be connected to the ground when not used.
27	SDOUT1	O	Serial Audio Output 1 Data Terminal, Audio Data Serial Output 1 Pin.
28	OSCLK1	I/O	Serial Audio Output 1 Bit Clock, Serial Bit Clock of Audio Data on the SDOUT1.
29	OLRCK1	I/O	Serial Audio Output 1 Left/Right Clock, Word Rate Clock of Audio Data on the SDOUT1.
31	RMCK	O	Recovered Master Clock for SPDIF/AES3, Master Clock Recovered from PLL. The frequency is 128x, 192x, 256x, 384x, 512x, 768x or 1024xFs, where Fs is the sample rate of the input SPDIF/AES3 data or ISCLK/64.
32	$\overline{\text{RST}}$	I	Reset Input. When $\overline{\text{RST}}$ is low, the MS8422N enters low power-dissipation mode and all internal states are reset. $\overline{\text{RST}}$ must keep in low level until the power supply, all input clock frequencies and phases are stable.
-	EPAD	-	Thermal Pad. It should be connected to the ground for heat dissipation.

PIN CONFIGURATION-HARDWARE MODE



## PIN DESCRIPTION-HARDWARE MODE

Pin	Name	Type	Description
1 2 5 6	RXP/RXN[1:0]	I	AES3/SPDIF Input, Differential receiver inputs AES3 or S/PDIF encoded digital data. RXP[1:0] contains non-inverting inputs of the differential input multiplexer. RXN[1:0] contains the inverting inputs of the differential input multiplexer. Useless inputs should be connected to the AGND.
3	VA	I	Analog Power Supply, Typically +3.3V. The power supply noise should be as small as possible, because power noise will directly affect the jitter performance of the recovered clock.
4	AGND	I	Analog Ground, The Ground of the Analog Circuit inside the Chip. The AGND and the DGND must be connected to the same ground.
7	SAOF	I	Serial Audio Output Format Select. When $\overline{RST}$ is released to select serial audio output format.
8	MS_SEL	I	Master/Slave Mode Select. when $\overline{RST}$ is released to select the master or slave mode of serial audio output terminal.
9	NV/RERR	O	Invalid Input/Receiver Error, Receiver Error Indication. The default output is NVERR. When a 20k $\Omega$ pull-up resistor is connected to VL, RERR is selected.
10	V/ $\overline{\text{AUDIO}}$	O	Valid Data/ $\overline{\text{AUDIO}}$ . In master mode, if this pin is connected with a 20k $\Omega$ pull-down resistor, it will output the serial valid data from the AES3 receiver through the rising and falling edges of OLRCK2. If this pin is connected with a 20k $\Omega$ pull-up resistor, the pin is low when AES3 inputs valid linear PCM data.
11	XTI	I	Crystal/Oscillator Input Crystal or Digital Clock as the Master Clock Input.
12	XTO	O	Crystal Output. Master Clock Output.
13	MCLK_OUT	O	MCLK Buffered Output XTI Clock. If this pin is connected with a 20k $\Omega$ pull-up resistor to VL, the SRC master clock source comes from PLL clock, otherwise it comes from internal ring oscillator.
14	TX_SEL	I	TX Pin Multiplexer Selection, Used to Select the AES3 Receiver Input for Pass-through to the TX Pin.
15	RX_SEL	I	Receiver Multiplexer Selection, Used to Select the AES3 Receiver Valid Input.
16	RCBL	O	Receiver Channel Status Block, Indicate the Beginning of the Channel Status Block. RCBL will go high during each Z preamble following the first detected Z preamble. If the Z preamble code is not detected, the output is uncertain.

Pin	Name	Type	Description
17	C	O	Channel Status Data. In master mode, output channel status data is from the AES3 receiver, sampled by the rising edges and falling edges of OLRCK. In hardware mode, this pin must be connected with a 20kΩ pull-up resistor to VL.
18	TX/U	O	Receiver Multiplex Pass-through/User Data-If there is no 20kΩ pull-up resistor, this pin outputs the receiver multiplex input selected by the TX_SEL pin. In master mode, if a 20kΩ pull-up resistor is connected to VL, this pin outputs serial user data from the AES3 receiver (updated on the rising and falling edges of OLRCK).
19	V_REG	I	Digital Core, Register Power Supply Input, Typically +3.3V.
20	VD_FILT	O	Regulator Voltage Output. A 10μF capacitor must be connected to the digital ground. It cannot be used as an external voltage source.
21	DGND	I	Digital Logic and I/O Ground, Logic and I/O Ground. The AGND and DGND must be connected to the same ground.
22	VL	I	Logic Input/Output Power Supply. Typical values are +1.8V, +2.5V, +3.3V.
23	SDOUT2	O	Serial Audio Output 2 Data Terminal, Audio Data Serial Output 2 Pin.
24	OSCLK2	I/O	Serial Audio Output 2 Bit Clock, Serial Bit Clock of Audio Data on the SDOUT2.
25	OLRCK2	I/O	Serial Audio Output 2 Left/Right Clock, Word Clock of Audio Data on the SDOUT2.
26	TDM_IN	I	TDM Serial Audio Input, Serial Audio Data Input. It must be connected to the ground when not used.
27	SDOUT1	O	Serial Audio Output 1 Data Terminal, Audio Data Serial Output 1 Pin.
28	OSCLK1	I/O	Serial Audio Output 1 Bit Clock, Serial Bit Clock of Audio Data on the SDOUT1.
29	OLRCK1	I/O	Serial Audio Output 1 Left/Right Clock, Word Rate Clock of Audio Data on the SDOUT1.
30	SRC_UNLOCK	O	SRC Unlocked Indication(Output), indicate whether SRC is locked. See "SRC Lock" for more details.
31	RMCK	O	Recovered Master Clock, Master Clock Recovered from PLL. The frequency is 128x, 192x, 256x, 384x, 512x, 768x or 1024xFs, where Fs is the sample rate of the input AES3 data or ISCLK/64. If this pin connects a 20kΩ pull-up resistor to VL, MCLK of SDOUT1 is from RMCK, otherwise it comes from the input clock of XTI-XTO.
32	$\overline{\text{RST}}$	I	Reset Input. When $\overline{\text{RST}}$ is low, the MS8422N enters low power-dissipation mode and all internal states are reset. $\overline{\text{RST}}$ must keep in low level until the power supply, all input clock frequencies and phases are stable.
-	EPAD	-	Thermal Pad. It should be connected to the ground for heat dissipation.



## ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

DGND=AGND =0V, all voltage values are relative to 0V.

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	VL	-0.3 ~ 5	V
	VA	-0.3 ~ 4.5	V
	V_REG	-0.3 ~ 5.2	V
Input Current, Any Pins other than Supplies <sup>1</sup>	I <sub>IN</sub>	±10	mA
Input Voltage Any pins other than RXP[1:0], RXN[1:0] or RX[3:0]	V <sub>IN</sub>	-0.3 ~ VL+0.4	V
Input Voltage RXP[1:0], RXN[1:0] or RX[3:0]	V <sub>IN</sub>	-0.3 ~ VA+0.4	V
Operating Temperature	T <sub>A</sub>	-40 ~ +125	°C
Storage Temperature	T <sub>STG</sub>	-65 ~ +150	°C

Note 1: Transient current of up to 100mA will not cause SCR latch-up.

## RECOMMENDED OPERATING CONDITIONS

GND =0V, all voltage values are relative to 0V.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VL	1.7	3.3	3.6	V
	VA	2.4	3.3	3.6	V
	V_REG	2.2	3.3	3.6	V
Operating Temperature	T <sub>A</sub>	-40		+85	°C

## ELECTRICAL CHARACTERISTICS

### Sample Rate Converter

XTI - XTO=24.576 MHz; Input Signal=1.000 kHz, Measurement Bandwidth=20 - Fso/2Hz, Word Length=24 bit<sup>2</sup>

Parameter	Min	Typ	Max	Unit
Resolution	16		24	bits
Sample Rate				
Slave	XTI/2048		XTI/128	kHz
Master	XTI/512		XTI/128	kHz
Sample Rate Ratio - Up sampling			1:6	Fsi:Fso
Sample Rate Ratio - Down sampling			6:1	Fsi:Fso
Interchannel Gain Mismatch		0.0		dB
Interchannel Phase Deviation		0.0		Degrees
Gain Error	-0.2		0	dB
Peak Idle Channel Noise Component			-144	dBFS
<b>Dynamic Range - Unweighted (997Hz, -60 dBFS Input)</b>				
44.1 kHz: 48 kHz		130		dB
48 kHz: 192 kHz		132		dB
48 kHz: 44.1 kHz		133		dB
48 kHz: 96 kHz		134		dB
96 kHz: 48 kHz		133		dB
<b>Total Harmonic Distortion + Noise (1kHz, -3 dBFS Input)</b>				
44.1 kHz: 48 kHz		-128		dB
48 kHz: 192 kHz		-128		dB
48 kHz: 44.1 kHz		-128		dB
48 kHz: 96 kHz		-134		dB
96 kHz: 48 kHz		-134		dB

Note 2: Fsi is the sample rate of input data. Fso is the sample rate of output data. The data separated by a colon is the ratio of Fsi to Fso.

### DC Electrical Characteristics

AGND=DGND=0V, all voltage values are relative to 0V.

Parameter		Min	Typ	Max	Unit
Power-Down Mode <sup>3</sup>					
Supply Current in power-down mode	VA = 3.3V		3.0		mA
	V_REG = 3.3V		3.1		
	VL = 1.8V		1.0		
	VL = 2.5V		1.7		
	VL = 3.3V		2.4		
Normal operation <sup>4</sup>					
Supply Current at 48 kHz Fsi and Fso	VA = 3.3V		18.8		mA
	V_REG = 3.3V		15.2		
	VL = 1.8V		2.7		
	VL = 2.5V		3.8		
	VL = 3.3V		5.2		
Supply Current at 192 kHz Fsi and Fso	VA = 3.3V		18.9		mA
	V_REG = 3.3V		32.4		
	VL = 1.8V		6.2		
	VL = 2.5V		8.8		
	VL = 3.3V		12		

Note:

3. Power-down mode is to change the register 0x02h to make the chip enter the low power dissipation mode, and then set  $\overline{\text{RST}}$  to low.

4. Normal operation is defined that  $\overline{\text{RST}}$  is high. The typical values were measured with the digital interface receiver in differential mode, where serial audio output port 1 in master mode is sourced by the SRC, and serial audio output port 2 in master mode is sourced by the AES3 receiver output.

### Digital Interface Characteristics

AGND=DGND= 0V, all voltage values are relative to 0V.

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current <sup>5</sup>	I <sub>IN</sub>			+32	μA
Input Capacitance	C <sub>IN</sub>		8		pF
Digital Interface Receiver -RXP[1:0], RXN[1:0], RX[3:0]					
Differential Input Sensitivity, RXP to RXN <sup>6</sup>			200		mVpp
Differential Input Impedance, RXP and RXN to GND			11		kΩ
Single-Ended Input Sensitivity, RX pins, Receiver Input Mode 1 <sup>6</sup>			316		mVpp
Single-Ended Input Impedance, RX pins, Receiver Input Mode 1			11		kΩ
High-Level Input Voltage, RX pins, Digital Mode	V <sub>IH</sub>	0.6×VA		VA+0.3	V
Low-Level Input Voltage, RX pins, Digital Mode	V <sub>IL</sub>	-0.3		0.8	V
Digital Input/Output					
High-Level Output Voltage (I <sub>OH</sub> = -4mA)	V <sub>OH</sub>	0.8×VL			V
Low-Level Output Voltage (I <sub>OL</sub> = -4mA)	V <sub>OL</sub>			0.64	V
High-Level Input Voltage	V <sub>IH</sub>	0.55×VL			V
Low-Level Input Voltage	V <sub>IL</sub>			0.4×VL	V
Input Hysteresis			0.2		V

Note:

5. When a digital signal is sent to the RX pin of AES, the RX\_MODE, RX\_SEL and INPUT\_TYPE bits released from pin  $\overline{\text{RST}}$  to the register 03h is configured as the digital input signal allowed on the driver pin, and pin RX receives 730μA current from the digital signal's supply.

6. The maximum sensitivity refers to AES3-2003.

### Switching Characteristics

Input: Logic 0 = 0 V, Logic 1 = VL; C<sub>L</sub> = 20 pF.

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RST}}$ Pin Low Pulse Width <sup>7</sup>		1			ms
PLL Clock Recovery Sampling Rate Range <sup>8</sup>		28		216	kHz
RMCK Output Jitter <sup>9</sup>	Differential RX Mode		200		ps RMS
	Single-Ended RX Mode		475		
XTI Frequency	Crystal	12		27.000	MHz
	Digital Clock Source	1.024		49.152	
XTI High/Low Pulse Width		9			ns

Parameter	Symbol	Min	Typ	Max	Unit
VL=3.3V, 5V					
RMCK/MCLK_OUT Output Frequency				55.296	MHz
RMCK/MCLK_OUT Output Duty Cycle		45	50	55	%
Slave Mode					
ISCLK Frequency				49.152	MHz
ISCLK High-level Time	t <sub>sckh</sub>	9.2			ns
ISCLK Low-level Time	t <sub>sckl</sub>	9.2			ns
OSCLK Frequency				26.9	MHz
OSCLK High-level Time	t <sub>sckh</sub>	16.7			ns
OSCLK Low-level Time	t <sub>sckl</sub>	16.7			ns
I/OLRCK Edge to I/OSCLK Rising Edge	t <sub>icks</sub>	5.7			ns
I/OSCLK Rising Edge to I/OLRCK Edge	t <sub>ickd</sub>	4.2			ns
OSCLK Falling Edge/OLRCK Edge to SDOUT Output Valid	t <sub>dpd</sub>			15	ns
SDIN/TDM_IN Setup Time before I/OSCLK Rising Edge	t <sub>ds</sub>	3.6			ns
SDIN/TDM_IN Hold Time after I/OSCLK Rising Edge	t <sub>dh</sub>	5.5			ns
TDM Mode OLRCK High-level Time <sup>10</sup>	t <sub>lrckh</sub>	20			ns
TDM Mode OLRCK Rising Edge to OSCLK Rising Edge	t <sub>fss</sub>	5.3			ns
TDM Mode OSCLK Rising Edge to OLRCK Falling Edge	t <sub>fsh</sub>	4.2			ns
Master Mode <sup>11</sup>					
I/OSCLK Frequency (non-TDM Mode)		48Fsi/o		128Fsi/o	MHz
I/OLRCK Duty Cycle		49.5		50.5	%
I/OSCLK Duty Cycle		45		55	%
I/OSCLK Falling Edge to I/OLRCK Edge	t <sub>icks</sub>			4.2	ns
OSCLK Falling Edge to SDOUT Output Valid	t <sub>dpd</sub>			4.6	ns
SDIN Setup Time before I/OSCLK Rising Edge	t <sub>ds</sub>	2.7			ns
SDIN Hold Time after I/OSCLK Rising Edge	t <sub>dh</sub>	5.5			ns
TDM Mode OSCLK Frequency <sup>12</sup>				49.152	MHz
TDM Mode OSCLK Falling Edge to OLRCK Edge	t <sub>fsm</sub>			4.2	ns
VL = 1.8V, 2.5V					
RMCK/MCLK_OUT Output Frequency (VL=1.8V)				13.5	MHz
RMCK/MCLK_OUT Output Frequency (VL=2.5V)				31	MHz
RMCK/MCLK_OUT Output Duty Cycle (VL=1.8V)		37	50	63	%
RMCK/MCLK_OUT Output Duty Cycle (VL=2.5V)		45	50	55	%

Parameter	Symbol	Min	Typ	Max	Unit
Slave Mode					
ISCLK Frequency				49.152	MHz
ISCLK High-level Time	$t_{sckh}$	9.2			ns
ISCLK Low-level Time	$t_{sckl}$	9.2			ns
OSCLK Frequency				15.7	MHz
OSCLK High-level Time	$t_{sckh}$	28.7			ns
OSCLK Low-level Time	$t_{sckl}$	28.7			ns
I/OLRCK Edge to I/OSCLK Rising Edge	$t_{icks}$	7.4			ns
I/OSCLK Rising Edge to I/OLRCK Edge	$t_{ickd}$	6.2			ns
OSCLK Falling Edge/OLRCK to SDOUT Output Valid	$t_{dpd}$			29.5	ns
SDIN/TDM_IN Setup Time before I/OSCLK Rising Edge	$t_{ds}$	4.7			ns
SDIN/TDM_IN Hold Time after I/OSCLK Rising Edge	$t_{dh}$	7.3			ns
TDM Mode OLRCK High-level Time <sup>10</sup>	$t_{lrckh}$	20			ns
TDM Mode OLRCK Rising Edge to OSCLK Rising Edge	$t_{fss}$	7.0			ns
TDM Mode OSCLK Rising Edge to OLRCK Falling Edge	$t_{fsh}$	6.2			ns
Master Mode <sup>11</sup>					
I/OSCLK Frequency (non-TDM Mode)		48Fsi/o		128Fsi/o	MHz
I/OLRCK Duty Cycle		45		55	%
I/OSCLK Duty Cycle		45		55	%
I/OSCLK Falling Edge to I/OLRCK Edge	$t_{icks}$			5.7	ns
OSCLK Falling Edge to SDOUT Output Valid (VL=1.8V)	$t_{dpd}$			11.2	ns
OSCLK Falling Edge to SDOUT Output Valid (VL=2.5V)	$t_{dpd}$			6.4	ns
SDIN Setup Time before I/OSCLK Rising Edge	$t_{ds}$	4.7			ns
SDIN Hold Time after I/OSCLK Rising Edge	$t_{dh}$	7.3			ns
TDM Mode OSCLK Frequency <sup>12</sup>				31I	MHz
TDM Mode OSCLK Falling Edge to OLRCK Edge (VL=1.8V)	$t_{fsm}$			9.6	ns
TDM Mode OSCLK Falling Edge to OLRCK Edge (VL=2.5V)	$t_{fsm}$			5.7	ns

Note:

7. After powering up the MS8422N,  $\overline{RST}$  must keep low until the power supplies and clocks are stable.

8. If ISCLK is selected as the clock source for the PLL, then the sampling rate is ISCLK/64。

9. Typical baseband jitter refers to section 3.4.2 of AES-12id-2006. The measured sampling rate is 48kHz.
10. In TDM mode, OLRCK must keep high for at least 1 OSCLK cycle and at most 255 OSCLK cycles.
11. In TDM formatted master mode, the TDM\_IN pin is not supported.
12. In TDM formatted master mode, the OSCLK frequency is fixed at 256×OLRCK.

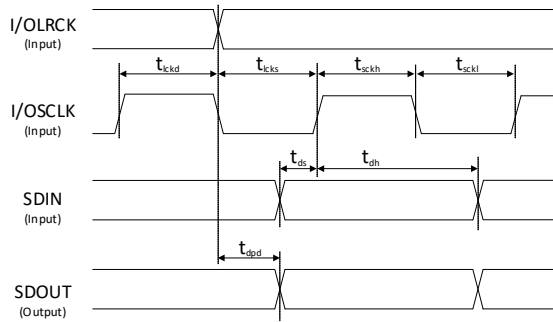


Figure 1. Non-TDM Slave Mode Timing

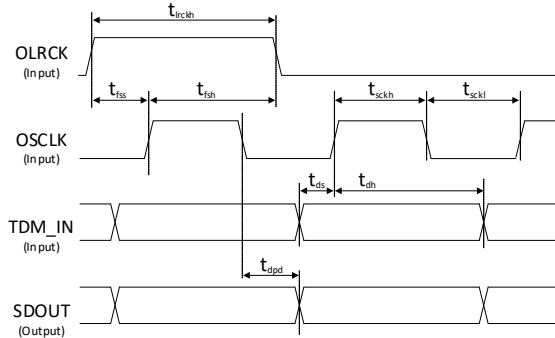


Figure 2. TDM Slave Mode Timing

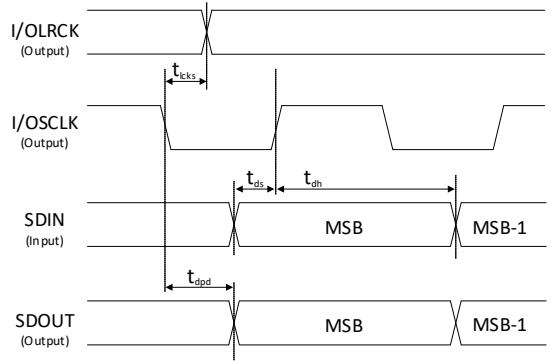


Figure 3. Non-TDM Master Mode Timing

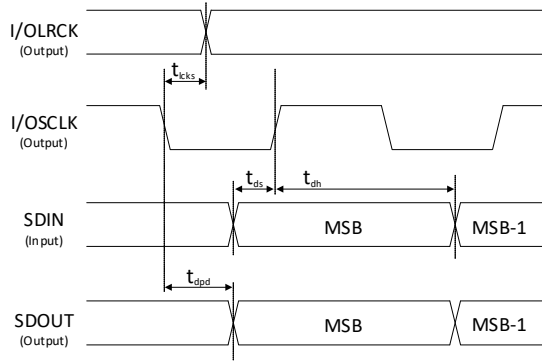


Figure 4. TDM Master Mode Timing

### Switching Characteristics- Control Port -SPI Mode

Input: Logic 0 = 0 V, Logic 1 = VL; C<sub>L</sub> = 20 pF.

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	f <sub>sck</sub>	0	6.0	MHz
RST Rising Edge to CS Falling Edge	t <sub>srs</sub>	500		μs
CCLK Edge to CS Falling Edge <sup>13</sup>	t <sub>spi</sub>	500		ns
CS High-level Time Between Transmissions	t <sub>csh</sub>	1.0		μs
CS Falling Edge to CCLK Edge	t <sub>css</sub>	20		ns
CCLK Low-level Time	t <sub>scl</sub>	66		ns
CCLK High-level Time	t <sub>sch</sub>	66		ns
Setup Time from CDIN to CCLK Rising Edge	t <sub>dsu</sub>	40		ns

Parameter	Symbol	Min	Max	Unit
Hold Time from CCLK Rising Edge to DATA <sup>14</sup>	$t_{dh}$	15		ns
CCLK Falling Edge to CDOOUT Valid <sup>15</sup>	$t_{scdov}$		100	ns
Time from $\overline{CS}$ Falling Edge to CDOOUT High-Z	$t_{cscdo}$		100	ns
CDOOUT Rising Edge Time	$t_{r1}$		25	ns
CDOOUT Falling Edge Time	$t_{f1}$		25	ns
CCLK and CDIN Rising Edge Time <sup>16</sup>	$t_{r2}$		100	ns
CCLK and CDIN Falling Edge Time <sup>16</sup>	$t_{f2}$		100	ns

Note:

13.  $t_{spi}$  is only needed on the first falling edge of  $\overline{CS}$  after the  $\overline{RST}$  rising edge,  $t_{spi} = 0$  at all other times.

14. Data must be held for sufficient time to bridge the transition time of CCLK.

15. CDOOUT should not be sampled during this time.

16.  $f_{sck} < 1\text{MHz}$ .

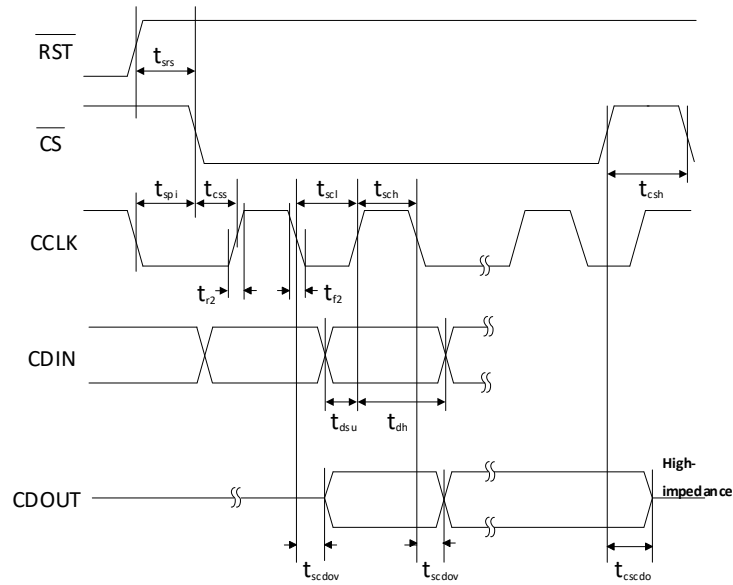


Figure 5. SPI Mode Timing



### Switching Characteristics - Control Port - I<sup>2</sup>C Mode

Input: logic 0 = 0 V, logic 1 = VL; C<sub>L</sub> = 20 pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	$f_{scl}$		100	kHz
$\overline{\text{RST}}$ Rising Edge to I <sup>2</sup> C Start	$t_{irs}$	500		$\mu\text{s}$
Bus Free Time between Transmissions	$t_{buf}$	4.7		$\mu\text{s}$
Start Condition Hold Time (prior to First Clock Pulse)	$t_{hdst}$	4.0		$\mu\text{s}$
Clock Low-level Time	$t_{low}$	4.7		$\mu\text{s}$
Clock High-level Time	$t_{high}$	4.0		$\mu\text{s}$
Setup Time for Repeated Start Condition	$t_{sust}$	4.7		$\mu\text{s}$
Hold Time from SCL Falling Edge to SDA <sup>17</sup>	$t_{hdd}$	10		ns
Setup Time from SDA to SCL Rising Edge	$t_{sud}$	250		ns
SCL and SDA Rising Time	$t_{rc}, t_{rd}$		1000	ns
SCL and SDA Falling Time	$t_{fc}, t_{fd}$		300	ns
Setup Time for Stop Condition	$t_{susp}$	4.7		$\mu\text{s}$
Delay from SCL Falling Edge to Response	$t_{ack}$	300	1000	ns

Note:

17. Data must be held for sufficient time to bridge the transition time of SCL  $t_{fc}$ .

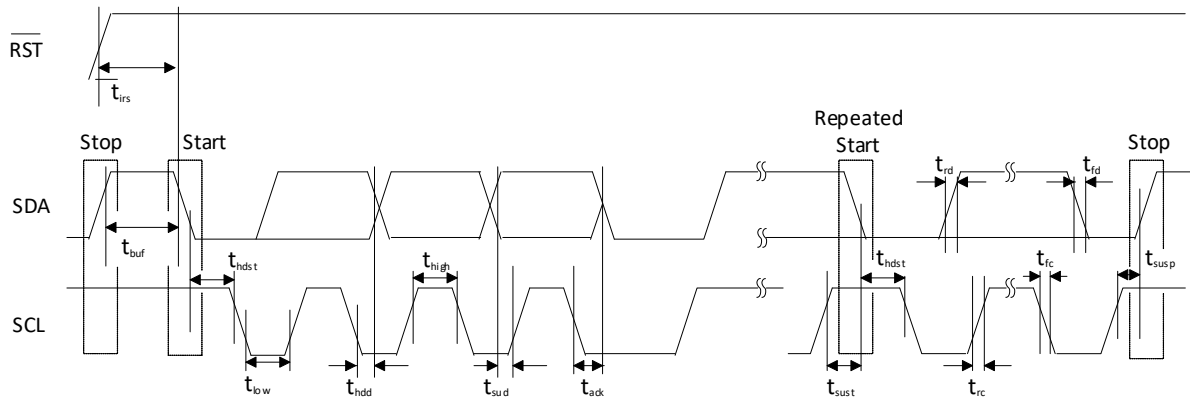


Figure 6. I<sup>2</sup>C Mode Timing

## TYPICAL APPLICATION

### 1. Software Mode

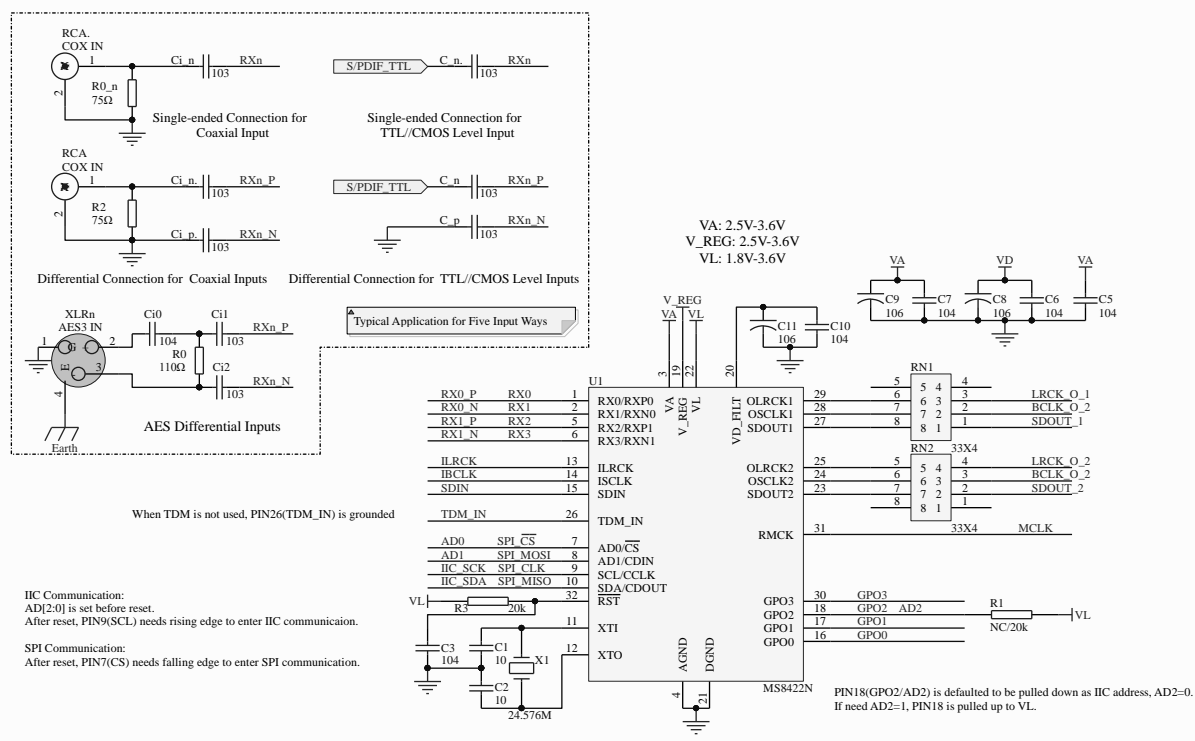


Figure 7. Typical Connection Diagram in Software Mode

## 2. Hardware Mode

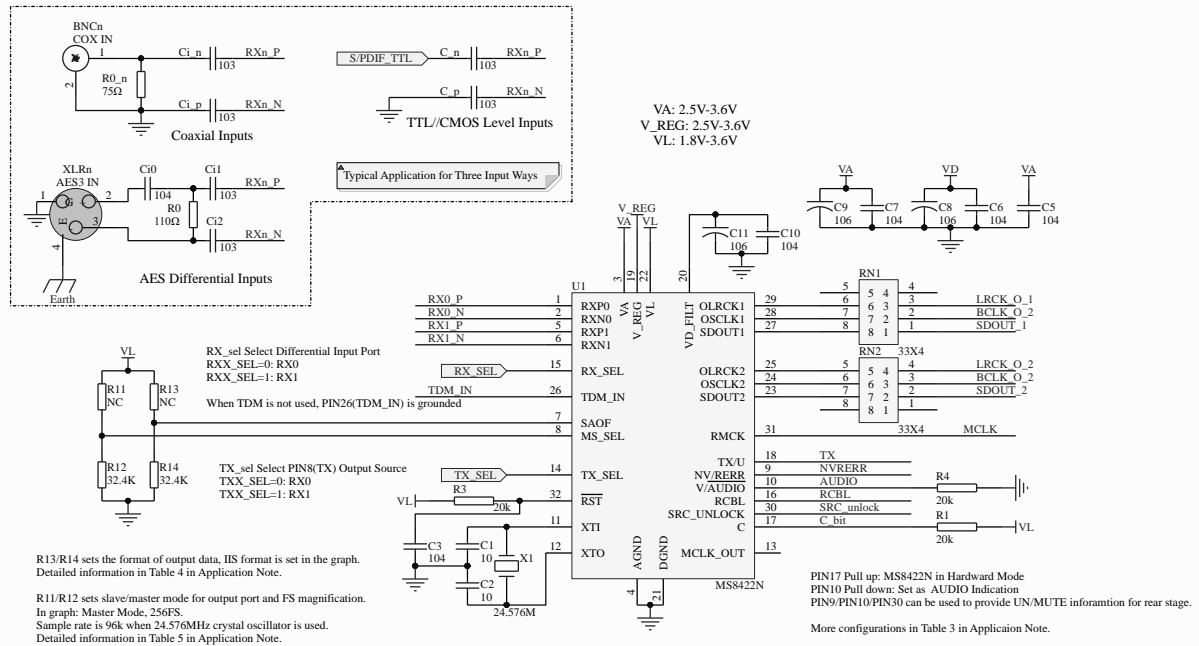
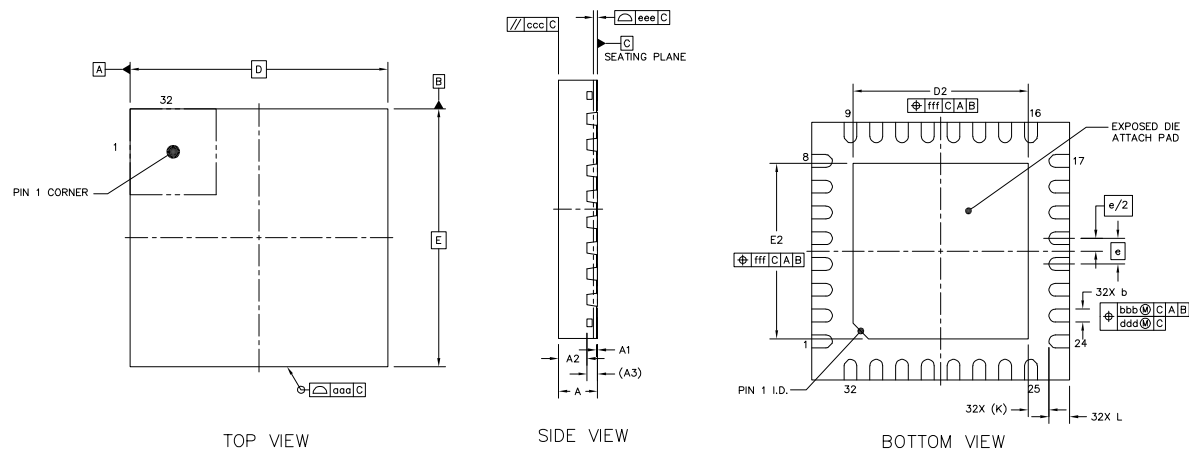


Figure 8. Typical Connection Diagram in Hardware Mode

# PACKAGE OUTLINE DIMENSIONS

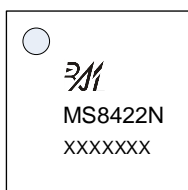
## QFN32



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.2	0.25	0.3
D	5 BSC		
E	5 BSC		
e	0.5 BSC		
D2	3.3	3.4	3.5
E2	3.3	3.4	3.5
L	0.3	0.4	0.5
K	0.4 REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
ddd	0.05		
fff	0.1		

## MARKING and PACKAGING SPECIFICATION

### 1. Marking Drawing Description



Product Name: MS8422N

Product Code: XXXXXXX

### 2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

### 3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS8422N	QFN32	1000	8	8000	4	32000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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