Function and Feature

The MS3989/MS3989N is a quad DMOS full-bridge driver capable of driving up to two stepper motors or four dc motors. Eachfull-bridge output is rated up to 1.2 A and 36 V. The MS3989/MS3989N includes fixed off-time pulse width modulation (PWM) current regulators, along with 2- bit nonlinear DACs (digital-to-analog converters) that allow stepper motors to be controlled in full,half, and quarter steps, and dc motors in forward, reverse, and coast modes. The PWM current regulator uses mixed decay mode for reduced audible motor noise, increased step accuracy, and reduced power dissipation.

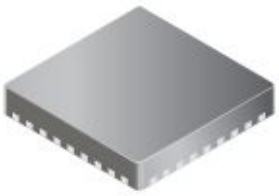
Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation. Protection features include thermal shutdown with hysteresis, undervoltage lockout (UVLO) and crossover current protection.Special power up sequencing is not required.

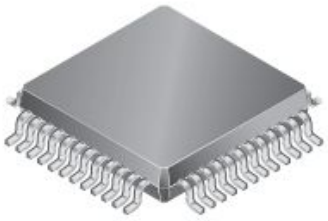
The MS3989/MS3989N is supplied in two packages QFN36，QFP48,with exposed power tabs for enhanced thermal performance.

Featues and benifits：

- ■36 V output rating
- ■4 full bridges
- ■High current outputs
- ■3.3 and 5 V compatible logic supply
- ■Synchronous rectification
- ■UVLO protection
- ■Thermal shutdown circuitry
- ■Crossover-current protection

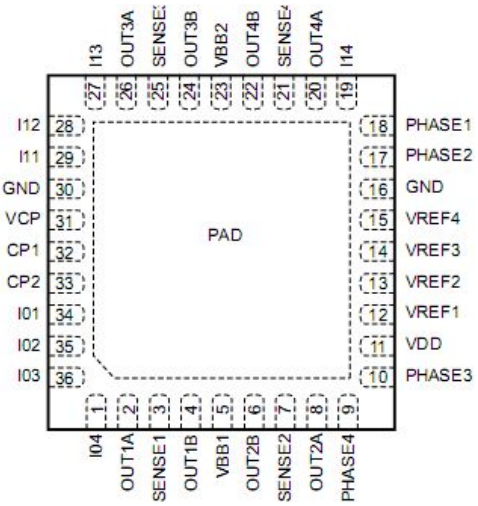
QFN36 LQFP48

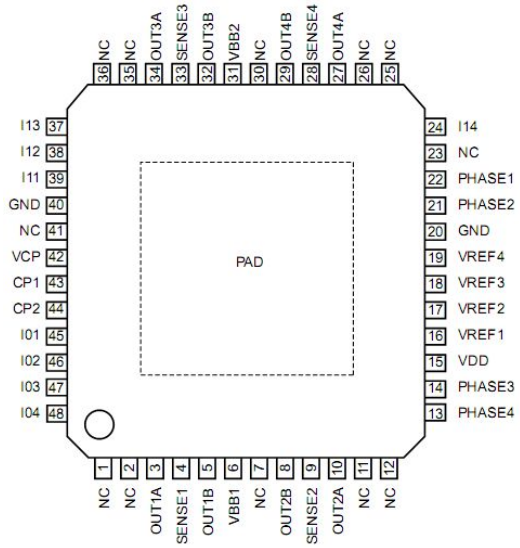




MS3989N MS3989

PIN Function description：

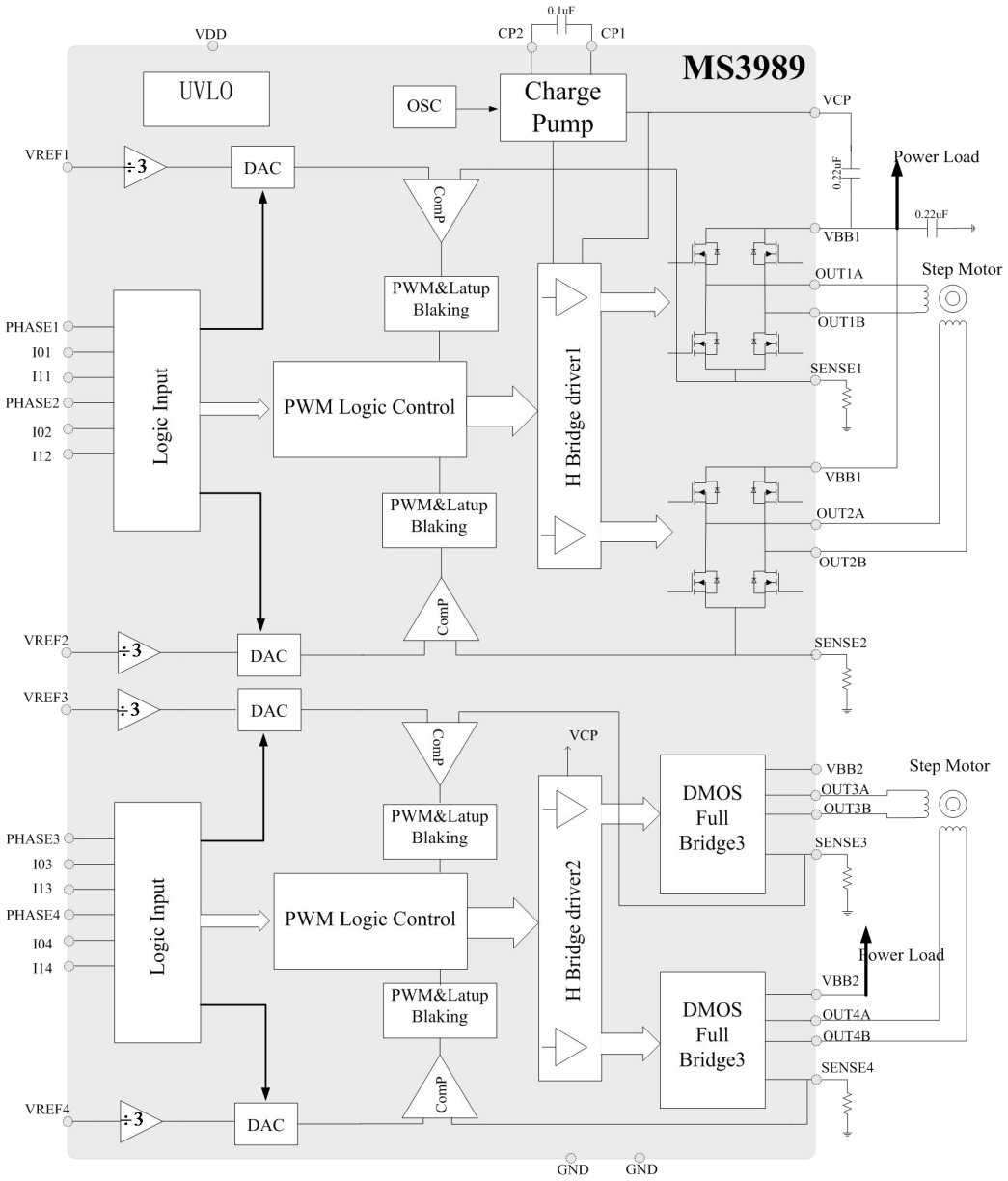




Pin No.		Name	Description
MS3989/MS3989NN	MS3989/MS3989N		
2	3	OUT1A	DMOS H Bridge1 outputA
3	4	SENSE1	H bridge 1 Sense resistor
4	5	OUT1B	DMOS H Bridge1 outputB
5	6	VBB1	Power Load
6	8	OUT2B	DMOS H Bridge2 outputB
7	9	SENSE2	H bridge 2 Sense resistor
8	10	OUT2A	DMOS H Bridge2 outputA
9	13	PHASE4	logic control
10	14	PHASE3	logic control
11	15	VDD	Logic Power
12	16	VREF1	Reference Voltage In
13	17	VREF2	Reference Voltage In
14	18	VREF3	Reference Voltage In
15	19	VREF4	Reference Voltage In
16	20	GND	gnd
17	21	PHASE2	logic control
18	22	PHASE1	logic control
19	24	I14	logic control
20	27	OUT4A	DMOS H Bridge4 outputA
21	28	SENSE4	H bridge 4 Sense resistor
22	29	OUT4B	DMOS H Bridge4 outputB
23	21	VBB2	Power Load
24	32	OUT3B	DMOS H Bridge3 outputB
25	33	SENSE3	H bridge 3 Sense resistor
26	34	OUT3A	DMOS H Bridge3 outputA
27	37	I13	logic control
28	38	I12	logic control
29	39	I11	logic control
30	40	GND	gnd
31	42	VCP	Charge Pump output
32	43	CP1	Pump capacitor1
33	44	CP2	Pump capacitor2
34	45	I01	logic control
35	46	I02	logic control
36	47	I03	logic control

1	48	I04	logic control
-	1,2,7,11,12,23, 25,26,30,35, 36,41	NC	No connect
-	-	PAD	Exposed pad for enhanced thermal performance.Should be soldered to the PCB.

Function Block diagram



（MS3989N same with MS3989）

Chip Characistics

Absolute rating：

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		-0.5~36	V
		Pulsed tw < 1 μs	38	V
Load Supply Voltage	V_{DD}		-0.4~7	V
Output Current	I_{OUT}	May be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a Junction Temperature of 150°C.	1.2	A
		Pulsed tw < 1 μs	2.8	A
Logic Input Voltage Range	Vin		-0.3~7	V
SENSEx Pin Voltage	Vsensex		0.5	V
		Pulsed tw < 1 μs	2.5	V
VREFx Pin Voltage	V_{REFX}		2.5	V
Operating Temperature Range	T_A		-40~85	℃
Junction Temperature	T_{Jmax}		150	℃
Storage Temperature Range	T_{stg}		-40~125	℃

Electrical Characteristics：

（Ta=25℃，V_{BB}=36V，unless otherwise noted）

Characteristics	Symbol	Test Conditions	Min	TYP	Max	Unit
Load Supply Voltage Range	VBB		8.0	-	36	V
Logic Supply Voltage Range	VDD		3.0	-	5.5	V
VDD Supply Current	IDD		-	7	10	mA
Output On Resistance	RDS（on）	Source driver，Iout=1.2A，Tj=25℃	-	700	800	mΩ
		Sink driver, ，	-	700	800	mΩ

		Iout=1.2A，Tj=25℃				
Vf , Outputs		Iout=1.2A	-	-	1.2	V
Output Leakage	IDSS	outputs， Vout=0 to VBB	-20	-	20	uA
VBB Supply Current	IBB	Iout=0mA， outputs on，PWM=50kHz，DC=50%	-	-	8	mA
Logic Input Voltage	Vin（1）		0.7VDD	-	-	V
	Vin（2）		-	-	0.3VDD	V
Logic Input Current	Iin		-20	<1.0	20	uA
Input Hysteresis	Vhys		150	300	500	mV
Propagation Delay Times	Tpd	PWM change to source on	350	550	1000	ns
		PWM change to source off	35	-	300	ns
		PWM change to sink on	350	550	1000	ns
		PWM change to sink off	35	-	250	ns
Crossover Delay	Tcod		300	425	1000	ns
Blank Time	Tblank		0.7	1	1.3	us
VREFx Pin Input Voltage Range	Vrefx	Operating	0	-	1.5	V
VREFx Pin Reference Input Current	Iref	Vref=1.5	-	-	±1	uA
Current Trip-Level Error	Verr	Vref=1.5 ， phase current 100%	-5	-	5	%
		Vref=1.5 ， phase current 67%	-5	-	5	%
		Vref=1.5 ， phase current 33%	-15	-	15	%
VBB UVLO Threshold	VUV（VBB）	VBB rising	7.3	7.6	7.9	V
VBB Hysteresis	VUV（VBB）hys		400	500	600	mV
VDD UVLO Threshold	VUV（VDD）	VDD rising	2.65	2.8	2.95	V
VDD Hysteresis	VUV（VDD）hys		75	105	125	mV
Thermal Shutdown	Tjtsd		155	165	175	℃

Temperature						
Thermal Shutdown Hysteresis	Tjtsd-hys		-	15	-	℃

note1：Current Trip-Level Error Verr =（Vref/3 - Vsense）/（Vref/3）

Function Description

Device Operation

The MS3989/MS3989N is designed to operate two stepper motors, four dc motors, or one stepper and two dc motors. The currents in each of the output full-bridges, all N-channel DMOS, are regulated with fixed off-time pulse width modulated (PWM) control circuitry. Each full-bridge peak current is set by the value of an external current sense resistor, RSx , and a reference voltage, VREFx . If the logic inputs are pulled up to VDD, it is good practice to use a high value pull-up resistor in order to limit current to the logic inputs, should an overvoltage event occur. Logic inputs include: PHASEx, I0x, and I1x.

Internal PWM Current Control

Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value, ITRIP . Initially, a diagonal pair of source and sink DMOS outputs are enabled and current flows through the motor winding and RSx. When the voltage across the current sense resistor equals the voltage on the VREFx pin, the current sense comparator resets the PWM latch, which turns off the source driver. The maximum value of current limiting is set by the selection of RS and the voltage at the VREF input with a transconductance function approximated by:

ITripMax = VREF / (3×RS)

Each current step is a percentage of the maximum current, ITripMax. The actual current at each step ITrip is approximated by:

ITrip = (% ITripMax / 100) ITripMax

where % ITripMax is given in the Step Sequencing table.

Note: It is critical to ensure that the maximum rating of ±500 mV on each SENSEx pin is not exceeded.

Fixed Off-Time

The internal PWM current control circuitry uses a one shot circuit to control the time the drivers remain off. The one shot off-time, toff , is internally set to 9μs.

Blanking

This function blanks the output of the current sense comparator when the outputs are switched by the internal current control circuitry. The comparator output is blanked to prevent false detections of overcurrent conditions, due to reverse recovery currents of the clamp diodes, or to switching transients related to the capacitance of the load. The stepper blank time, tBLANK , is approximately 1 μs.

Control Logic

Communication is implemented via the industry standard I1, I0, and PHASE interface. This communication logic allows for full, half, and quarter step modes. Each bridge also has an independent VREF input so higher resolution step modes can be programmed by dynamically changing the voltage on the VREFx pins.

Charge Pump (CP1 and CP2)

The charge pump is used to generate a gate supply greater than the VBB in order to drive the source-side DMOS gates. A 0.1 μF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1 μF ceramic capacitor is required between VCP and VBBx to act as a reservoir to operate the high-side DMOS devices.

Shutdown

In the event of a fault (excessive junction temperature, or low voltage on VCP), the outputs of the device are disabled until the fault condition is removed. At power-up, the undervoltage lockout (UVLO) circuit disables the drivers.

Synchronous Rectification

When a PWM-off cycle is triggered by an internal fixed off-time cycle, load current will recirculate. The MS3989/MS3989N synchronous rectification feature will turn on the appropriate MOSFETs during the current decay, and effectively short out the body diodes with the low RDS(on) driver. This significantly lowers power dissipation. When a zero current level is detected, synchronous rectification is turned off to prevent reversal of the load current.

Mixed Decay Operation

The bridges operate in mixed decay mode. Referring to figure 2, as the trip point is reached, the device goes into fast decay mode for 30.1% of the fixed off-time period. After this fast decay portion, tFD , the device switches to slow decay mode for the remainder of the off-time. During transitions from fast decay to slow decay, the drivers are forced off for approximately 600 ns. This feature is added to prevent shoot-through in the bridge. As shown in figure 2, during this “dead time” portion, synchronous rectification is not active, and the device operates in fast decay and slow decay only.

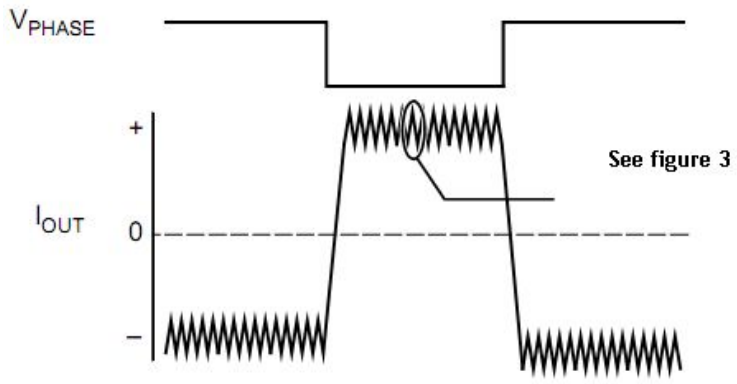


Figure 2： mixed decay mode

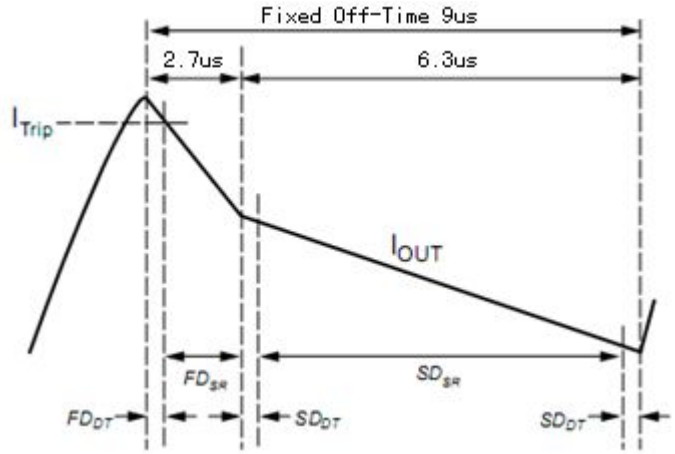


Figure 3： mixed decay mode operation

Step Sequencing Diagrams:

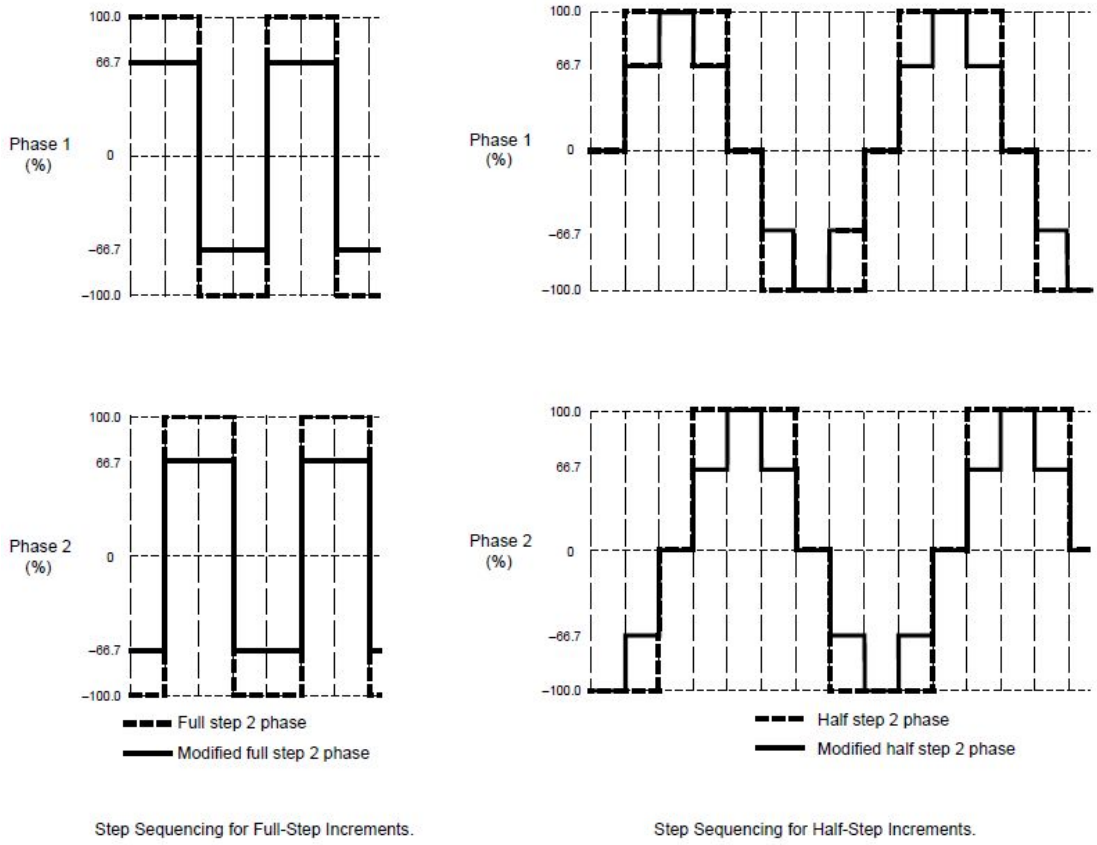


Figure4

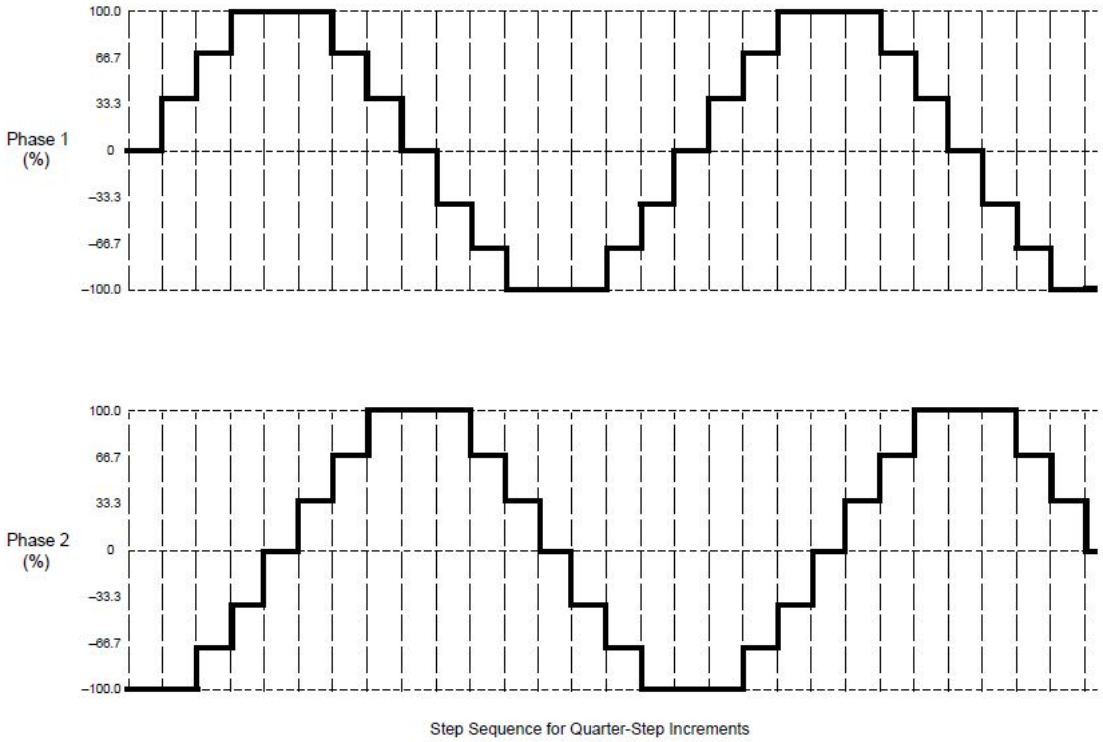


Figure5

Step Sequencing Settings

Full	1/2	1/4	Phase 1 ($\%I_{TripMax}$)	I0x	I1x	PHASE	Phase 2 ($\%I_{TripMax}$)	I0x	I1x	PHASE
	1	1	0	H	H	x	100	L	L	1
		2	33	L	H	1	100	L	L	1
1	2	3	100/66*	L/H*	L	1	100/66*	L/H*	L	1
		4	100	L	L	1	33	L	H	1
	3	5	100	L	L	1	0	H	H	X
		6	100	L	L	1	33	L	H	0
2	4	7	100/66*	L/H*	L	1	100/66*	L/H*	L	0
		8	33	L	H	1	100	L	L	0
	5	9	0	H	H	x	100	L	L	0
		10	33	L	H	0	100	L	L	0
3	6	11	100/66*	L/H*	L	0	100/66*	L/H*	L	0
		12	100	L	L	0	33	L	H	0
	7	13	100	L	L	0	0	H	H	X
		14	100	L	L	0	33	L	H	1
4	8	15	100/66*	L/H*	L	0	100/66*	L/H*	L	1
		16	33	L	H	0	100	L	L	1

Figure6

Application Information

DC Motor Control

Each of the 4 full bridges has independent PWM current control circuitry that makes the MS3989/MS3989N capable of driving up to four dc motors at currents up to 1.2 A. Control of the dc motors is accomplished by tying the I0, I1 pins together creating an equivalent ENABLE function with maximum current defined by the voltage on the corresponding VREF pin. The dc motors can be driven via a PWM signal on this enable signal, or on the corresponding PHASE pin. Motor control includes forward, reverse, and coast.

Layout

The printed circuit board should use a heavy groundplane. For optimum electrical and thermal performance, the MS3989/MS3989N must be soldered directly onto the board. On the underside of the MS3989/MS3989N package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

Grounding

In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance singlepoint ground, known as a star ground, located very close to the device. By making vthe connection between the exposed thermal pad and the groundplane directly under the MS3989/MS3989N, that area becomes an ideal location for a star ground point. A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal. The recommended PCB layout shown in the diagram below, illustrates how to create a star groundunder the device, to serve both as low impedance ground point and thermal path.

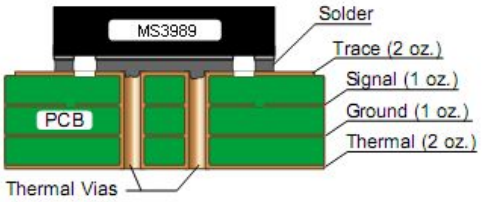


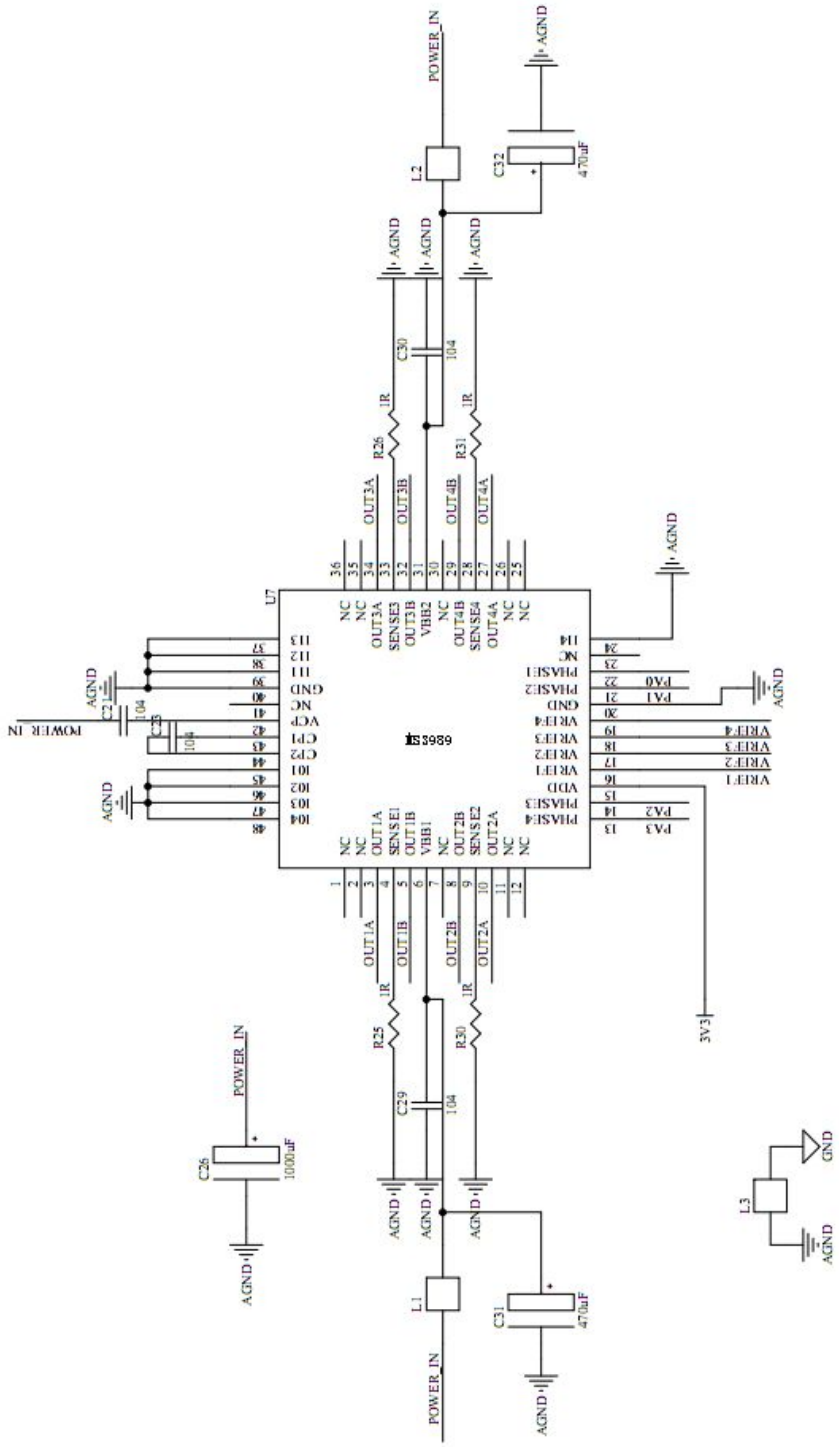
Figure7 PCB show

Sense Pins

The sense resistors, RSx, should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. As shown in the layout below, the SENSEx pins have very short traces to the RSx resistors and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.

Note: When selecting a value for the sense resistors, be sure not to exceed the maximum voltage on the SENSEx pins of ±500 mV.

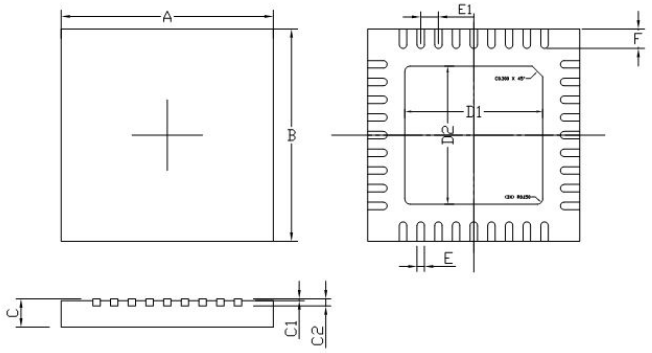
Typical applition diagram



Package show

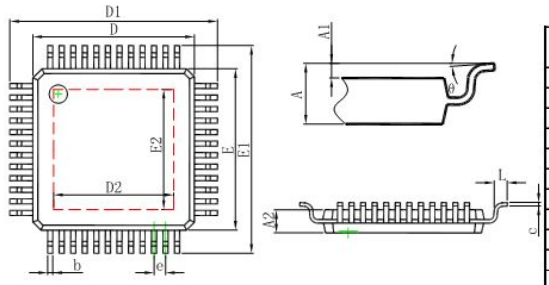
QFN36 UNIT: mm

尺寸 / 标注	最小（mm）	最大（mm）	尺寸 / 标注	最小（mm）	最大（mm）
A	6.0±0.1		D1	3.90TYP	
B	6.0±0.1		D2	3.90TYP	
C	0.70	0.80	E	0.210±0.025	
C1	0~0.050		E1	0.500TYP	
C2	0.203TYP		F	0.550TYP	



QFP48 UNIT: mm

TQFP48/PP（7×7） PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.950	1.050	0.037	0.041
b	0.190	0.260	0.007	0.010
c	0.090	0.200	0.004	0.008
D	6.900	7.100	0.272	0.280
D1	8.850	9.150	0.348	0.360
D2	5.100	5.300	0.201	0.209
E	6.900	7.100	0.272	0.280
E1	8.850	9.150	0.348	0.360
E2	5.100	5.300	0.201	0.209
e	0.500(BSC)		0.020(BSC)	
L	0.450	0.750	0.018	0.030
θ	1°	7°	1°	7°