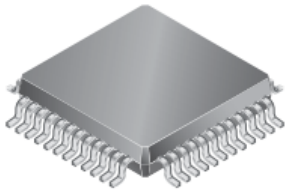
Four-channel DMOS Full-bridge Driver

PRODUCT DESCRIPTION

The MS3999 is a DMOS full-bridge driver with four channels and programmable current, which can drive two stepper motors or four DC motors. The driving current of each full-bridge can be up to 1.2A at 36V. The MS3999 integrates the PWM current regulator with fixed off-time. In addition, the chip also integrates an 8-bit DAC with four channels to realize digital control for driver channel current. Through digital I^2C interface, programming the DAC input can realize 256 microsteps motor drive. PWM current regulator uses mixed decay mode, which can reduce audio motor noise and power dissipation and improve step accuracy. The chip integrates internal synchronous rectification control circuit to reduce PWM operating power dissipation.

The chip integrates protection circuits, such as thermal shutdown hysteresis, undervoltage protection (UVLO), overturn protection, the specific power-on sequence is not required.

The MS3999 adopts TQFP48 package.



TQFP48

FEATURES

- 36V Output
- Four-channel Full-bridge
- Four-channel 8-bit DAC
- 1x or 2x Output by DAC Programming
- Dual Stepper Motor Driving
- High-current Output
- 3.3V and 5V Logic
- Synchronous Rectification
- UVLO
- Thermal Shutdown
- Overturn Protection

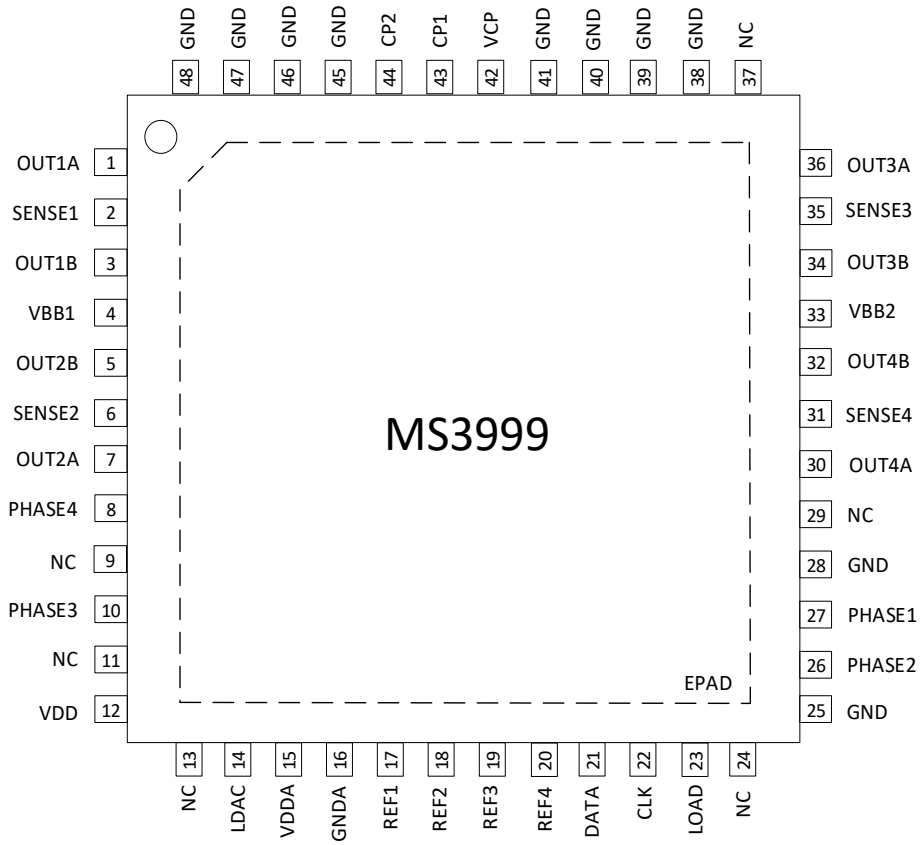
APPLICATIONS

- Security Monitoring
- Stage Light
- Toy
- Robot
- Medical Device

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS3999	TQFP48	MS3999

PIN CONFIGURATION

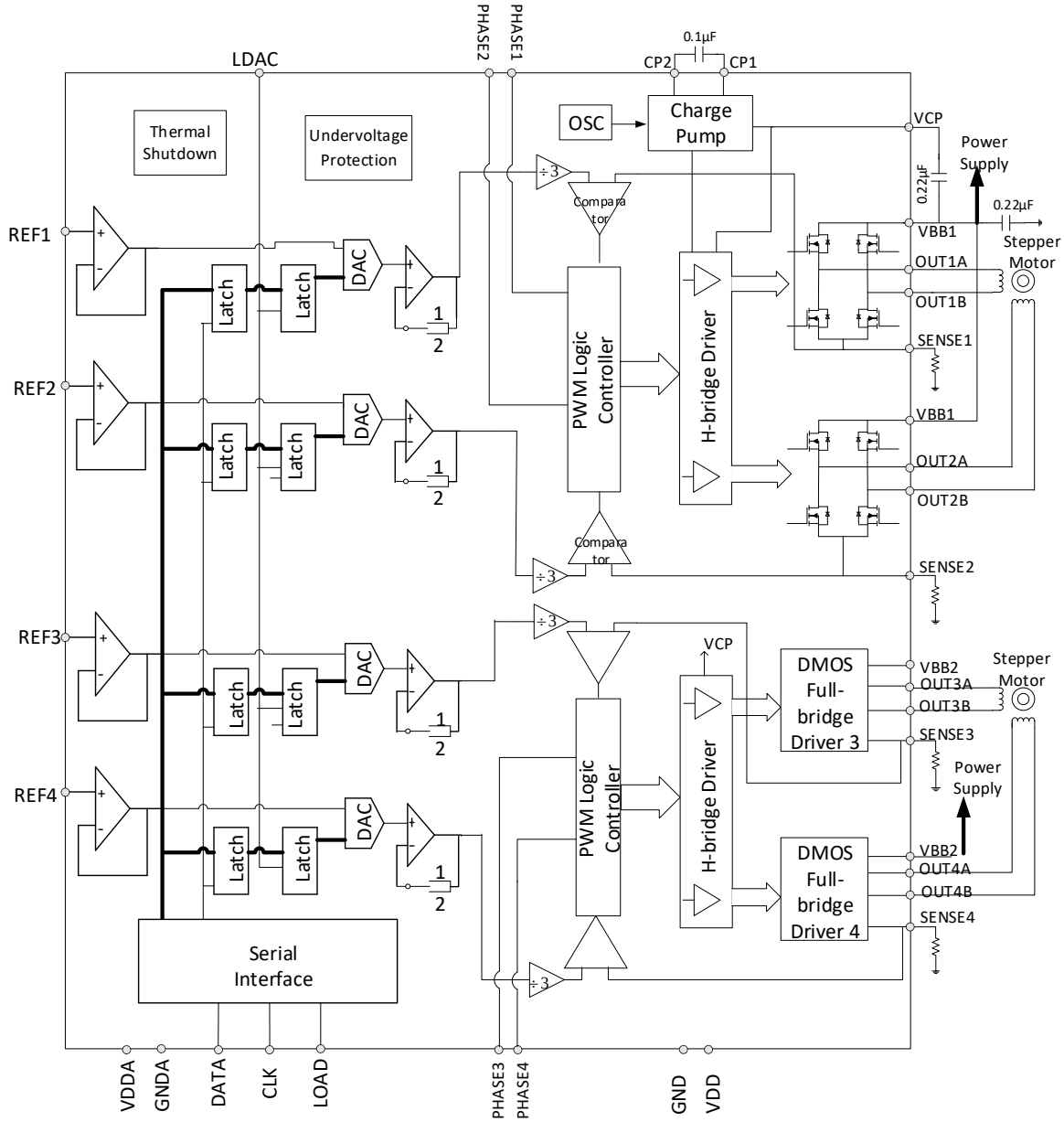


PIN DESCRIPTION

Pin	Name	Type	Description
1	OUT1A	O	DMOS H-Bridge Channel 1 Output A
2	SENSE1	IO	Channel 1, SENSE Resistor Pin
3	OUT1B	O	DMOS H-Bridge Channel 1 Output B
4	VBB1	-	Load Power Supply 1
5	OUT2B	O	DMOS H-Bridge Channel 2Output B
6	SENSE2	IO	Channel 2, SENSE Resistor Pin
7	OUT2A	O	DMOS H-Bridge Channel 2 Output A
8	PHASE4	I	Channel 4, Direction Control Input Pin
10	PHASE3	I	Channel 3, Direction Control Input Pin
12	VDD	-	Logic Power Supply
14	LDAC	I	DAC Data Loading. When LDAC is high, the input data is read at the serial interface, the DAC output cannot be updated. Only when LDAC is from high to low, the DAC output can be updated.
15	VDDA	-	Analog Power Supply
16	GNDA	-	Analog Ground
17	REF1	I	Reference Voltage of DAC Channel 1
18	REF2	I	Reference Voltage of DAC Channel 2
19	REF3	I	Reference Voltage of DAC Channel 3
20	REF4	I	Reference Voltage of DAC Channel 4
21	DATA	I	Serial Interface Digital Data Input. On the falling edge of clock signal, every data is written to the register of the serial interface.
22	CLK	I	Serial Interface Clock. On the falling edge of input clock, the input serial data is written to the register of the serial interface.
23	LOAD	I	Serial Interface Data Load. When LDAC is low, data is locked in the output latches. And analog signal is generated immediately in the channel selected by DAC.
25	GND	-	Ground
26	PHASE2	I	Channel 2, Direction Control Input Pin
27	PHASE1	I	Channel 1, Direction Control Input Pin
28	GND	-	Ground

Pin	Name	Type	Description
30	OUT4A	O	DMOS H-Bridge Channel 4 Output A
31	SENSE4	IO	Channel 4, SENSE Resistor Pin
32	OUT4B	O	DMOS H-Bridge Channel 4 Output B
33	VBB2	-	Load Power Supply 2
34	OUT3B	O	DMOS H-Bridge Channel 3 Output B
35	SENSE3	IO	Channel 3, SENSE Resistor Pin
36	OUT3A	O	DMOS H-Bridge Channel 3 Output A
38	GND	-	Ground
39	GND	-	Ground
40	GND	-	Ground
41	GND	-	Ground
42	VCP	IO	Charge Storage Capacitor Pin
43	CP1	IO	Charge-pump Capacitor Pin
44	CP2	IO	Charge-pump Capacitor Pin
45	GND	-	Ground
46	GND	-	Ground
47	GND	-	Ground
48	GND	-	Ground
9,11,13,24, 29, 37	NC	-	No Connection
-	EPAD	-	Exposed Thermal Pad, Soldered to PCB Directly

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Load Power Supply	V_{BB}	-0.5 ~ 36	V
Logic Power Supply	V_{DD}	-0.4 ~ 7	V
Analog Power Supply	V_{DDA}	-0.4 ~7	V
Output Current	I_{OUT}	1.2	A
Logic Input Voltage Range	V_{IN}	-0.3 ~ 7	V
Voltage on the Sensex Pin	V_{SENSEX}	0.5	V
Operating Temperature	T_A	-40 ~ 105	°C
Junction Temperature	T_{JMAX}	150	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A=25°C, V_{BB}=24V, V_{DD}=3.3V.

Driving Part

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Driving Power Supply	V_{BB}		8.0		36	V
Logic Power Supply	V_{DD}		3.0		5.5	V
Analog Power Supply	V_{DDA}		2.7		5.25	V
Reference Input	$V_{REF1234}$	REF1234 Pin Input	0		V_{DDA}-1.5	V
VDD Current	I_{DD}			4	10	mA
Output Resistance	$R_{DS(on)}$	Source Drive, I_{OUT}=500mA,T_J=25°C		700		mΩ
		Drain Drive, I_{OUT}=500mA,T_J=25°C		700		mΩ
Forward Voltage Drop	V_F	I_{OUT}=1.2A		1.2		V
Output Leakage Current	I_{DSS}		-20		20	μA
VBB Current	I_{BB}	I_{OUT}=0mA, Output Enable, PWM=50kHz, DC=50%		5	10	mA
High-level Logic Input	V_{IN1}		0.7×V_{DD}			V
Low-level Logic Input	V_{IN2}				0.3×V_{DD}	
Logic Input Current	I_{IN}		-20	<1.0	20	μA
Hysteresis	V_{HYS}			300		mV
Propagation Delay	t_{PD}	PWM Conversion, Source Drive Enable		730		ns
		PWM Conversion, Source Drive Disable		250		ns
		PWM Conversion, Drain Drive Enable		730		ns
		PWM Conversion, Drain Drive Disable		180		ns

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Overturn Protection	t_{COD}			600		ns
Blank Time	t_{BLANK}			1		μs
VBB UVLO	$V_{UV(VBB)}$	VBB Rising		7.3		V
VBB Hysteresis	$V_{UV(VBB)HYS}$			500		mV
VDD UVLO	$V_{UV(VDD)}$	VDD Rising		2.8		V
VDD Hysteresis	$V_{UV(VDD)HYS}$			100		mV
Thermal Shutdown	T_{JTSD}			165		°C
Thermal Shutdown Hysteresis	$T_{JTSD-HYS}$			15		°C

DAC Parameters

Unless otherwise noted, V_{DDA}=3.3V±5%, V_{REF}=2V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Current	I_{IH}	$V_I=V_{DD}$			±10	μA
low-level Input Current	I_{IL}	V_I=0			±10	μA
Current-sink Output	$I_{O(SINK)}$	Each DAC Output	20			μA
Current-source Output	$I_{O(SOURCE)}$	Each DAC Output	1			mA
Input Capacitor	C_i			15		pF
Referenced Input Capacitor				15		pF
Power Supply Current	I_{DDA}	V_{DDA}=3.3V			2	mA
Referenced Input Current	I_{REF}	V_{DDA}=3.3V, $V_{REF1234}$=1.5V			±10	μA
Integral Nonlinear Error[1]	E_L	$V_{REF1234}$=1.25V, Gain=2			±1	LSB
Differential Nonlinear Error[2]	E_D	$V_{REF1234}$=1.25V, Gain=2			±0.9	LSB
Zero Error[3]	E_{ZS}	V_{REF}=1.25V, Gain=2	0		30	mV
Zero Error Temperature Coefficient[4]		V_{REF}=1.25V, Gain=2		10		μV/℃
Full-scale Error[5]	E_{FS}	V_{REF}=1.25V, Gain=2			±60	mV
Full-scale Temperature Coefficient[6]		V_{REF}=1.25V, Gain=2		±25		μV/℃
Power Supply Rejection Ratio[7, 8]	PSRR			0.5		mV/V

DAC Parameters (Gain=2)

Unless otherwise noted, V_{DDA}=5V±5%, V_{REF}=2V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Current	I_{IH}	$V_I=V_{DD}$			±10	μA
low-level Input Current	I_{IL}	V_I=0			±10	μA
Current-sink Output	$I_{O(SINK)}$	Each DAC Output	20			μA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Current-source Output	$I_{O(SOURCE)}$	Each DAC Output	2			mA
Input Capacitor	C_i			15		pF
Referenced Input Capacitor				15		pF
Power Supply Current	I_{DD}	V_{DDA}=5V			2	mA
Referenced Input Current	I_{REF}	V_{DDA}=5V, V_{REF}=2V			±10	μA
Integral Nonlinear Error[1]	E_L	V_{REF}=2V, Gain=2			±1	LSB
Differential Nonlinear Error[2]	E_D	V_{REF}=2V, Gain=2			±0.9	LSB
Zero Error[3]	E_{ZS}	V_{REF}=2V, Gain=2	0		30	mV
Zero Error Temperature Coefficient[4]		V_{REF}=2V, Gain=2		10		μV/℃
Full-scale Error[5]	E_{FS}	V_{REF}=2V, Gain=2			±60	mV
Full-scale Temperature Coefficient[6]		V_{REF}=2V, Gain=2		±25		μV/℃
Power Supply Rejection Ratio[7, 8]	PSRR			0.5		mV/V

Note:

1. Integral nonlinear error indicates the actual output deviation from the maximum value of the curve from 0 to full scale (not exclude zero and full-scale errors).

2. Differential nonlinear error refers to the difference between the change in output voltage generated by any two adjacent digital codes and 1 LSB in an 8-digit code. Monotonic indicates that the output voltage direction change is as same as the direction of digital codes.

3. Zero-point error refers to the difference between the output voltage and GND when the input is all zeros.

4. The temperature coefficient of zero error is determined by the following formula:

$$ZSETC=[ZSE(T_{MAX})-ZSE(T_{MIN})]/V_{REF}\times 10^6/(T_{MAX}-T_{MIN})$$

5. Under the condition of load resistance 10kΩ, when the input is all 1, full scale error refers to the difference between actual output voltage and ideal output voltage.

6. The temperature coefficient of full-scale error is determined by the following formula:

$$FSETC=[FSE(T_{MAX})-FSE(T_{MIN})]/V_{REF}\times 10^6/(T_{MAX}-T_{MIN})$$

7. Measurement of zero error rejection ratio: When the 8-bit digital input is all 0, the power supply voltage VDD changes from 4.75V to 5.25V, its influence to the output voltage is measured.

8. Measurement of full-scale error rejection ratio: When the 8-bit digital input is all 1 and the supply voltage VDD changes from 3V to 3.6V, its influence to the output voltage is measured.

FUNCTION DESCRIPTION

Device Characteristics

The MS3999 could drive two stepper motors or four DC motors. A stepper motor and two DC motors can also be driven. The output H full-bridge is consisted of four N-channel DMOS, controlled by PWM. The output peak current of each full bridge is decided by Rsensex (resistor on the Sense) and DACoutx (output voltage of digital to analog conversion).

PHASEx Direction Control Pin

PHASEx	Direction
0	Positive Current A→B
1	Negative Current B→A

Internal PWM Current Control Principle

Each H full-bridge integrates the PWM current control circuit with fixed decay time, making load current not exceed the setting value I_{TRIP}. At the initial stage, one H-bridge diagonal pair of source and drain DMOS are enabled, and current flows through motor and R_{SENSE}. When the voltage on R_{SENSE} is equal to DACout voltage, current detection comparator would reset PWM latches and disable source DMOS.

The maximum current limit is determined by Rsense(Rs) and DACout (DAC output) voltage, the maximum current is calculated:

$$I_{TRIPMax}=V_{DACOUT}/(3\times Rs)$$

The formula of DAC output: $V(DACOUT1|2|3|4)=REF\times\frac{CODE}{256}\times(1+RNG)$

So, the current is decided by REF, digital programming CODE and gain selection RNG.

In addition, please note that the maximum voltage on Rsense doesn't exceed ±500mV.

Fixed Off-time

Internal PWM control circuit integrates one fixed-time pulse to disable drivers, the off-time (t_{OFF}) is set to 9μs.

Blank Time

When internal circuit control makes output change, the output of current detection comparator would be ignored within blank time to avoid output false detection, such as overcurrent, reverse recovery current of clamp diode and reverse transmission caused by output capacitor. The blank time is set to 1μs.

Charge Pump (CP1, CP2)

The charge-pump circuit generates a higher power supply than VBB to drive the source DMOS of H bridge. In applications, due to the need for charge and discharge, a 0.1μF ceramic capacitor is needed to be connected between CP1 and CP2. A 0.1μF ceramic capacitor is also required between VCP and VBBx to store charge.

Shutdown Function

When unexpected conditions such as excessive junction temperature or low VCP occur, output is disabled. At startup, output can be disabled by UVLO when VBB is undervoltage.

Synchronous Rectification

When the internal fixed decay time circuit is triggered and the PWM-off works, the load current will produce a reflux. During current decay, the MS3999 synchronous rectification function will enable the corresponding DMOS and short the parasitic diode with Rdson to reduce power consumption effectively. When detecting zero current, synchronous rectification is disabled to prevent the load current from reversing.

Mixed Decay Mode

H-bridge operates in mixed decay mode as shown in following figures. When current reaches current limit, fast decay mode is performed and the duration time (t_{FD}) occupies 30.1% of total decay period. Then system is in slow decay mode. During the conversion from fast to slow decay, driver would be disabled for 600ns(dead time). The setting could avoid bridge throughout. Just as shown in figure 1 and figure 2, during dead time, synchronous rectification cannot take effect, the chip only operates in fast and slow decay modes.

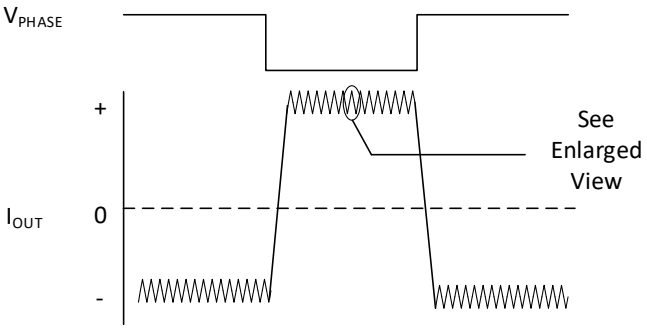


Figure 1. Mixed Decay Mode

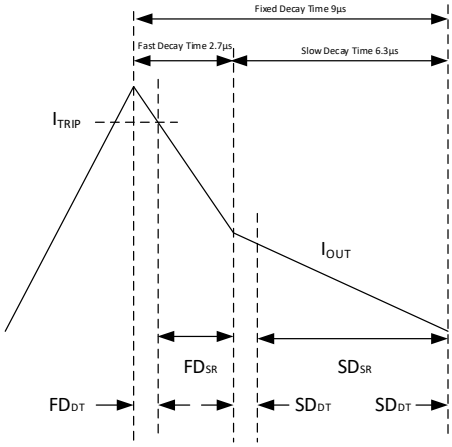


Figure 2. Enlarged View of Mixed Decay Mode

Digital-to-analog Converter DAC

Through I^2C digital interface CLK, DATA inputs 11bit data. Where, 8bit is as the input of DAC. Though DAC and amplifiers, the referenced voltage $V_{DACOUT1234}$ of current comparator can be converted. The different output current of H bridge can be obtained by programming input of different digital sequences. For example: programming makes $V_{DACOUT1}$ of DAC first channel changes with half-wave sinx, and $V_{DACOUT2}$ of second channel changes with half-wave cosx. Two channels combined can control stepper motors rotate steadily.

1. Resistor-string DAC

The MS3999 DAC is consisted of 4 resistor-string DACs, the core of every DAC is a resistor with 256 taps. Table 1 indicates the corresponding relationship between the level at each tap and the corresponding 256 digital codes. In the resistor string, one end of the resistor is connected to GND, and the other end is connected to the output end of the input buffer. The resistor string ensures monotonicity. Linearity is determined by the matching accuracy of the resistor string and the performance of the output buffer. When the reference voltage inputs to the buffer, the DAC can be seen as a load with high impedance to the reference source. The output of each DAC is buffered by a gain-configurable operational amplifier with a choice of 1x or 2x gain outputs. When the circuit is powered on, the digital input of the DAC is set to all zeros. The output voltage of each DAC can be calculated by the following formula:

$$V(DACOUT1\ |2|3|4) = REF \times \frac{CODE}{256} \times (1 + RNG)$$

CODE ranges from 0 to 255. The range control bit RNG is 0 or 1, which is in the serial command word.

Table 1. Ideal Transmission Characteristics

D7	D6	D5	D4	D3	D2	D1	D0	Output Level
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256)×REF(1+RNG)
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	1	(127/256)×REF(1+RNG)
1	0	0	0	0	0	0	0	(128/256)×REF(1+RNG)
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	(255/256)×REF(1+RNG)

2. Operating Timing

The MS3999 has four available control methods, as shown in figure 3- figure 6.

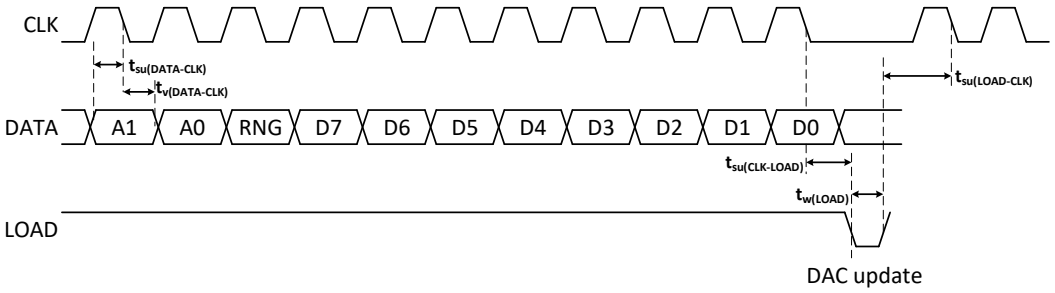


Figure 3. Output Update for LOAD Control (LDAC=Low)

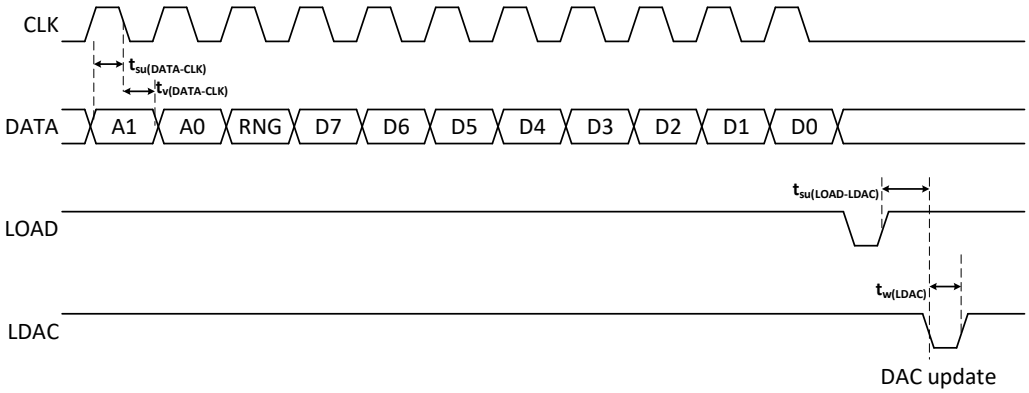


Figure 4. Output Update for LDAC Control

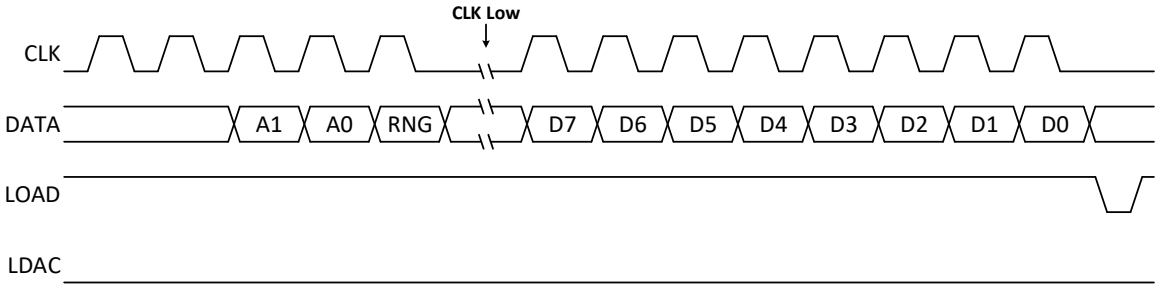


Figure 5. Output Update for LDAC Control, Using 8-bit Serial Command Word (LDAC=Low)

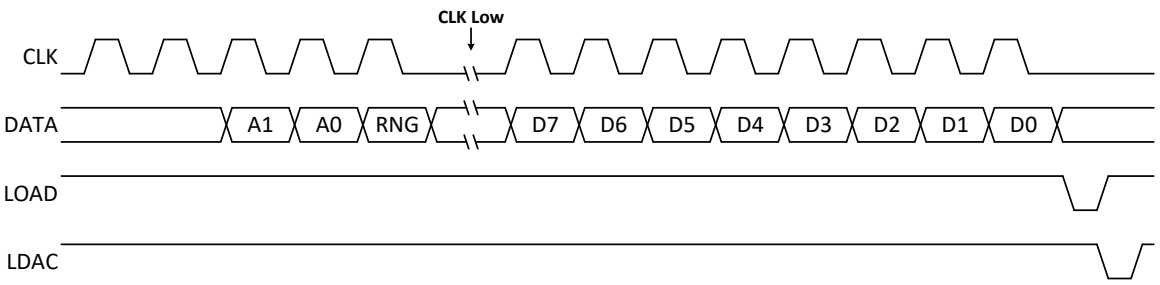


Figure 6. Output Update for LDAC Control, Using 8-bit Serial Command Word

When LOAD is high, on the falling edge of CLK, data on the DATA pin is written to the latches. Once all data is latched, LOAD is pulled low. Data is transferred from the serial input register to the selected DAC for work, as shown in figure 3. When LDAC becomes low, DAC output voltage is immediately updated. During the process of writing serial data, when LDAC is high, new data is latched. Only when waiting for LDAC to be pulled low, the digital-to-analog conversion can be performed, as shown in figure 4. The most significant bit (MSB) is written first, and the data conversion takes 8 clock cycles, as shown in figure 5 and figure 6. table 2 lists the timing relationship.

Table 2. The MS3999 DAC Timing Relationship

Parameter	Min	Typ	Max	Unit
CLK Frequency			10	MHz
Set up Time, Data Input, $t_{su(DATA-CLK)}$ (See Figure 3 and Figure 4)	50			ns
Valid Time, Data Input Valid after CLK↓, $t_{v(CLK\_LOAD)}$(See Figure 3 and Figure 4)	50			ns
Set up Time, CLK Falling Edge to LOAD, $t_{su(CLK-LOAD)}$ (See Figure 3)	50			ns
Set up Time, LOAD↑ to CLK↓, $t_{su(LOAD-CLK)}$ (See Figure 3)	50			ns
Pulse Width, LOAD, $t_{w(LOAD)}$ (See Figure 3)	250			ns
Pulse Width, LDAC, $t_{w(LDAC)}$ (See Figure 4)	250			ns
Set up Time, LOAD↑ to LDAC↓, $t_{su(LOAD-LDAC)}$(See Figure 4)	0			ns

Table 3 lists the selection of DAC path corresponding to A1 and A0. RNG bit controls output voltage range. When RNG = Low, the output voltage range is between reference voltage and GND. When RNG = High, the output voltage range is between 2 times the reference voltage and GND.

Table 3. Serial Input Decoding

A1	A0	Selected DAC channel
0	0	DAC1
0	1	DAC2
1	0	DAC3
1	1	DAC4

Stepper Motor Subdivision Control

Taking the following 1, 2 channels as an example, 3, 4 channels similar.

Using two-channel H-bridge, combined with two-channel DAC, two direction control PHASEx feet, can realize micro-step stepper motor control. The following figure shows control timing. Where, DACout1, 2 are the output of the digitally-controlled DAC, and Ia，Ib are the two-phase current of the stepper motor:

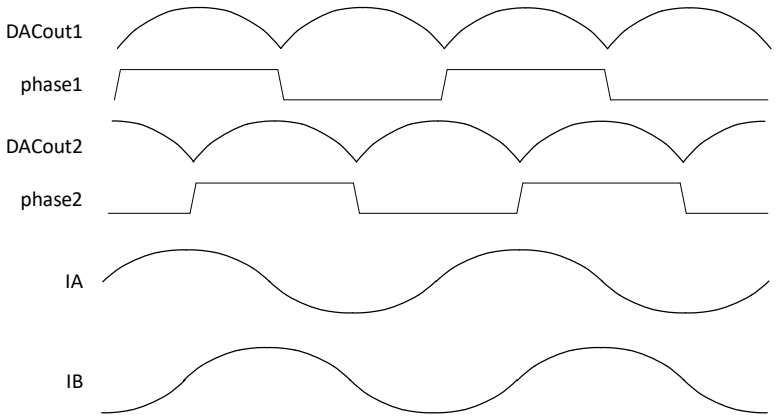
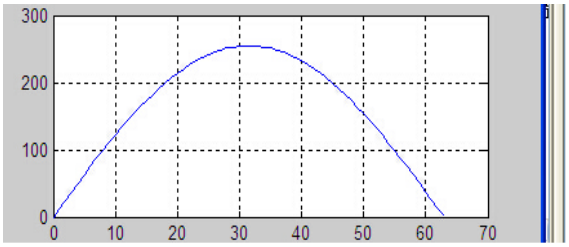


Figure 7. Stepper Motor Subdivision Control Diagram

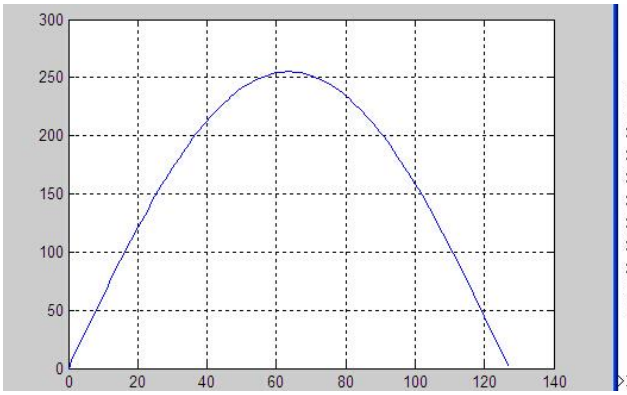
The DACOUT1 and DACOUT2 voltages are achieved through the input of digital programming control DAC; 32, 64, 128, 256 microsteps. Step subdivision of sin half-wave DAC input digital sequence can be referred to the following table (cos half-wave phase shift π/2), when used to convert to 8bit binary system in the DATA pin serial input:

32-Step Subdivision:




```
  0,  13,  25,  38,  51,  63,  75,  87,
 99, 111, 122, 133, 144, 154, 164, 174,
183, 191, 199, 207, 214, 221, 227, 233,
237, 242, 246, 249, 251, 253, 254, 255,
255, 254, 253, 251, 249, 245, 242, 237,
232, 227, 221, 214, 207, 199, 191, 182,
173, 164, 154, 143, 133, 122, 110,  99,
 87,  75,  62,  50,  37,  25,  12,   1,
```

64-Step Subdivision:




```
  0,   6,  13,  19,  25,  31,  38,  44,
 50,  56,  62,  68,  74,  80,  86,  92,
 98, 104, 110, 115, 121, 126, 132, 137,
142, 148, 153, 158, 163, 167, 172, 177,
181, 186, 190, 194, 198, 202, 206, 209,
213, 216, 220, 223, 226, 229, 231, 234,
236, 239, 241, 243, 245, 246, 248, 249,
251, 252, 253, 253, 254, 254, 255, 255,
255, 255, 255, 254, 253, 253, 252, 251,
250, 248, 247, 245, 243, 241, 239, 237,
234, 232, 229, 226, 223, 220, 217, 214,
210, 206, 203, 199, 195, 191, 186, 182,
178, 173, 168, 164, 159, 154, 149, 143,
138, 133, 127, 122, 116, 111, 105,  99,
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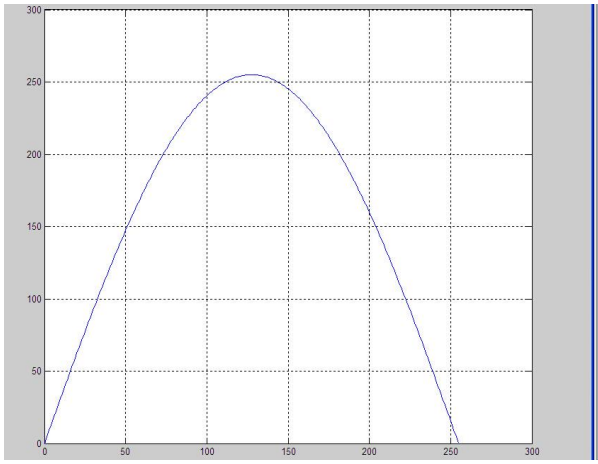
 45,  39,  33,  26,  20,  14,   7,   1,
```

128-step Subdivision:




```
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 25,  28,  31,  34,  38,  41,  44,  47,
 50,  53,  56,  59,  62,  65,  68,  71,
 74,  77,  80,  83,  86,  89,  92,  95,
 98, 101, 104, 107, 109, 112, 115, 118,
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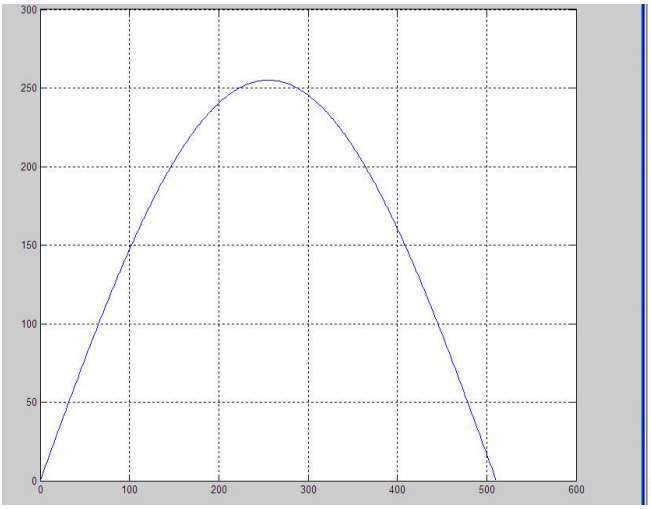
256-step Subdivision:

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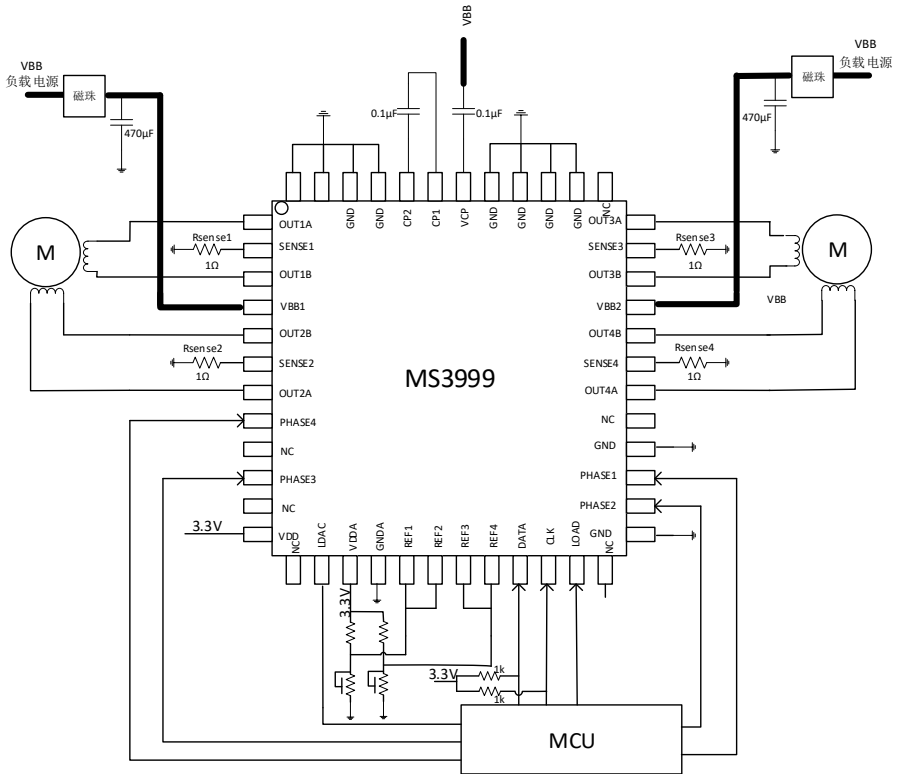
TYPICAL APPLICATION



DC Motor Control

The chip integrates four H-bridge drives, each of which is equipped with an independent PWM current control circuit, so it can drive four 1.2A current DC motors. In applications, the current and the PHASE pin can be set by four-channel DAC to control forward rotation, reverse rotation of the motor.

Layout Making

Heavy ground plane is required for printed circuit board. In order to achieve better performance and heat dissipation, the MS3999 should be directly soldered to the board. On the back of the MS3999 is a metal heat sink, which is directly soldered on the exposed PCB board to radiate heat to other layers.

Layout Ground Trace

In order to reduce ground drift, it is necessary to set one special ground trace with single point and low impedance near the chip in PCB. Generally, the ground wire position in contact with MS3999 heat sink and PCB is an ideal special ground wire position.

Special ground trace with low impedance could effectively avoid ground drift and ensure the stability of power supply.

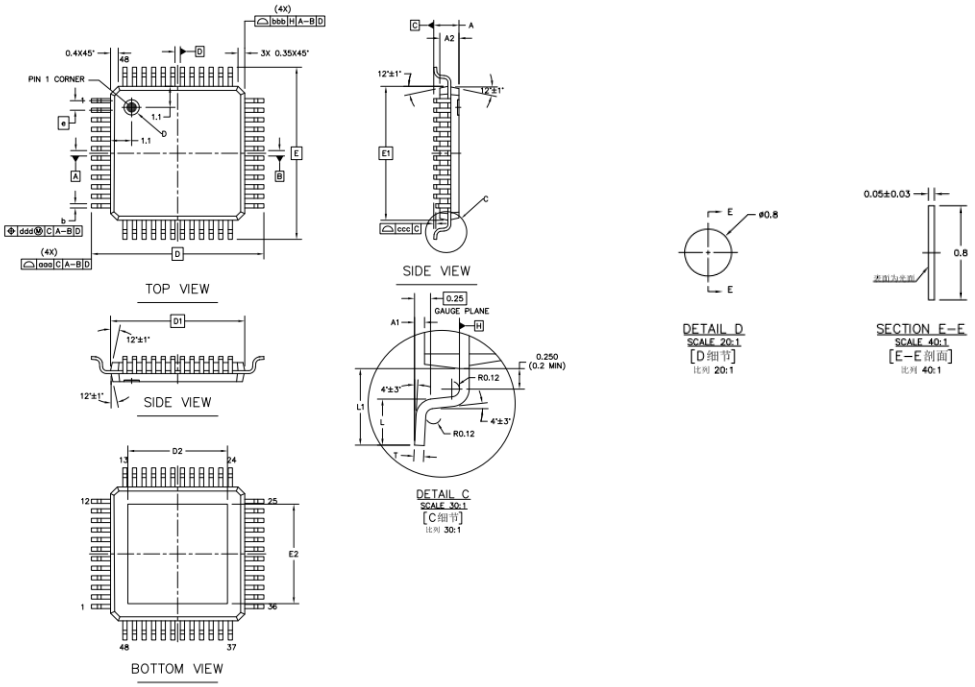
SENSE Pin Setting

Resistor RSx on the Sense pin must be connected to GND by a low resistance path. Because the large current flows though RSx ang generate a accurate feedback voltage to Sense comparator, forming the uncertain voltage drop to reduce the accuracy of Sense comparator.

When selecting the Sense resistor, please note that operating voltage on the Sense pin doesn't exceed ±500mV.

PACKAGE OUTLINE DIMENSIONS

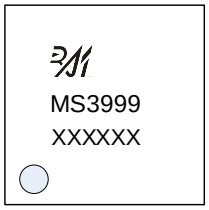
TQFP48



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.19	-	0.26
T	0.09	-	0.20
e	0.5BSC		
L	0.5	0.6	0.7
L1	1.0REF		
D	9BSC		
E	9BSC		
D1	7BSC		
E1	7BSC		
D2	5.1	5.2	5.3
E2	5.1	5.2	5.3
aaa	0.2		
bbb	0.2		
ccc	0.08		
ddd	0.08		

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS3999

Product Code: XXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Tray	Tray/Box	Piece/Box	Box/Carton	Piece/Carton
MS3999	TQFP48	250	10	2500	4	10000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1、The operator shall ground through the anti-static wristband.

2、The equipment shell must be grounded.

3、The tools used in the assembly process must be grounded.

4、Must use conductor packaging or anti-static materials packaging or transportation.

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http:// www.relmon.com