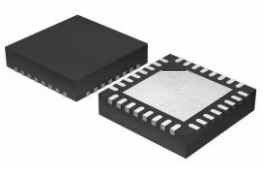
Dual-Channel, Ultra-Low Noise, 256 Microstepping, Low-Voltage Motor Driver

PRODUCT DESCRIPTION

The MS41929 is dual-channel, 5V low-voltage stepper motor driver. Ultra-low noise microstepping could be realized by voltage driving method with current microstepping and torque ripple correction technology.

The MS41929 has a built-in DC motor driver and the output resistance is low to 1.1Ω.

The MS41929 integrates crystal oscillator magnification module and can use passive crystal oscillator.



QFN32

FEATURES

- Voltage Driving Method, 256 Microstepping (Dual-channel)
- Maximum Driving Current ±0.5A for Each H-Bridge
- 4-Wire SPI Communication
- Built-in Dual-Chanel LED Driver (Open-drain Output)
- Built-in DC Motor Driver, Maximum Driving Current ±0.5A
- Passive Crystal Oscillator
- QFN32 Package (Back Thermal Pad)

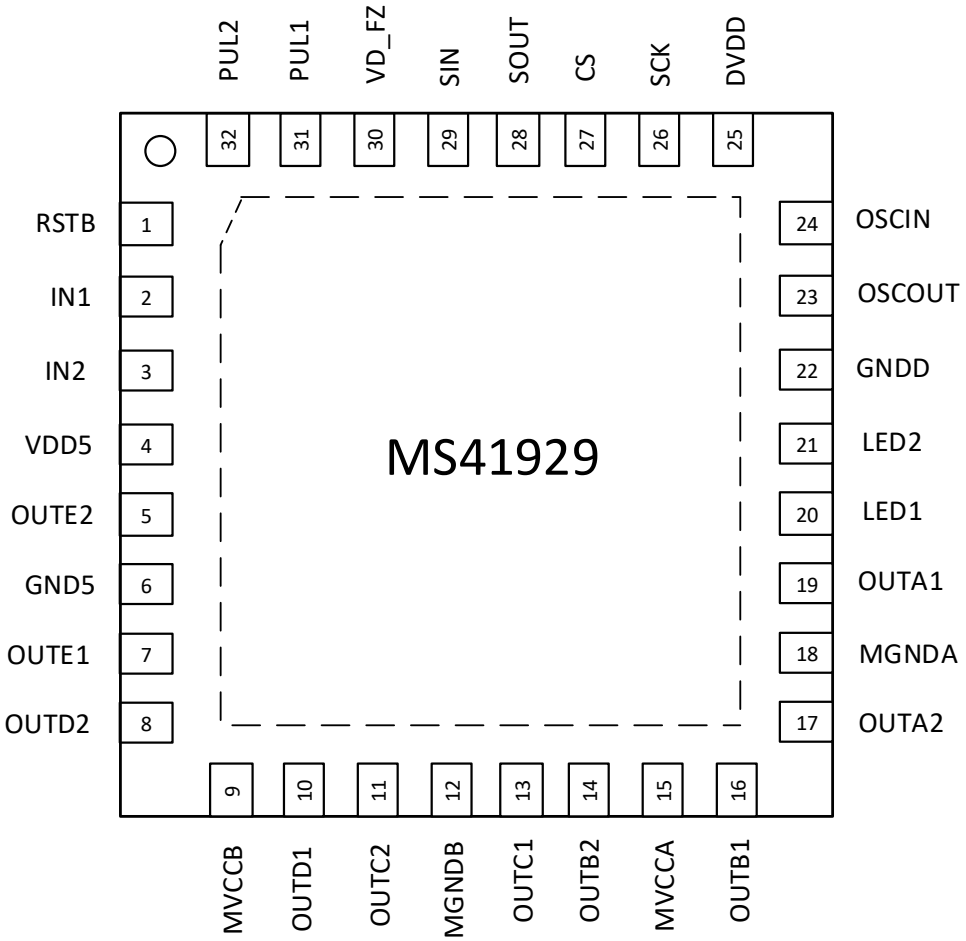
APPLICATIONS

- Robot, Precision Industry Device
- Camera
- Monitoring Camera

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS41929	QFN32	MS41929

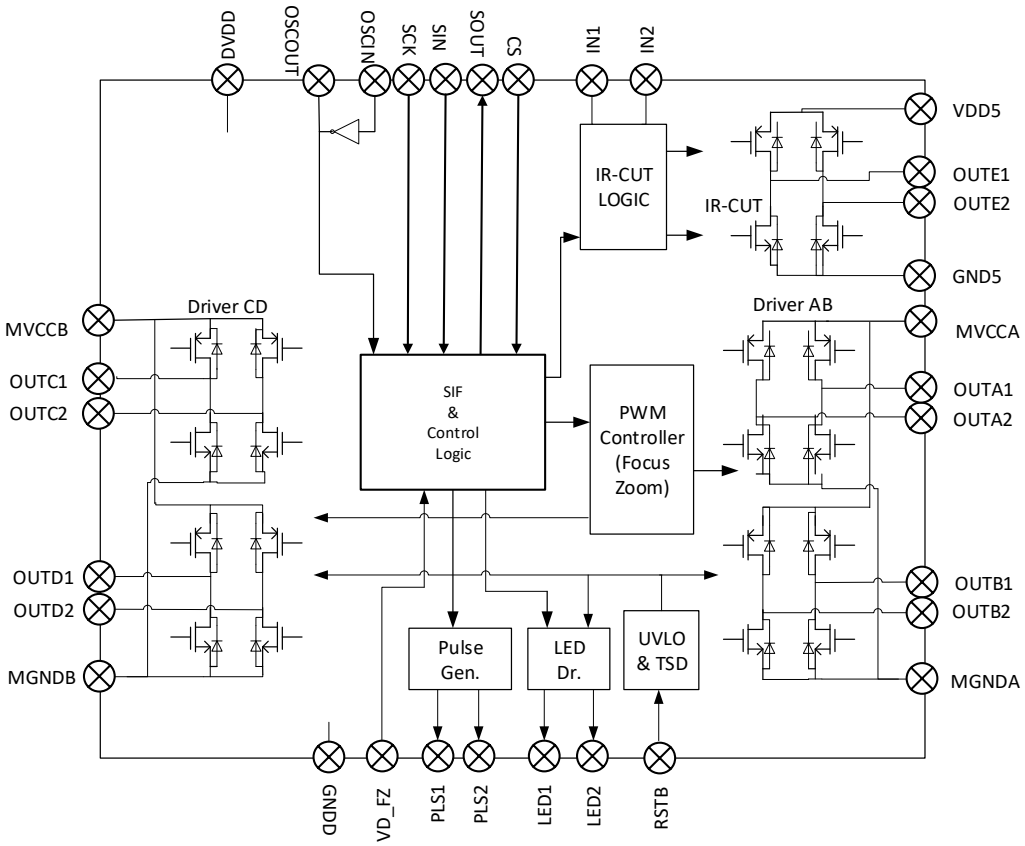
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	RSTB	I	Reset Signal Input
2	IN1	I	DC Motor Logic Input
3	IN2	I	DC Motor Logic Input
4	VDD5	-	DC Motor Power Supply E
5	OUTE2	O	Motor Output E2
6	GND5	-	DC Motor Ground E
7	OUTE1	O	Motor Output E1
8	OUTD2	O	Motor Output D2
9	MVCCB	-	Motor Power Supply B
10	OUTD1	O	Motor Output D1
11	OUTC2	O	Motor Output C2
12	MGNDB	-	Motor GNDB
13	OUTC1	O	Motor Output C1
14	OUTB2	O	Motor Output B2
15	MVCCA	-	Motor Power Supply A
16	OUTB1	O	Motor Output B1
17	OUTA2	O	Motor Output A2
18	MGNDA	-	Motor GND A
19	OUTA1	O	Motor Output A1
20	LED1	I	LED Driver Open-drain 1
21	LED2	I	LED Driver Open-drain 2
22	GNDD	-	Digital GND
23	OSCOUT	O	OSCIN Output
24	OSCIN	I	OSCIN Input
25	DVDD	-	3V Digital Power Supply
26	SCK	I	Serial Clock Input
27	CS	I	Chip Select Input
28	SOUT	O	Serial Data Output
29	SIN	I	Serial Data Input
30	VD_FZ	I	Stepper Motor Driver, Synchronous Signal Input
31	PLS1	O	Pulse 1 Output
32	PLS2	O	Pulse 2 Output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Ratings

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply, Analog and Control Part [1]	DVDD	-0.3 ~ +4.0	V
Load Power Supply 1 [1]	MVCCx VDD5	-0.3 ~ +6.0	V
Power Dissipation [2]	P_D	141.1	mW
Operating Temperature [3]	T_A	-40 ~ +100	°C
Storage Temperature [3]	T_{STG}	-65 ~ +150	°C
Junction Temperature	T_J	-40 ~ +150	°C
Stepper Motor, H-Bridge Drive Current	$I_{M1(CD)}$	±0.5	A/ch
Instantaneous H-Bridge Drive Current	$I_{M(pluse)}$	±0.6	A/ch
Input Voltage, Digital Part [4]	V_{IN}	-0.3 ~ (DVDD + 0.3)	V
ESD (HBM)	V_{ESD}	±3k	V

Note:

1. Absolute maximum ratings are used in the range of power dissipation.

2. Power dissipation refers to the value of encapsulated monomer at T_A=85°C. In practice, it is expected to refer to the technical data and P_D-T_A characteristic diagram on the basis of power supply, load, ambient temperature conditions, and then carry out the heat dissipation design which does not exceed the power dissipation value.

3. Except power dissipation, ambient temperature and storage temperature parameters, all parameters are at T_A=25°C.

4. (DVDD+0.3) voltage shall not exceed 4.0V.

Operating Power Supply

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	DVDD	2.7	3.3	3.6	V
	MVCCx	3.0	5	5.5	

Terminal Tolerance Current and Voltage Ranges

Note: 1. The parameters cannot exceed the absolute maximum ratings in any conditions.

2. Rated voltage value refers to each terminal voltage with respect to GND. GND is the voltage of GNDD, MGNDA, MGNDB, GND5. GND = GNDD = MGNDA = MGNDB=GND5.

3. 3V power is the voltage of DVDD.

4. Outside input voltage and current are strictly prohibited except the described terminals below.

5. For the current, "+" means the current flowing to IC, and "-" means the current flowing out from IC.

Pin	Name	Range	Unit
24	OSCIN	-0.3 ~ (DVDD + 0.3)	V
23	OSCOUT	-0.3 ~ (DVDD + 0.3)	V
27	CS	-0.3 ~ (DVDD + 0.3)	V
26	SCK	-0.3 ~ (DVDD + 0.3)	V
29	SIN	-0.3 ~ (DVDD + 0.3)	V
30	VD_FZ	-0.3 ~ (DVDD + 0.3)	V
1	RSTB	-0.3 ~ (DVDD + 0.3)	V
8	OUTD2	±0.5	A
10	OUTD1	±0.5	A
11	OUTC2	±0.5	A
13	OUTC1	±0.5	A
14	OUTB2	±0.5	A
16	OUTB1	±0.5	A
17	OUTA2	±0.5	A
19	OUTA1	±0.5	A
7	OUTE1	±0.5	A
5	OUTE2	±0.5	A
20	LED1	30	mA
21	LED2	30	mA

Note: (DVDD+0.3) voltage should not exceed 4.0V.

ELECTRICAL CHARACTERISTICS

MVCCx =VDD5= 5V, DVDD =3.3V. Unless other noted, T_A = 25°C ±2°C.

Current Consumption

Parameter	Symbol	Condition	Min	Typ	Max	Unit
MVCC Power Supply Current when Reset	$I_{Omdisable}$	Output Open-circuit,		0		μA
MVCC Power Supply Current when Enable	$I_{menable}$	27MHz Input		0.45		mA
DVDD Power Supply Current when Reset	$I_{cc3reset}$	Output Open-circuit,		445		μA
DVDD Power Supply Current when Enable	$I_{cc3enable}$	27MHz Input		2.8		mA
Power Supply Current when Standby	$I_{ccstandby}$	RSTB = High Output Open-circuit, 27MHz Input, Total Current		4		mA
Power Supply Current When FZ = Enable	I_{CCps}	RSTB = High Output Open-circuit, 27MHz Input, FZ = Enable, Total Current		5.5		mA

Digital Input and Output

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Voltage	$V_{in(H)}$	RSTB	0.54× DVDD		DVDD +0.3	V
Low-level Input Voltage	$V_{in(L)}$	RSTB	-0.3		0.25× DVDD	V
SOUT High-level Output	$V_{out(H)}$	I_{OUT}=1mA	DVDD -0.5			V
SOUT Low-level Output	$V_{out(L)}$	I_{OUT}=1mA			0.5	V
PLS1~2 High-level Output	$V_{out(H)}$		0.9× DVDD			V
PLS1~2 Low-level Output	$V_{out(L)}$				0.1× DVDD	V
Input Pull-down Impedance	$R_{pullret}$	RSTB		100		kΩ

Stepper Motor Driver (Focal Length and Zoom Control in Camera)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-side On Resistance	R_{onFZHS}	I_M = 200mA			0.8	Ω
Low-side On Resistance	R_{onFZLS}	I_M = 200mA			0.7	Ω
H-Bridge Leakage Current	I_{leakFZ}				1	μA

LED Driver

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On Resistance	R_{onLED}	I_M = 20mA		2		Ω
Output Leakage Current	$I_{leakLED}$				1	μA

DC Motor Driver (DRIVER E, IR-CUT in Camera)

Unless other noted, VDD5=5V, R_L=20Ω, T_A=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-side On Resistance	R_{oncuth}	I_{outE}=200mA		0.8		Ω
Low-side On Resistance	R_{oncutl}	I_{outE}=200mA		0.45		Ω
Output Leakage Current	I_{leakE}				1	μA
Output Enable Time	t7	Direct Input Mode, R_L=20Ω			300	ns
Output Disable Time	t8	Direct Input Mode, R_L=20Ω			300	ns
Delay Time, Inx Rising to outx Rising	t9	Direct Input Mode, R_L=20Ω			160	ns
Delay Time, Inx Falling to outx Falling	t10	Direct Input Mode, R_L=20Ω			160	ns
Outx Rise Time	t11	Direct Input Mode, R_L=20Ω	30		188	ns
Outx Fall Time	t12	Direct Input Mode, R_L=20Ω	30		188	ns
Delay Time, SPI Input to H-Bridge Output	t13	SPI Input Mode, R_L=20Ω		25×t_{SCK}		s

Digital Input/Output

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input	$V_{in(H)}$	SCK,SIN,CS,VD_FZ	0.54× DVDD			V
Low-level Input	$V_{in(L)}$	SCK,SIN,CS,VD_FZ			0.25× DVDD	V
OSC DC Coupled Input Amplitude	V_{oscDC}	Use external clock, DC coupled input to OSCOUT, Minimum amplitude	2.4			V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OSC AC Coupled Input Amplitude	V_{oscAC}	Use external clock, AC coupled input with 0.1μF capacitor	1			V
RSTB Signal Pulse	t_{rst}		100			μs
Input Maximum Hysteresis Error	V_{hysin}	SCK,SIN,CS,VD_FZ		0.34		V
Image Synchronous Signal Width	VD_w		80			μs
CS Signal Wait Signal 1	$t_{(VD-CS)}$		400			ns
CS Signal Wait Signal 2	$t_{(CS-DT1)}$		5			μs

Thermal Shutdown

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Temperature for Thermal Shutdown	T_{tsd}			145		°C
Maximum Hysteresis Error for Thermal Shutdown	ΔT_{tsd}			35		°C

Power Supply Monitor Circuit

Parameter	Symbol	Condition	Min	Typ	Max	Unit
3.3V Reset	V_{rston}			2.48		V
3.3V Reset Maximum Hysteresis Error	V_{rsthys}			0.2		V
MVCCx Reset	$V_{rstFZon}$			2.42		V
MVCCx Reset Maximum Hysteresis Error	$V_{rstFZhys}$			0.21		V

FUNCTION DESCRIPTION

1. Serial Interface

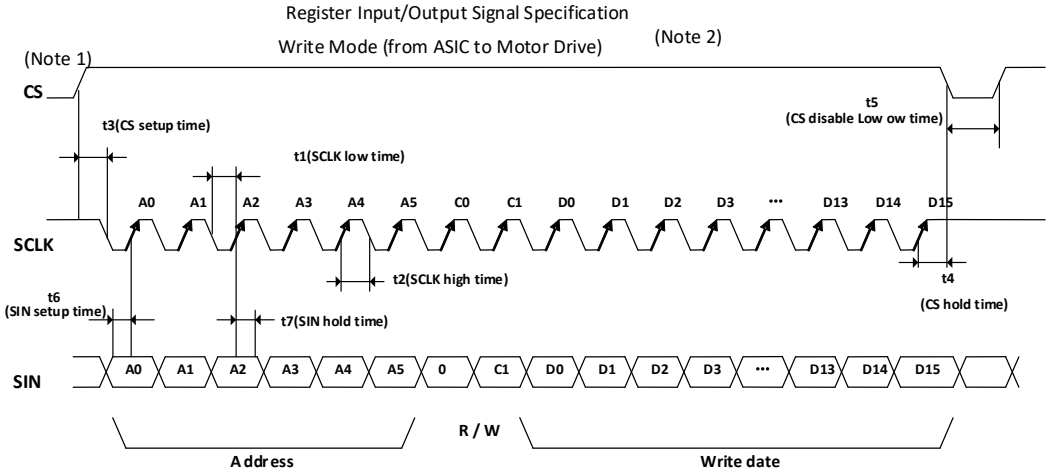


Figure 1. Data Write

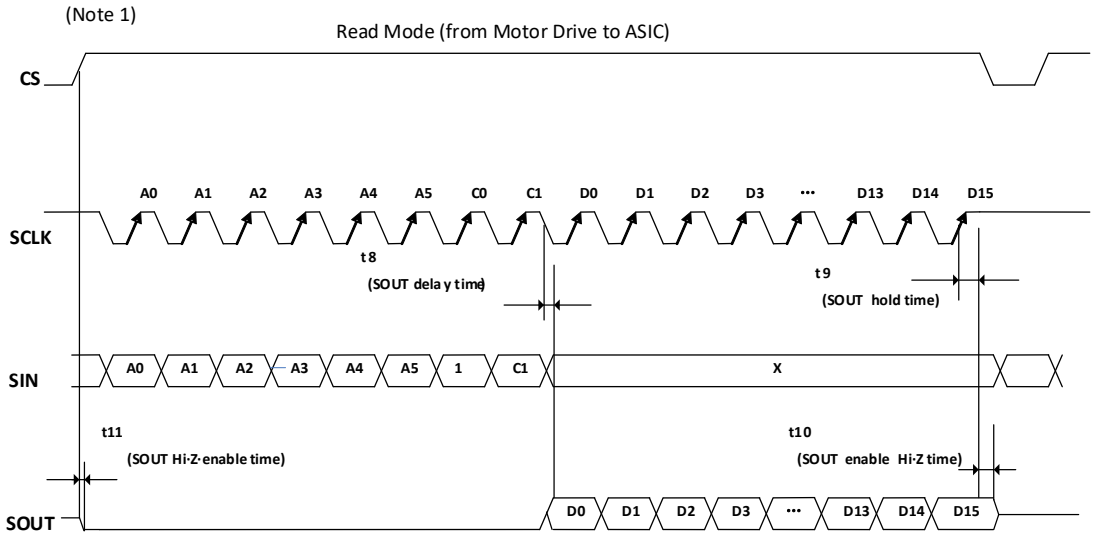


Figure 2. Data Read

Note: 1. In read/write mode, CS starts from 0 by default every cycle.

2. When in write mode, the system clock must be input from OSCIN terminal.

Electrical Parameters (Design Reference)

VDD5=MVCCx =5V, DVDD = 3.3V.

Unless other noted, T_A = 25°C ±2°C. The characteristics are only design values and only for references.

1.1 Serial Port Input

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Serial Clock	Sclock		1		5	MHz
SCK Low Time	t1		100			ns
SCK High Time	t2		100			ns
CS Setup Time	t3		60			ns
CS Hold Time	t4		60			ns
CS Low Time	t5		100			ns
SIN Setup Time	t6		50			ns
SIN Hold Time	t7		50			ns
SOUT Delay Time	t8				60	ns
SOUT Hold Time	t9		60			ns
SOUT Enable-Hi-Z Time	t10				60	ns
SOUT Hi-Z-Enable Time	t11				60	ns
SOUT Capacitor Load	tsc				40	pF

1. The data conversion starts on the rising edge of CS and stops on the falling edge of CS.

2. The data stream unit of a conversion is 24 bits.

3. When the address and data are input from the SIN pin, the clock signal SCK remains consistent under the condition of CS=1.

4. The data is driven into IC on the rising edge of SCK signal. At the same time, when the data is output, it is read out from SOUT pin (the data is output on the rising edge of SCK).

5. SOUT outputs a high impedance state when CS=0, and when CS = 1, outputs "0" unless there is a data read.

6. The control of entire serial interface is reset when CS=0.

1.2 Data Format

0	1	2	3	4	5	6	7
A0	A1	A2	A3	A4	A5	C0	C1

8	9	10	11	12	13	14	15
D0	D1	D2	D3	D4	D5	D6	D7

16	17	18	19	20	21	22	23
D8	D9	D10	D11	D12	D13	D14	D15

C0: Register Read and Write Options: 0: Write Mode, 1: Read Mode

C1: Not Use

A5~A0: Register Address

D15~D0: Data Written to Register

1.3 Register Map

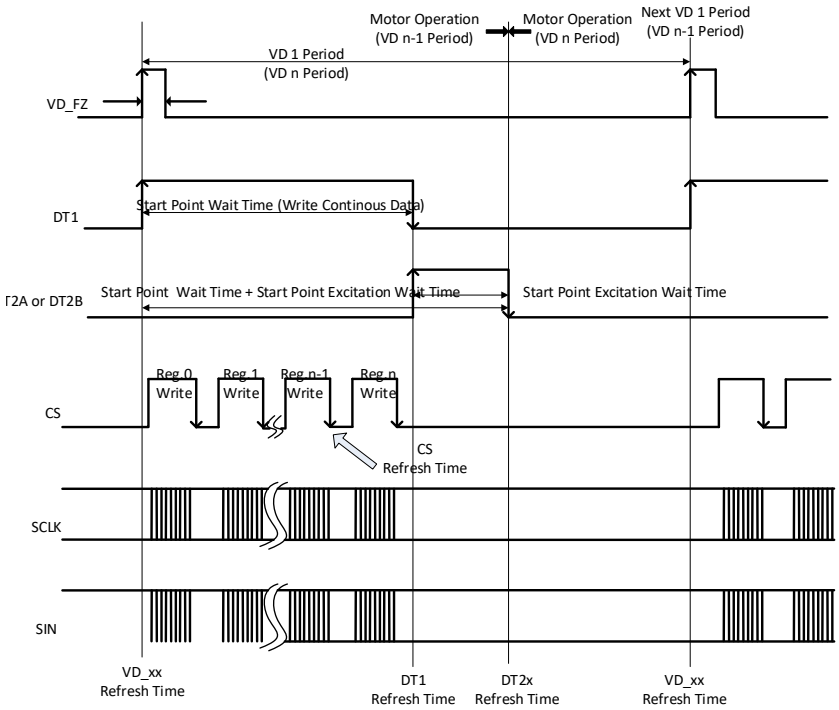
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Reserved						MODE SEL_FZ	Reserved	TEST EN1			Reserved				
20H		PWMRES [1:0]		PWMMODE[4:0]					DT1[7:0]							
21H									TEST EN2			FZTEST[4:0]				
22H			PHMODAB[5:0]						DT2A[7:0]							
23H	PPWB[7:0]								PPWA[7:0]							
24H			MICROAB [1:0]		LEDB	ENDISAB	BRAKE AB	CCWCW AB	PSUMAB[7:0]							
25H	INTCTAB[15:0]															
27H			PHMODCD[5:0]						DT2B[7:0]							
28H	PPWD[7:0]								PPWC[7:0]							
29H			MICROCD [1:0]		LEDA	ENDISCD	BRAKE CD	CCWCW CD	PSUMCD[7:0]							
2AH	INTCTCD[15:0]															
2CH														IN SWICH	IN1	IN2

1.4 Register List

Address	Register Name/Bit Width	Description	Page
0Bh	TESTEN1	TEST Mode Enable 1	27
	MODESEL_FZ	VD_FZ Polarity Select	16
20h	DT1[7:0]	Start Point Wait Time	19
	PWMMODE[4:0]	Microstep Output PWM Frequency	20
	PWMRES[1:0]	Microstep Output PWM Resolution	20
21h	FZTEST[4:0]	PLS1/2 Output Signal Select	27
	TESTEN2	TEST Mode Enable 2	27
22h	DT2A[7:0]	Start Point Excitation Wait Time (α Motor)	20
	PHMODAB[5:0]	Phase Correction (α Motor)	21
23h	PPWA[7:0]	Peak Pulse Width of A Channel	22
	PPWB[7:0]	Peak Pulse Width of B Channel	22
24h	PSUMAB[7:0]	Step Number of Stepper Motor (α Stepper Motor)	23
	CCWCWAB	Rotation Direction (α Motor)	24
	BRAKEAB	Brake State (α Motor)	24
	ENDISAB	Enable/Disable (α Motor)	24
	LEDB	LED B Output Control	29
	MICROAB[1:0]	Sine Wave Microstep (α Motor)	25
25h	INTCTAB[15:0]	Microstep Cycle (α Motor)	25
27h	DT2B[7:0]	Start Point Excitation Wait Time (β Motor)	20
	PHMODCD[5:0]	Phase Correction (β Motor)	21
28h	PPWC[7:0]	Peak Pulse Width of C Channel	22
	PPWD[7:0]	Peak Pulse Width of D Channel	22
29h	PSUMCD[7:0]	Step Number of Stepper Motor (β Stepper Motor)	23
	CCWCWCD	Rotation Direction (β Motor)	24
	BRAKECD	Brake State (β Motor)	24
	ENDISCD	Enable/Disable (β Motor)	25
	LEDA	LED A Output Control	29
	MICROCD[1:0]	Sine Wave Microstep (β Motor)	25
2Ah	INTCTCD[15:0]	Microstep Cycle (β Motor)	25
2Ch	INSWICH	DC Motor Enable	
	IN1	DC Motor Input Control 1	
	IN2	DC Motor Input Control 2	

All register bit data is initialized at RSTB = 0.

1.5 Register Setup Time



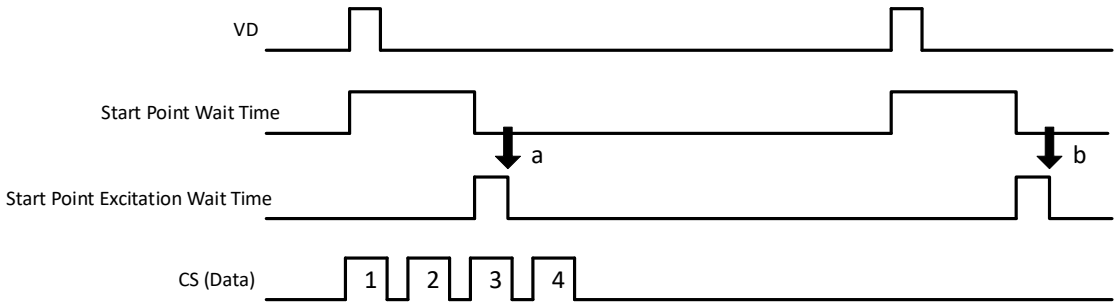
Address	Name	Setup Time
0Bh	TESTEN1	CS
	MODESEL_FZ	CS
20h	DT1[7:0]	VD_FZ
	PWMMODE[4:0]	DT1
	PWMRES[1:0]	DT1
21h	FZTEST[4:0]	CS
	TESTEN2	CS
22h	DT2A[7:0]	DT1
	PHMODAB[5:0]	DT2A
23h	PPWA[7:0]	DT1
	PPWB[7:0]	DT1
24h	PSUMAB[7:0]	DT2A
	CCWCWAB	DT2A
	BRAKEAB	DT2A
	ENDISAB	DT1 or DT2A*
	LEDB	CS
	MICROAB[1:0]	DT2A

Address	Name	Setup Time
25h	INTCTAB[15:0]	DT2A
27h	DT2B[7:0]	DT1
	PHMODCD[5:0]	DT2B
28h	PPWC[7:0]	DT1
	PPWD[7:0]	DT1
29h	PSUMCD[7:0]	DT2B
	CCWCWCD	DT2B
	BRAKECD	DT2B
	ENDISCD	DT1 or DT2B*
	LEDA	CS
	MICROCD[1:0]	DT2B
2Ah	INTCTCD[15:0]	DT2B

* 0→1: it works on DT1; 1→0: it works on DT2x

In principle, the setup of registers for microsteps should be completed during the time period when the start point is delayed (see figure on page 14). Data written outside the start delay can also be stored in registers. However, if the write operation is executed after the refresh time, the written register will not be valid at the scheduled time. For example, if the updated data 1~4 is written as shown in the following figure after the start point excitation delay, data 1 and 2 are immediately updated at time a, and data 3 and 4 are updated at time b. Even if the data is written continuously, the update time interval is 1 VD cycle.

For the above reasons, in order to update data timely, the establishment of the register data needs to be completed during the start point delay.



2. VD Internal Process

In this system, the response time and rotation time of stepper motor are respectively based on the rising edge of VD_FZ. The polarity of VD_FZ is set by the following registers.

Register Detail

MODESEL_FZ (VD_FZ Polarity Select)

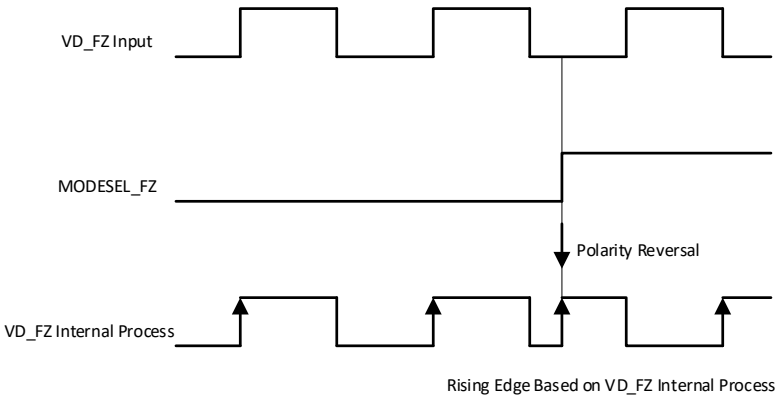
Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						MODESEL_FZ									

MODESEL_FZ sets the VD_FZ polarity.

When set to "0", the polarity is based on the rising edge of VD_FZ. When set to "1", the polarity is based on the falling edge of VD_FZ.

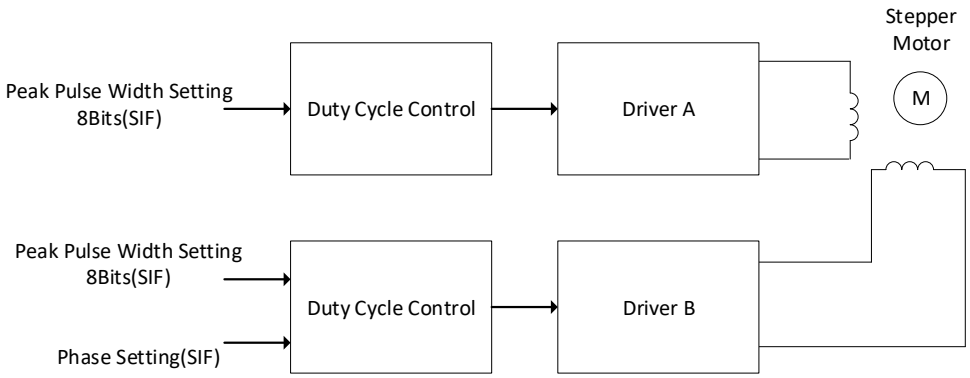
MODESEL_FZ selects the polarity of input VD_FZ. Based on MODESEL_FZ select time, the edge would be generated as shown below and is independent of VD_FZ edge.

Set Value	VD Polarity
0	Non-inverting
1	Inverting



3. Stepper Motor Microstep Driver

3.1 Block Diagram



The block for stepper motor driver used to focus and magnify. The following settings can be used to perform a series of controls. The following is the description of the motor α: driver A/B. C, D perform the same algorithm as the motor α.

Main Setting Parameters:

Phase correction: The phase difference between driver A and driver B is targeted on 90°, and can be adjusted from -22.5° to +21.8°.	——>PHMODAB[5:0]
Amplitude Setting: Set the load current of driver A/B independently	——>PPWA[7:0],PPWB[7:0]
PWM Frequency: PWM frequency setting of driver output	——>PWMMODE[4:0],PWMRES[1:0]
Microstep Number: Can be set to 64,128, 256	——>MICROAB[1:0]
Step Cycle: Motor Rotation Speed Setting. It is independent of microstep mode of sine wave.	——>INTCTAB[15:0]

3.2 Setup Time of Related Settings

The setup time and related time are shown below.

Because the settings of 27h to 2Ah are same as 22h to 25h, the description for 27h to 2Ah is ignored. If the related registers are updated, a setting load refresh is implemented for each VD cycle. When the same setting is executed with more than 2VD pulses, it is not necessary to write register data on each VD pulse.

DT1[7:0] (Start Point Delay, Address 20h)

Update data time setting. It must be set after the system hardware reset (Pin RSTB: Low → High), before starting excitation and driving motor (DT1 ends).

Since this setting is updated every time a VD pulse comes, it is not necessary to write during the start point delay.

PWMMODE[4:0], PWMRES[1:0] (Microstep Output PWM Frequency, Address 20h)

Set PWM frequency of the microstep output. Need to be set to execute before starting excitation and driving motor (DT1 ends).

DT2A[7:0] (Start Point Excitation Delay, Address 22h)

Update data time setting. It must be set after reset (Pin RSTB: Low → High), before starting excitation and driving motor (DT1 ends).

PHMODAB[5:0] (Phase Correction, Address 22h)

By correcting the phase difference between coils A and B, the driver produces less noise.The appropriate phase correction must be based on the rotation direction and speed. This setting needs to change with the rotation direction (CCWCWAB) or the rotation speed (INTCTAB).

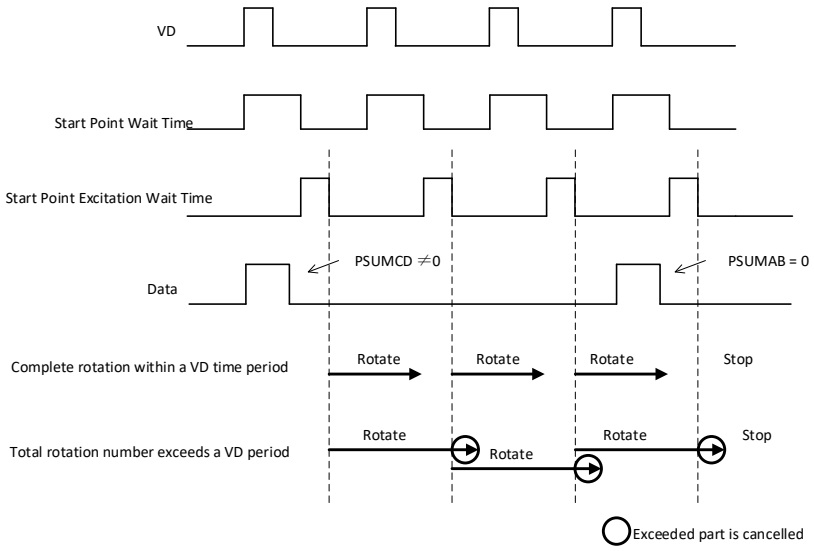
PPWA[7:0],PPWB[7:0] (Peak Pulse Width, Address 23h)

Set the PWM maximum duty cycle. Setting needs to be set before starting excitation and driving motor (DT1 ends).

PSUMAB[7:0] (Step Number of Stepper Motor, Address 24h)

The rotation number of the motor is set within 1 VD time interval.

The number of the motor rotation is set when each VD pulse is input. Therefore, setting the time to "0" can stop the motor rotation. When the total number of rotations exceeds the time of 1 VD pulse, the exceeded part will be canceled.



CCWCWAB (Rotation Direction, Address 24h)

Motor rotation direction setting. Just set it before selecting the rotation direction.

BRAKEAB (Motor Brake Setting, Address 24h)

Set the current to 0 when braking. This setting is generally used to stop the motor immediately because it is difficult to obtain final position when this setting is performed.

ENDISAB (Motor Operation Enable/Disable, Address 24h)

Set the motor work enable. When set to disable, the motor pin outputs high impedance state, and should not be set to disable while the motor is rotating.

LEDA (LED Setting, Address 24h)

LED on/off setting. It is set on the falling edge of CS. It is independent of motor driver and achieved by independent setting,

MICROAB[1:0] (Sine Wave Frequency Division, Address 24h)

Set the frequency division number of sine wave. This setting does not change the number and speed of rotation. It is set only when the rotation speed doesn't reach the demand. After reset (Pin RSTB: Low→High), setting is effective.

INTCTAB[15:0] (Pulse Period, Address 25h)

Pulse period setting. The rotation speed depends on this setting.

3.3 How to adjust the register value when the stepper motor is driven by microstep

In order to control lens, it is required to set the number and speed of motor rotation for each VD.The related registers are:

INTCTxx[15:0]: Set the time of each step (corresponding to the rotation speed)

PSUMxx[7:0]: Total number of rotation steps in each VD period

When the motor is continuously driven in a continuous VD period, the continuous rotation time needs to be set to adapt to the VD period.

The followings are how to calculate INTCTxx[15:0] and PSUMxx[7:0] when the motor is rotating.

1) Calculate INTCTxx[15:0] (determine the motor rotation speed)

INTCTxx[15:0] × 768 = OSCIN Frequency/Rotation Frequency

2) PSUMxx[7:0] is calculated by INCTxx[15:0]. Don't just only look at the value of PSUMxx[7:0].

When the following equation holds, the continuous rotation time and VD time are same, and the motor achieves uniform rotation.

INTCTxx[15:0] × PSUMxx[7:0] × 24 = OSCIN Frequency/ VD Frequency

3) After the setting of PSUMxx[7:0] is completed, INTCTxx[15:0] is recalculated from above formula.

For example, OSCIN Frequency = 27MHz, VD Frequency = 60Hz

Calculate PSUMxx[7:0] and INTCTxx[15:0] to make the motor rotate at 800pps (1-2 phase), 800pps is equal to 100Hz, so

INTCTxx[15:0] = 27MHz / (100Hz × 768) =352

Corresponding

PSUMxx[7:0] = 1/(60Hz)×27MHz/ (352 ×24) = 53

Recalculate INTCTxx[15:0]:

PSUMxx[7:0] = 1/(60Hz)×27MHz/ (53 ×24) = 354

If the left side of the equation in 2) is smaller than the right side, the rotation time is smaller than the VD period, which will cause discontinuous rotation. On the contrary, rotation beyond VD time period will be canceled.

3.4 Register Detail

DT1[7:0] (Start Point Wait Time)

Address			20h			Initial Value			0Ah						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT1[7:0]							

DT1[7:0] sets the delay time of data writing to the system (start point wait time)

The motor can be activated precisely after the start point wait time is flipped from "1" to "0". The start point wait time is calculated from the rising edge of the synchronization video signal (VD_FZ).

Because the start point delay time is mainly used to wait for the serial data to be written. The register value should be set to greater than "0". If it is "0", the corresponding data cannot be updated.

Refer to page 14 for the relationship between VD_FZ and the start point wait time.

DT1	Start Point Wait
0	Prohibit
1	303.4μs
255	77.4ms
n	n×8192/27MHz

DT2A[7:0] (Start Point Excitation Wait Time Motor α)

Address			22h			Initial Value			03h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2A[7:0]							

DT2B[7:0] (Start Point Excitation Wait Time Motor β)

Address			27h			Initial Value			03h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2B[7:0]							

DT2A[7:0] and DT2B[7:0] set the wait delay time before the motor α and motor β start to rotate.

The motor starts to rotate after the start point excitation wait time is flipped from "1" to "0". The start point excitation wait time starts to calculate at the end of start point wait time.

This signal is a separate delay for AB. The register value should be set to greater than "0". If it is "0", the corresponding data can't be updated.

Refer to page 14 for the relationship between VD_FZ and the start point excitation wait time.

DT2	Start Point Excitation Wait
0	Prohibit
1	303.4μs
255	77.4ms
n	n×8192/27MHz

PWMMODE[4:0] (Microstep Output PWM Frequency)

Address			20h			Initial Value			1Ch						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			PWMMODEAB[4:0]												

PWMRES[1:0] (Microstep Output PWM Resolution)

Address			20h			Initial Value			1						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	PWMRES														

PWMMODE[4:0] sets the microstep output PWM frequency by setting the frequency division of system clock OSCIN.

PWMMODE[4:0] can be set in the range of 1 to 31. The frequency of PWM wave is same when PWMMODE = 0 and PWMMODE = 1.

PWM frequency is decided by PWMRES[1:0] and PWMMODE[4:0].

The PWM frequency is calculated by the following formula

$$\text{PWM Frequency} = \text{OSCIN Frequency} / ((\text{PWMMODE} \times 2^3) \times 2^{\text{PWMRES}})$$

When OSCIN=27MHz, PWM frequency is shown in the following table (kHz)

PWMMODE	PWMRES			PWMMODE	PWMRES		
	0	1	2		0	1	2
1	3375.0	1687.5	843.8	17	198.5	99.3	49.6
2	1687.5	843.8	421.9	18	187.5	93.8	46.9
3	1125.0	526.5	281.3	19	177.6	88.8	44.4
4	843.8	421.9	210.9	20	168.8	84.4	42.2
5	675.0	337.5	168.8	21	160.7	80.4	40.2
6	526.5	281.3	140.6	22	153.4	76.7	38.4
7	482.1	241.1	120.5	23	146.7	73.4	36.7
8	421.9	210.9	105.5	24	140.6	70.3	35.2
9	375.0	187.5	93.8	25	135.0	67.5	33.8
10	337.5	168.8	84.4	26	129.8	64.9	32.5
11	306.8	153.4	76.7	27	125.0	62.5	31.3
12	281.3	140.6	70.3	28	120.5	60.3	30.1
13	259.6	129.8	64.9	29	116.4	58.2	29.1
14	241.1	120.5	60.3	30	112.5	56.3	28.1
15	225.0	112.5	56.3	31	108.9	54.4	27.2
16	210.9	105.5	52.7				

PHMODAB[5:0] (Motor α Phase Correction)

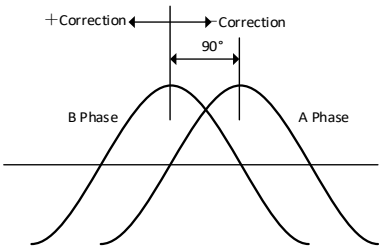
Address			22h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODAB[5:0]													

PHMODCD[5:0] (Motor β Phase Correction)

Address			27h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODCD[5:0]													

The current phase difference in motor α and motor β is set by PHMODAB[5:0] and PHMODCD[5:0] respectively. The default value is 90° and set 1 unit to 0.7°. Meanwhile, the data can be subject to positive and negative deviation.

PHMODAB	Phase Correction Number
000000	±0°
000001	+0.7°
011111	+21.80°
100000	-22.50°
111111	-0.7°
Damping Unit	360°/512 = 0.70°



The phase difference between the stepper motor coils is generally 90°. However, due to different motors or process deviations, the phase difference will also be shifted by 90°. Therefore, even if the phase difference of the drive waveform current is 90°, the motor itself is not 90° difference, it will produce torque ripple, and the noise still exists.

The main purpose of this setting is to reduce the torque ripple caused by motor changes.

PPWA[7:0] (Peak Pulse Width for Driver A)

PPWB[7:0] (Peak Pulse Width for Driver B)

Address			23h			Initial Value			0,0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWB[7:0]									PPWA[7:0]						

PPWC[7:0] (Peak Pulse Width for Driver C)

PPWD[7:0] (Peak Pulse Width for Driver D)

Address			28h			Initial Value			0,0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWD[7:0]									PPWC[7:0]						

The maximum duty cycle of the PWM wave is set by PPWA[7:0] to PPWD[7:0], which determines the position of the peak output current from driver A to D.

The maximum duty cycle is calculated by the following equation:

$$\text{Driver} \times \text{Maximum Duty Cycle} = PPWx / (PWMMODE \times 8)$$

When PPWx = 0， coil current is 0.

For example, when PPWA[7:0]=200, PWMMODE[4:0]=28, maximum duty cycle is:

$$200 / (28 \times 8) = 0.89$$

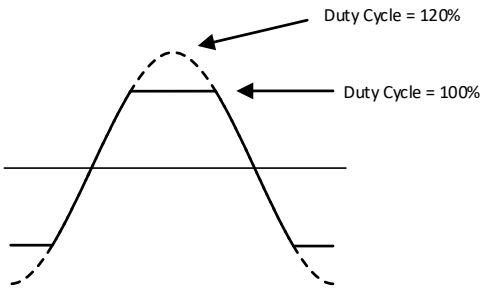
Depending on the values of PWMMODE and PPWx, the maximum duty cycle may exceed 100%.

Of course, the duty cycle cannot exceed 100% in fact and the peak point of sine wave will be truncated as shown in the following figure.

For example, when PWMMODE = 10, PPWx = 96,

Maximum Duty Cycle = 90/(10 × 8) = 120%

The waveform of the target current is shown as follows:



PSUMAB[7:0] (Step Number of Motor α)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMAB[7:0]							

PSUMCD[7:0] (Step Number of Motor β)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMCD[7:0]							

PSUMAB[7:0] and PSUMCD[7:0] set the total step number of the motor α and motor β respectively.

If want to stop the motor, set PSUMxx[7:0]=0.

Register Value	Total Step Number		
	64 Microstep	128 Microstep	256 Microstep
0	0	0	0
1	2	4	8
255	510	1020	2040
n	2n	4n	8n

As long as the maximum duty cycle of PWM wave is not set as "0", when PSUMxx[7:0]=0, the motor can keep in the release state.

An example to know the meaning of setting:

When PSUMAB[7:0]=8 is set, run 16 steps in 64 microstep mode, i.e. 16/64=1/4 sine cycle. Similarly, in 128 and 256 microstep modes, it is also a quarter of the period of sine wave.

CCWCWAB (Rotation Direction of Motor α)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CCWCWAB								

CCWCWCD (Rotation Direction of Motor β)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CCWCWCD								

CCWCWAB and CCWCWCD set the rotation direction of the motor α and motor β respectively.

Direction Definition:

Set Value	Motor Rotation Direction
0	Forward
1	Reverse

BRAKEAB (Brake State of Motor α)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						BRAKEAB									

BRAKECD (Brake State of Motor β)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						BRAKECD									

BRAKEAB and BRAKECD set the brake mode of the motor α and motor β respectively.

Set Value	Motor Brake
0	Normal State
1	Brake State

In brake state, the two high-side PMOS FETs of H-bridge are all turned on. The brake mode cannot be used in normal operation and can only be used during emergency shutdown. It is recommended to use in abnormal state.

ENDISAB (Motor α Enable/Disable)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISAB										

ENDISCD (Motor β Enable/Disable)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISCD										

ENDISAB and ENDISCD set the output control of the motor α and motor β respectively.

When ENDISxx = 0, motor outputs high impedance state. However, internal excitation position counter still keeps counting at ENDISxx=0. Therefore, when the motor is needed to stop in normal state, set PSUMxx[7:0] = 0 instead of ENDISxx = 0.

Set Value	Motor Output State
0	Output Off (High-impedance State)
1	Output On

MICROAB[1:0] (Sine Wave Frequency Division of Motor α)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROAB[1:0]													

MICROCD[1:0] (Sine Wave Frequency Division of Motor β)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROCD[1:0]													

MICROAB and MICROCD set the frequency division of sine wave for motor α and motor β respectively.

The 64 division waveform is shown on page 26.

MICROAB	Frequency Division
00	256
01	256
10	128
11	64

INTCTAB[15:0] (Step Cycle of Motor α)

Address			25h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTAB[15:0]															

INTCTCD[15:0] (Step Cycle of Motor β)

Address			2Ah			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTCD[15:0]															

INTCTAB[15:0] and INTCTCD[15:0] set a microstep cycle of the motor α and motor β respectively .

Register Value	Total Step Number		
	64 Microstep	128 Microstep	256 Microstep
0	0	0	0
1	444ns	222ns	111ns
Max	29.1ms	14. 6ms	7.3ms
n	12n/27MHz	6n/27MHz	3n/27MHz

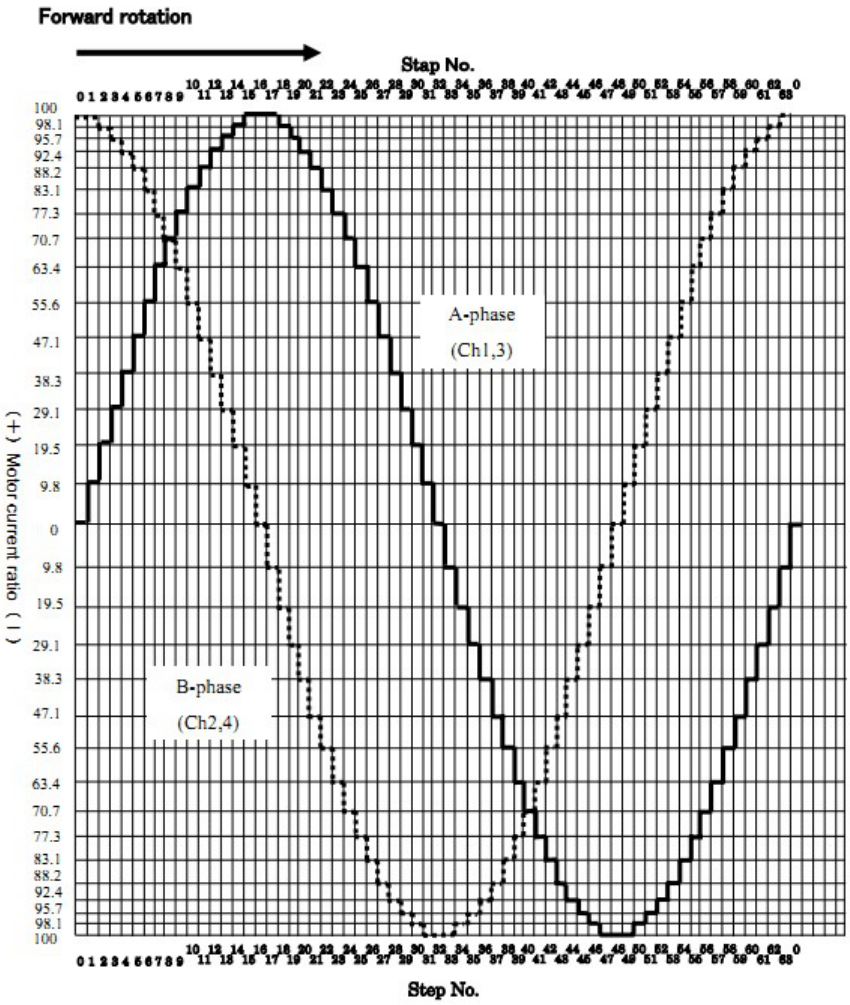
When INTCTAB[15:0]=0, as long as PWM maximum duty cycle is not 0, the motor will remain in release state .

For example: when INTCTAB[15:0]=400, step cycle in 64 microstep:

$$12\times400/27MHz=0.178ms$$

Therefore, the period of each sine wave is 11.4ms (87.9Hz). Similarly, in 128 microstep or 256 microstep, it is also 11.4ms.

Stepper Motor Driver (64 Microstep Current Curve)



4. Test Signal

FZTEST[4:0] (Test Signal Output Setting)

Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											FZTEST[4:0]				

TESTEN1 (Test Setting 1)

Address			0Bh			Initial Value			0			TESTEN2			
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN1							

TESTEN2 (Test Setting 2)

Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN2							

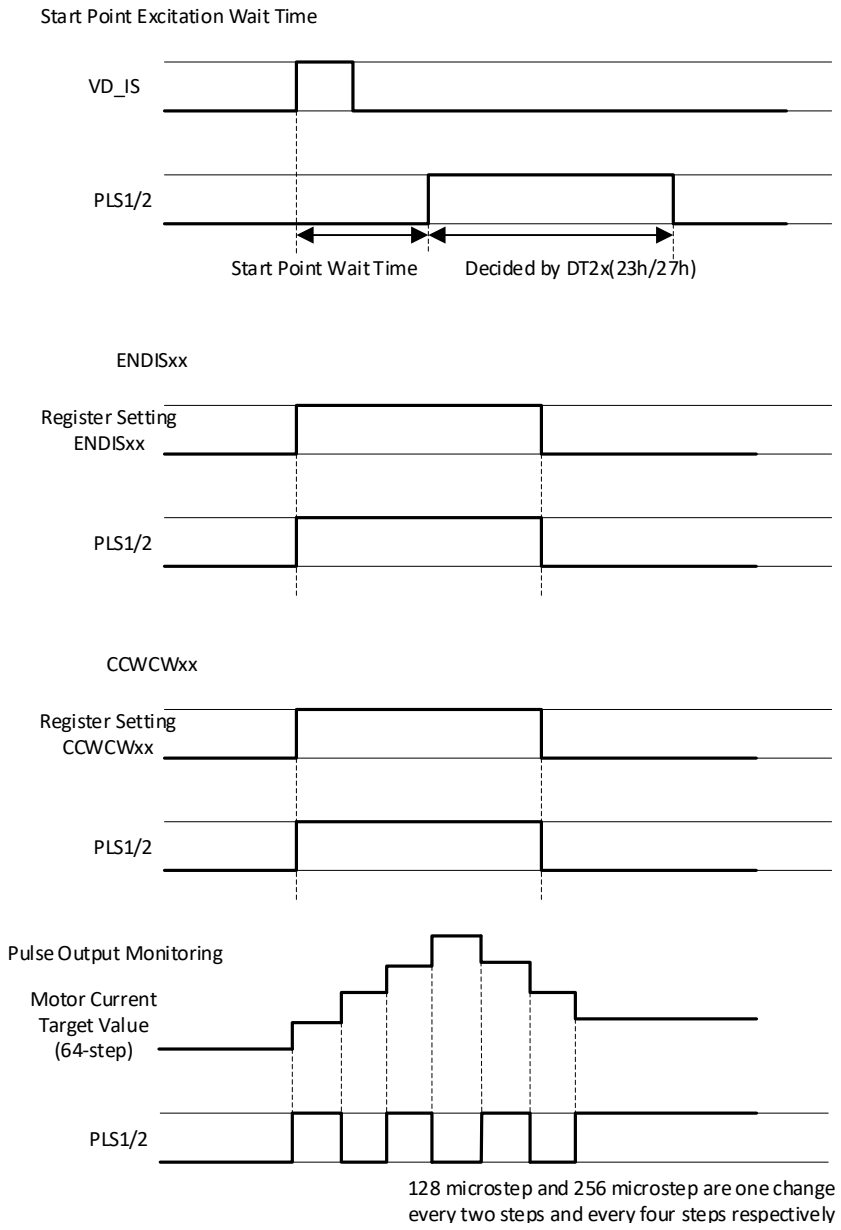
FZTEST[4:0] selects the test signals output by PLS1 and PLS2.

TESTEN1 and TESTEN2 need to be set to "1" to allow the test signal output.

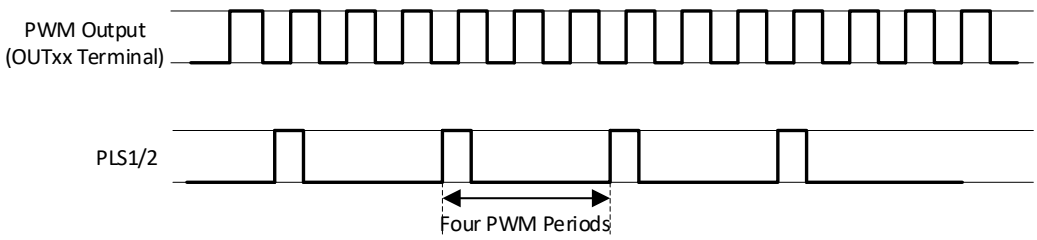
The following table is the output setting signal.

Setting	A Cycle		Description
	PLS1	PLS2	
1	Start Point Wait Time	0	H-Bridge Output for Start Point Wait Time
2	Start Point Excitation Wait Time A	Start Point Excitation Wait Time B	H-Bridge Output for Start Point Excitation Wait Time
3	ENDISAB	ENDISCD	ENDISxx Setting
4	CCWCWAB	CCWCWCD	CCWCWxx Setting
5	Monitor Output Pulse A	Monitor Output Pulse B	“H”/“L” change in 64 microstep when motor is rotating
6	PWM Period Monitoring	0	PWM Period Signal of Motor Output
7	Complete Pulse Output for Driver A	Complete Pulse Output for Driver B	H-Bridge Output when Motor Rotating
11	“H”Bridge PMOS1 A	“H”Bridge NMOS1 A	Monitor Driver A
12	“H”Bridge PMOS2 A	“H”Bridge NMOS2 A	
13	“H”Bridge PMOS1 B	“H”Bridge NMOS1 B	Monitor Driver B
14	“H”Bridge PMOS2 B	“H”Bridge NMOS2 B	
15	“H”Bridge PMOS1 C	“H”Bridge NMOS1 C	Monitor Driver C
16	“H”Bridge PMOS2 C	“H”Bridge NMOS2 C	
17	“H”Bridge PMOS1 D	“H”Bridge NMOS1 D	Monitor Driver D
18	“H”Bridge PMOS2 D	“H”Bridge NMOS2 D	

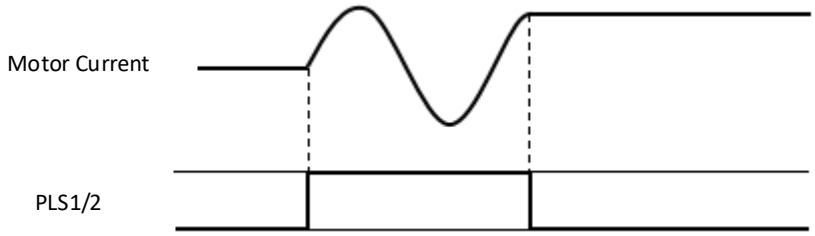
The relevant waveforms are described as follows:



PWM Circle Monitoring



Complete Pulse Output



5. LED Driver

LEDA (LED A Setting)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				LEDA											

LEDB (LED B Setting)

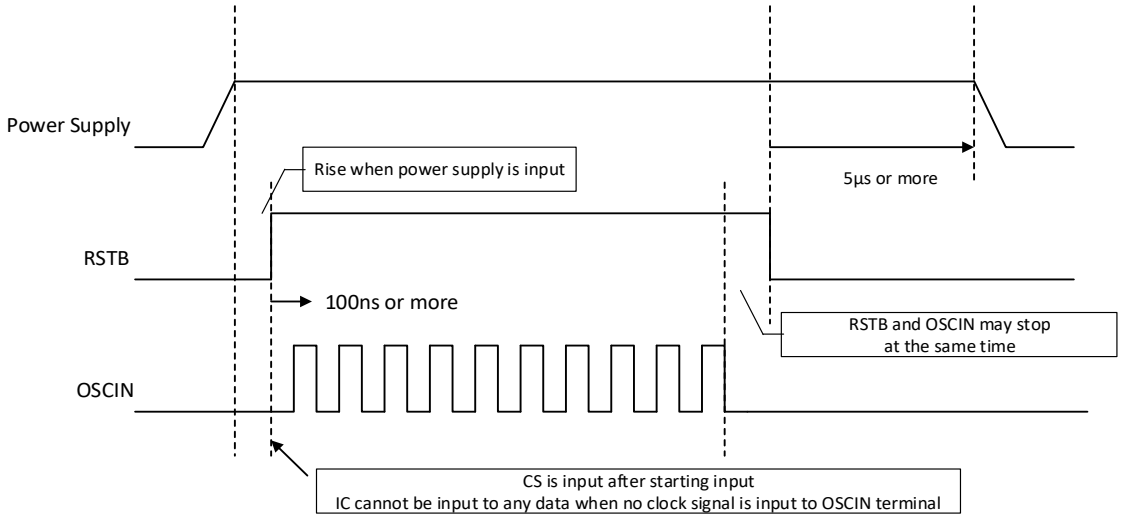
Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				LEDB											

LEDA and LEDB set output enable for LED A and LED B respectively.

Set Value	LED Output
0	Off
1	On

(1) Start and Finish Timing

The start and finish timing of power signal, RSTB and OSCIN are shown in the following figure.



(2) Input Capacitance of Input Pin

The capacitance of input pin is 10pF or less.

(3) OSCIN, VD Signal Time

Once VD signal (VD_FX or VD_IS input) is synchronized with OSCIN, the VD and OSCIN signals have no constraint on input time.

(4) Power-down Mode

When PDWNB is 0, power-down mode is set.

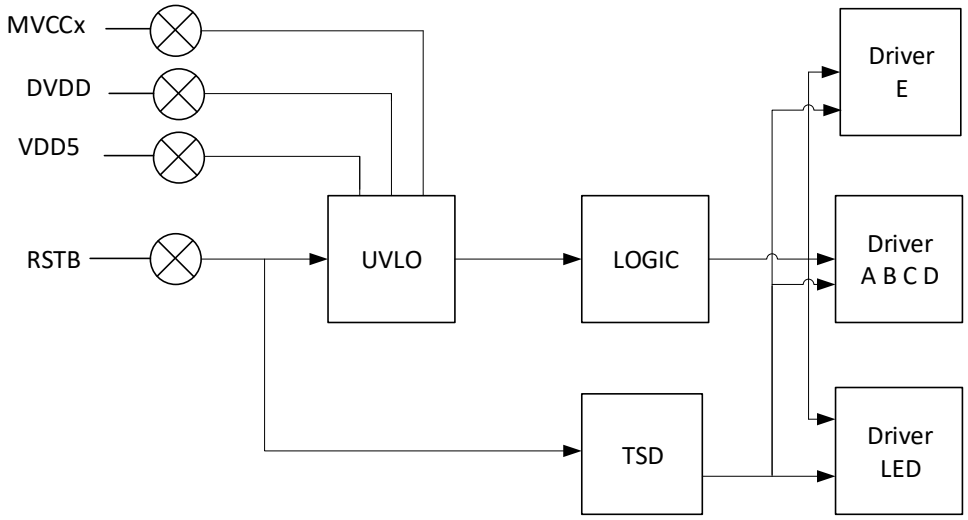
In power-down mode, the circuit of Iris analog part stops operating (motor driver is not influenced). Only when motor driver is used, power dissipation can be reduced by setting PDWNB to “0”.

The operations for related pins in power-down mode are shown as follows:

Pin	Operation
Related Input Pins	Ground
Related Output Pins	NC
CREFIN	NC
REF	NC

6. Reset/Protection Circuit

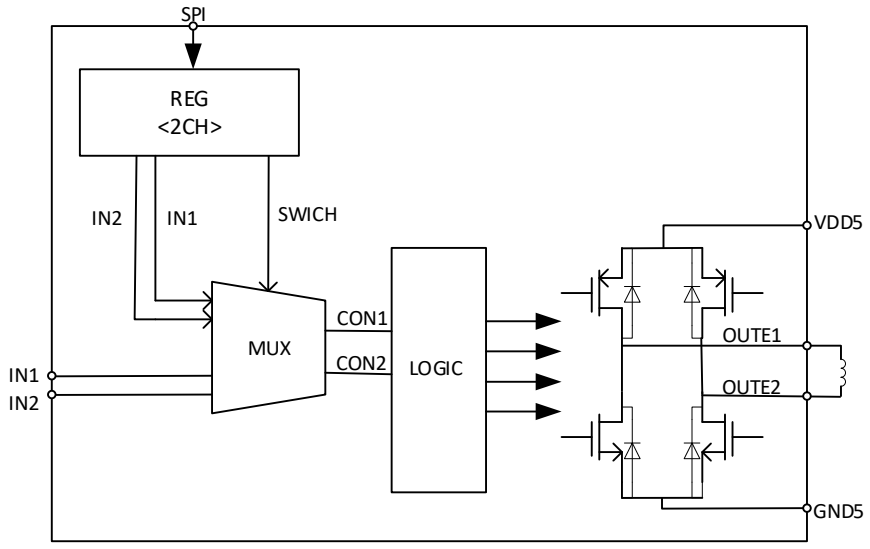
The following figure shows the relationship between RSTB, UVLO, TSD and other circuits.



The corresponding specifications are shown in the following table.

	Setting	Hall Amplifier	Focus/Zoom Output	LED
RSTB	Disable	Logic Reset->Disable	Logic Reset->Output Shutdown	
Thermal Shutdown (TSD)	×	×	Output Shutdown	
Undervoltage Lockout (UVLO)	×	Logic Reset->Disable	Logic Reset->Output Shutdown	

7. DC Driver E Circuit



DC motor (used in IR-CUT in camera) driver adopts PWM control method. There are two input control methods: direct input mode and SPI input mode. The MS41929 has a MUX switch. When MUX selects SWICH default '0' at power-up, IN1, IN2 direct input mode is selected; when SWICH register is set to '1', SPI input mode is selected.

SWICH Register: Register REG_2CH<2> bit2, Power-up Default '0''. It is set to '1' when serial input.

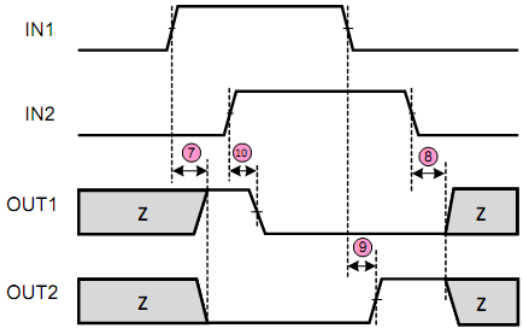
IN1 Register: Register REG_2CH<1> bit1, Power-up Default '0'.

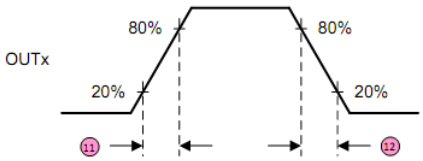
IN2 Register: Register REG_2CH<0> bit0, Power-up Default '0'.

Truth table of output is as follows:

Direct Input Mode REG_2CH<2>='0'		Register Control Mode REG_2CH<2>='1'	Output		
IN1	IN2	2CH Register Value	OUTE1	OUTE2	Motor State
0	0	0004h	Z	Z	Coast
0	1	0005h	L	H	Reverse
1	0	0006h	H	L	Forward
1	1	0007h	L	L	Brake

Transmission Delay Time for DC Motor in Direct Mode



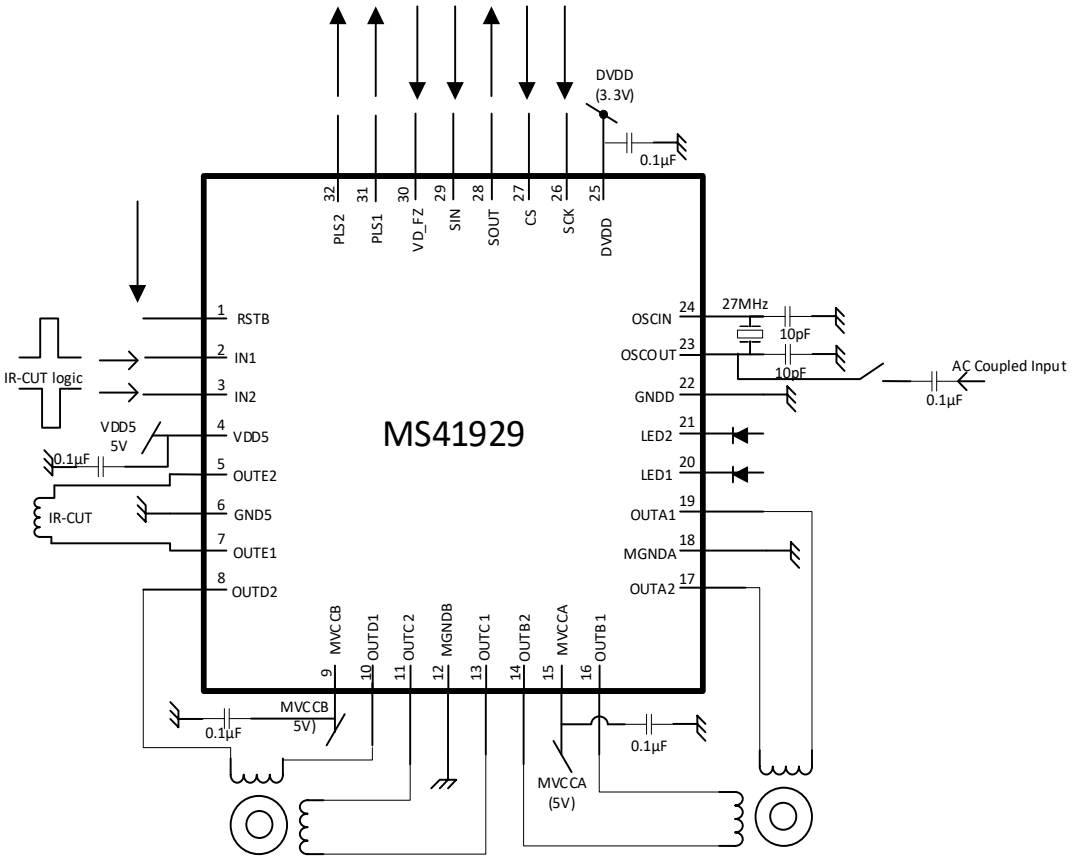


t7, t8, t9 and t10 transmission delay are all less than 300ns in direct mode, details see P8.

Delay Time of DC Motor in SPI Mode

22 data and 3 control bits are written every writing in SPI mode. The transmission delay is about t_{SCK}×25 from writing register 2CH to actual work of control time. If the serial clock of writing data is 0.5MHz, the digital delay time is 25×1/0.5M=50μs. And the maximum output frequency of H-bridge is 10kHz.

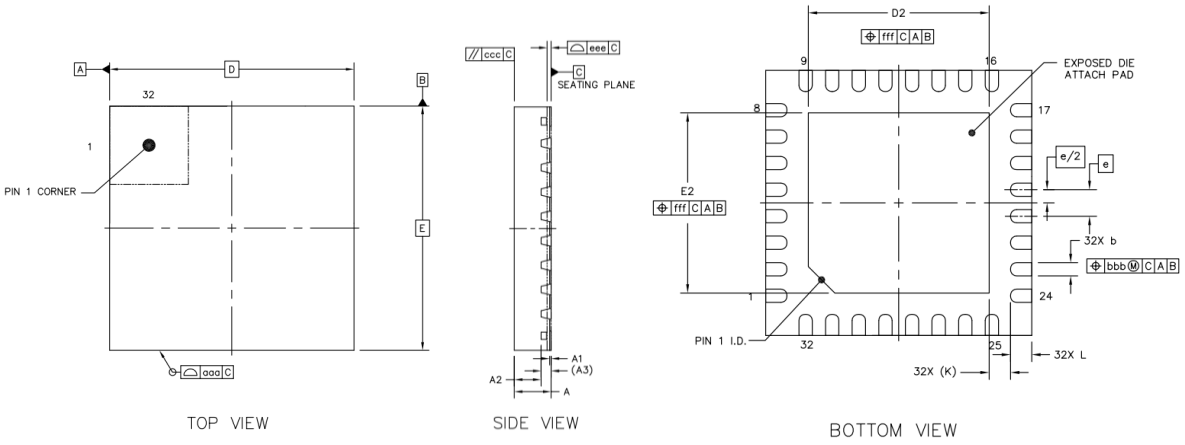
TYPICAL APPLICATION DIAGRAM



Note: In application, the Pin23, 24 are connected with 27MHz passive crystal oscillator. Pin23 can also externally connected with 27MHz clock input. It is noted that the amplitude of DC coupled input clock needs to exceed 2.4V. The amplitude of input clock needs to exceed 1V when 0.1μF capacitor is AC coupled.

PACKAGE OUTLINE DIMENSIONS

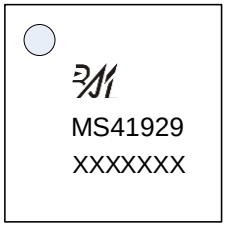
QFN32



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203REF		
b	0.2	0.25	0.3
D	5BSC		
E	5BSC		
e	0.5BSC		
D2	3.3	3.4	3.5
E2	3.3	3.4	3.5
L	0.3	0.4	0.5
K	0.4REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS41929

Product Code： XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS41929	QFN32	4000	1	4000	8	32000

STATEMENT

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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