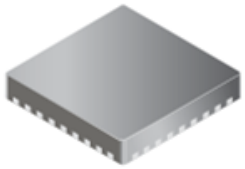
# Dual-Channel, Low Noise, 256 Microstepping, 12V Motor Driver

## PRODUCT DESCRIPTION

The MS41969 is dual-channel, 12V stepper motor driver. Ultra-low noise microstepping could be realized by voltage driving method with current microstepping and torque ripple correction technology.

The MS41969 has a built-in DC motor driver.

The MS41969 also has oscillator magnification module internally and can use passive oscillator.



**QFN36**

## FEATURES

- Voltage Driving Method, 256 Microstepping (Dual-channel)
- Maximum Driving Current ±1.2A for Each H-Bridge
- 4-Wire SPI Communication
- Built-in DC Motor Drive, Maximum Driving Current ±0.5A
- Passive Oscillator
- QFN36 Package (Back Thermal Pad)

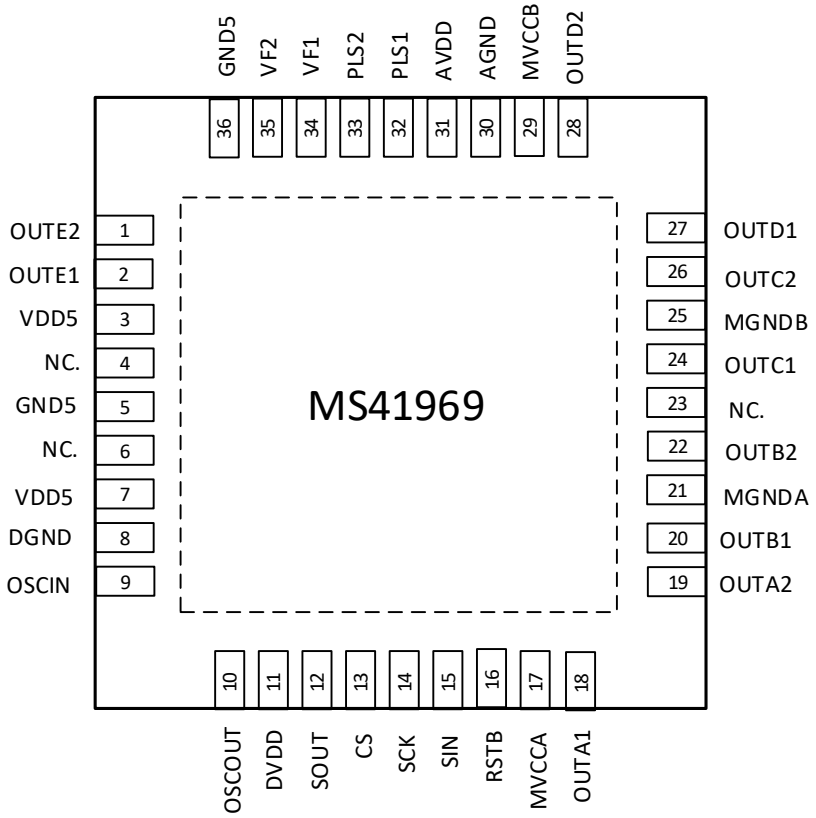
## APPLICATIONS

- Robot, Precision Industry Device
- Camera
- Monitoring Camera

## PRODUCT SPECIFICATION

| Part Number | Package | Marking |
|---|---|---|
| MS41969 | QFN36 | MS41969 |

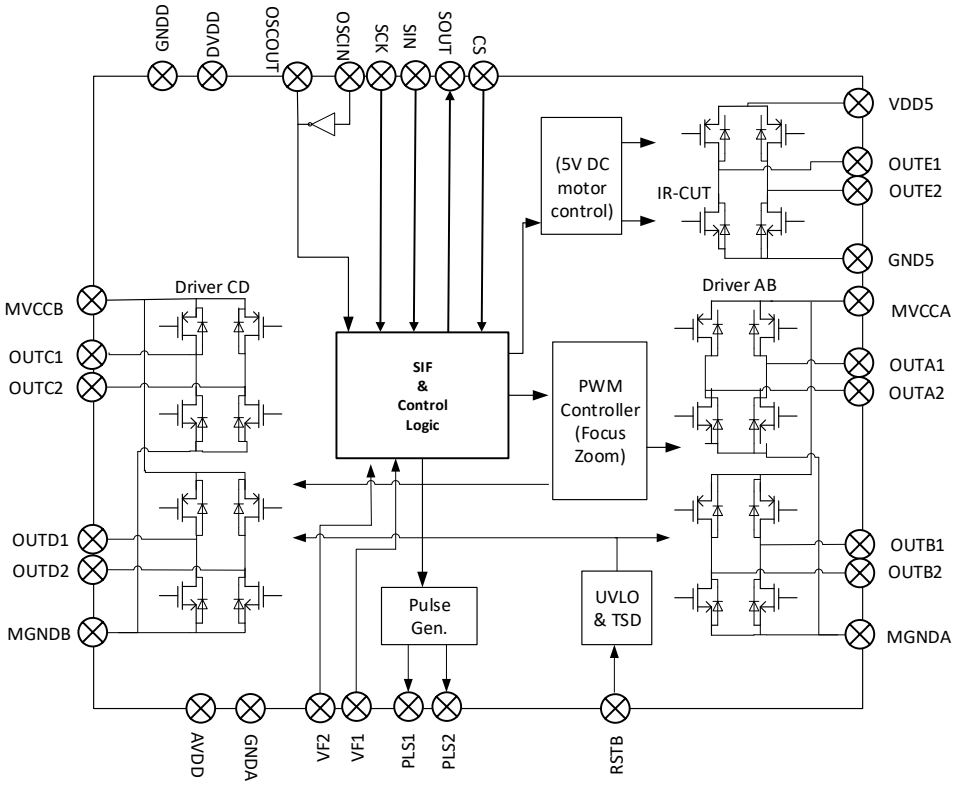
## PIN CONFIGURATION



## PIN DESCRIPTION

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | OUTE2 | O | Motor Output E2 |
| 2 | OUTE1 | O | Motor Output E1 |
| 3, 7 | VDD5 | P | DC Motor Power Supply E |
| 4, 6, 23 | NC. | - | Not Connection |
| 5, 36 | GND5 | - | DC Motor Ground E |
| 8 | DGND | - | Digital Ground |
| 9 | OSCIN | I | OSCIN Oscillator Input |
| 10 | OSCOUT | O | OSCIN Oscillator Output |
| 11 | DVDD | P | 5V Digital Power Supply |
| 12 | SOUT | O | Serial Data Output |
| 13 | CS | I | Chip Select Input |
| 14 | SCK | I | Serial Clock Input |
| 15 | SIN | I | Serial Data Input |
| 16 | RSTB | I | Reset Signal Input |
| 17 | MVCCA | P | Motor Power Supply A |
| 18 | OUTA1 | O | Motor Output A1 |
| 19 | OUTA2 | O | Motor Output A2 |
| 20 | OUTB1 | O | Motor Output B1 |
| 21 | MGNDA | - | Motor GND A |
| 22 | OUTB2 | O | Motor Output B2 |
| 24 | OUTC1 | O | Motor Output C1 |
| 25 | MGNDB | - | Motor GND B |
| 26 | OUTC2 | O | Motor Output C2 |
| 27 | OUTD1 | O | Motor Output D1 |
| 28 | OUTD2 | O | Motor Output D2 |
| 29 | MVCCB | P | Motor Power Supply B |
| 30 | AGND | - | Analog Ground |
| 31 | AVDD | P | 3.3V Analog Power Supply, Logic Output Power Supply |
| 32 | PLS1 | O | Motor Monitor Signal, Pulse 1 Output |
| 33 | PLS2 | O | Motor Monitor Signal, Pulse 2 Output |
| 34 | VF1 | I | Motor AB, Synchronous Signal Input |
| 35 | VF2 | I | Motor CD, Synchronous Signal Input |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

**Absolute Ratings**

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Power Supply, Analog and Control Part [1] | AVDD<br>DVDD | -0.3 ~ +6.0 | V |
| Load Power Supply 1 [1] | VDD5 | -0.3 ~ +6.0 | V |
| Load Power Supply 2 | MVCCx | 0 ~ 18 | V |
| Power Dissipation [2] | PD | 141.1 | mW |
| Operating Temperature [3] | Topr | -40 ~ +85 | °C |
| Storage Temperature [3] | Tstg | -55 ~ +125 | °C |
| Stepper Motor, H Bridge Drive Current | $I_{M1(CD)}$ | ±1.2 | A/ch |
| Instantaneous H Bridge Drive Current | $I_{M(pluse)}$ | ±1.8 | A/ch |
| Input Voltage, Digital Part [4] | Vin | -0.3 ~ (DVDD + 0.3) | V |
| ESD | HBM | ±4k | V |

Note:

1. Absolute maximum ratings are used in the range of power dissipation.

2. Power dissipation refers to the value of encapsulated monomer at Ta=85°C.

In practice, it is expected to refer to the technical data and PD-Ta characteristic diagram on the basis of power supply, pressure, load, ambient temperature conditions, and then carry out the heat dissipation design which does not exceed the power dissipation value.

3. Except power dissipation, ambient temperature and storage temperature parameters, all parameters are at Ta=25°C.

4. (DVDD+0.3) and (AVDD+0.3) voltage shall not exceed 6.0V.

**Operating Power Supply**

| Parameter | Symbol | Range | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Power Supply | AVDD | 3 | 3.3 | 3.6 | V |
| | DVDD | 3 | 5 | 5.5 | |
| | VDD5 | 3 | 5 | 5.5 | |
| | MVCCx | 3 | 12 | 15 | |

Note: Each power is needed to be supplied when in use, otherwise undervoltage is triggered and chip would stop operation. In general, DVDD is 5V. If it is 3.3V, the maximum frequency of OSC system clock is 20MHz

**Terminal Tolerance Current and Voltage Ranges**

The parameters cannot exceed the absolute maximum ratings in any conditions.

Rated voltage value refers to each terminal voltage with respect to GND . GND is the voltage of DGND, AGND, MGNDA, MGNDB, GND5. GND=DGND=MGNDA=MGNDB=GND5=AGND.

3.3V power is the voltage of AVDD.

5V logic power is the voltage of DVDD.

5V load power is the voltage of VDD5.

Outside input voltage and current are strictly prohibited except the described terminals below.

For the current, "+" means the current flowing to IC, and "-" means the current flowing out from IC.

| Pin | Name | Range | Unit |
|---|---|---|---|
| 9 | OSCIN | -0.3 ~ (DVDD + 0.3) | V |
| 10 | OSCOUT | -0.3 ~ (DVDD + 0.3) | V |
| 13 | CS | -0.3 ~ (DVDD + 0.3) | V |
| 14 | SCK | -0.3 ~ (DVDD + 0.3) | V |
| 15 | SIN | -0.3 ~ (DVDD + 0.3) | V |
| 34 | VF1 | -0.3 ~ (DVDD + 0.3) | V |
| 35 | VF2 | -0.3 ~ (DVDD + 0.3) | V |
| 16 | RSTB | -0.3 ~ (DVDD + 0.3) | V |
| 28 | OUTD2 | ±1.2 | A |
| 27 | OUTD1 | ±1.2 | A |
| 26 | OUTC2 | ±1.2 | A |
| 24 | OUTC1 | ±1.2 | A |
| 22 | OUTB2 | ±1.2 | A |
| 20 | OUTB1 | ±1.2 | A |
| 19 | OUTA2 | ±1.2 | A |
| 18 | OUTA1 | ±1.2 | A |
| 2 | OUTE1 | ±0.5 | A |
| 1 | OUTE2 | ±0.5 | A |

Note: (DVDD+0.3) voltage should not exceed 6.0V.

## ELECTRICAL CHARACTERISTICS

MVCCx = 12V, VDD5 =5V, DVDD = 5V, AVDD = 3.3V. Unless other noted, Ta = 25°C ± 2°C.

**Current Consumption**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Standby Power Supply Current | Iccstandby | RSTB = low output open-circuit<br>27MHz input<br>Total currents of all powers | | 1.1 | 2 | mA |
| Operating Power Supply Current | ICC1 | RSTB = high<br>No load<br>No 27MHz input<br>Total currents of all powers | | 2.6 | 4 | mA |
| | ICC2 | RSTB = high<br>No load<br>27MHz input<br>Total currents of all powers | | 14 | 20 | mA |

**Digital Input and Output**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High-level Input Voltage | Vin(H) | RSTB | 0.54×DVDD | | DVDD+0.3 | V |
| Low-level Input Voltage | Vin(L) | RSTB | -0.3 | | 0.2×DVDD | V |
| SOUT High-level Output | Vout(H):SDATA | [SOUT] 1mA current source | AVDD-0.5 | | | V |
| SOUT Low-level Output | Vout(L):SDATA | [SOUT] 1mA current sink | | | 0.5 | V |
| PLS1~2 High-level Output | Vout(H):MUX | | 0.9×AVDD | | | V |
| PLS1~2 Low-level Output | Vout(L):MUX | | | | 0.1×AVDD | V |
| Input Pull-down Impedance | Rpullret | RSTB | 50 | 100 | 200 | kΩ |

**Stepper Motor Drive**

Focal length and zoom control in camera

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| H Bridge ON Impedance | RonFZ | IM = 500mA (HS+LS) | 0.40 | 0.62 | 0.82 | Ω |
| H Bridge Leakage Current | IleakFZ | | | | 0.8 | μA |

**DC Motor Drive (DC motor, DRIVER E, IR-CUT in camera)**

VDD5=5V, Iout=500mA, Ta=25°C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output ON Impedance | Roncut | IE=500mA<br>Total resistance of high and low side FETs | 1.0 | 1.25 | 1.5 | Ω |
| Output Leakage Current | IleakE | | | | 0.8 | μA |
| Delay from SPI Input to DC Output | t13 | SPI input mode, RL=20Ω | | 25×TSCK | | s |

**Digital Input**

DVDD=5 V

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High-level Input Threshold Voltage | Vin(H) | SCK,SIN,CS,VDx | | 2.3 | | V |
| Low-level Input Threshold Voltage | Vin(L) | SCK,SIN,CS,VDx | | 2.0 | | V |
| RSTB Signal Pulse | trst | | 100 | | | μs |
| Input Maximum Hysteresis Error | Vhysin | SCK,SIN,CS,VDx | | 0.34 | | V |
| OSCIN DC High-level Input Voltage | OSCdcH | External CLK or active OSC | 4.1 | | DVDD | V |
| OSCIN DC Low-level Input Voltage | OSCdcL | External CLK or active OSC | 0 | | 1 | V |
| OSCIN AC Input | OSCdc | DC operation point | | DVDD/2 | | V |
| OSCIN AC Input Vpp | OSCacvpp | External CLK or active OSC, AC-coupled 0.1μF capacitor | 2 | | DVDD | V |
| Active OSC Power Supply | OSCvp | Active OSC | | DVDD | | V |
| Synchronization Signal Width | VFxw | | 80 | | | μs |
| CS Signal Wait Signal 1 | t(VD-CS) | | 400 | | | ns |
| CS Signal Wait Signal 2 | t(CS-DT1) | | 5 | | | μs |

**Thermal Shutdown**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Temperature of Thermal Shutdown | Ttsd | | | 145 | | °C |
| Maximum Hysteresis Error of Thermal Shutdown | ΔTtsd | | | 35 | | °C |

**Power Supply Monitor Circuit**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DVDD Reset | Vrston | | | 2.48 | | V |
| DVDD Reset Maximum Hysteresis Error | Vrsthys | | | 0.2 | | V |
| MVCCx Reset | VrstFZon | | | 2.42 | | V |
| MVCCx Reset Maximum Hysteresis Error | VrstFZhys | | | 0.21 | | V |

## FUNCTION DESCRIPTION

### 1. Serial Interface

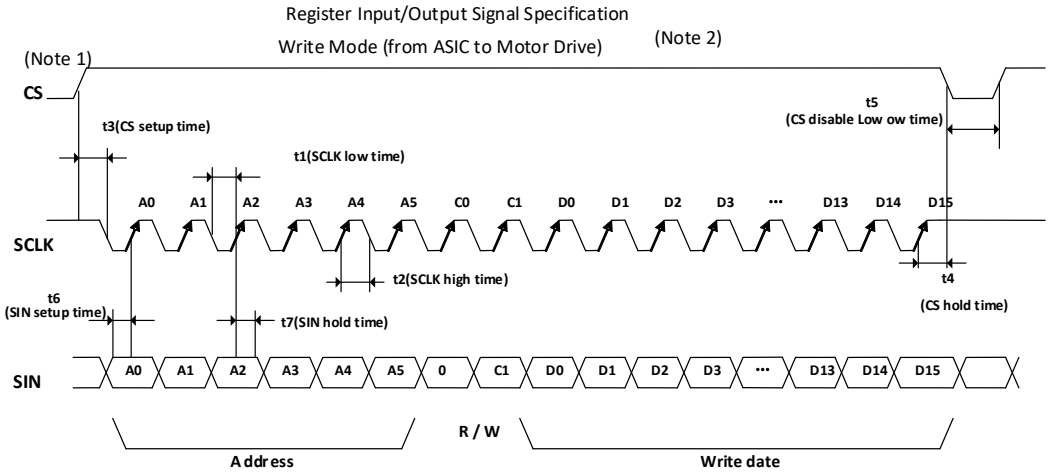



Figure 1. Data Write

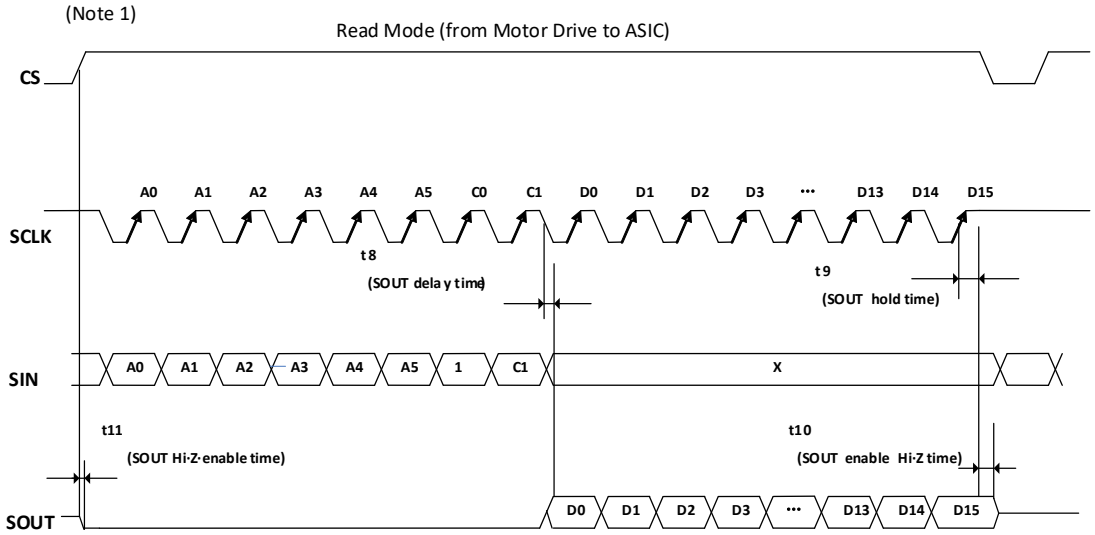



Figure 2. Data Read

Note: 1. In read/write mode, CS starts from 0 by default every cycle.

2. When in write mode, the system clock must be input from OSCIN terminal.

**Electrical Parameters (Design Reference)**

VDD5=MVCCx=5V, DVDD=5V, AVDD=3.3V

Unless other noted,Ta = 25°C ±2°C. The characteristics are only design values and only for references.

**1.1 Serial Port Input**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Serial clock | Sclock | | 1 | | 5 | MHz |
| SCK low time | t1 | | 100 | | | ns |
| SCK high time | t2 | | 100 | | | ns |
| CS setup time | t3 | | 60 | | | ns |
| CS hold time | t4 | | 60 | | | ns |
| CS disable high time | t5 | | 100 | | | ns |
| SIN setup time | t6 | | 50 | | | ns |
| SIN hold time | t7 | | 50 | | | ns |
| SOUT delay time | t8 | | | | 60 | ns |
| SOUT hold time | t9 | | 60 | | | ns |
| SOUT Enable-Hi-Z time | t10 | | | | 60 | ns |
| SOUT Hi-Z-Enable time | t11 | | | | 60 | ns |
| Sout C load | tsc | | | | 40 | pF |

1. The data conversion starts on the rising edge of CS and stops on the falling edge of CS.

2. The data stream unit of a conversion is 24 bits.

3. When the address and data are input from the SIN pin, the clock signal SCK remains consistent under the condition of CS=1.

4. The data is driven into IC on the rising edge of SCK signal. At the same time, when the data is output, it is read out from SOUT pin (the data is output on the rising edge of SCK).

5. SOUT outputs a high impedance state when CS=0, and when CS = 1, outputs "0" unless there is a data read.

6. The control of entire serial interface is reset when CS=0.

**1.2 Data Format**

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A0 | A1 | A2 | A3 | A4 | A5 | C0 | C1 |

| 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|
| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |

| 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |
|---|---|---|---|---|---|---|---|
| D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 |

C0: Register Read and Write Options: 0: Write Mode, 1: Read Mode

C1: No Use

A5~A0: Register Address

D15~D0: Data Written to Register

### 1.3 Register Map

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0BH | Reserved | | | | | | MODE SEL_FZ | Reserved | | | | Reserved | | | | |
| 20H | | PWMRES[1:0] | | PWMMODE[4:0] | | | | | DT1[7:0] | | | | | | | |
| 21H | | | | | | | | | TEST EN2 | | | FZTEST[4:0] | | | | |
| 22H | | | PHMODAB[5:0] | | | | | | DT2A[7:0] | | | | | | | |
| 23H | PPWB[7:0] | | | | | | | | PPWA[7:0] | | | | | | | |
| 24H | | | MICROAB [1:0] | | LEDB | ENDIS AB | BRAKE AB | CCWCW AB | PSUMAB[7:0] | | | | | | | |
| 25H | INTCTAB[15:0] | | | | | | | | | | | | | | | |
| 27H | | | PHMODCD[5:0] | | | | | | DT2B[7:0] | | | | | | | |
| 28H | PPWD[7:0] | | | | | | | | PPWC[7:0] | | | | | | | |
| 29H | | | MICROCD [1:0] | | LEDA | ENDIS CD | BRAKE CD | CCWCW CD | PSUMCD[7:0] | | | | | | | |
| 2AH | INTCTCD[15:0] | | | | | | | | | | | | | | | |
| 2CH | | | | | | | | | | | | | | IN SWICH | IN1 | IN2 |

### 1.4 Register List

| Address | Register Name/Bit Width | Description | Page |
|---|---|---|---|
| 0Bh | MODESEL_FZ | VFx Polarity Select | 15 |
| 20h | DT1[7:0] | Start Point Wait Time | 19 |
| | PWMMODE[4:0] | Microstep Output PWM Frequency | 20 |
| | PWMRES[1:0] | Microstep Output PWM Resolution | 20 |
| 21h | FZTEST[4:0] | PLS1/2Output Signal Select | 26 |
| | TESTEN2 | TEST Mode Enable 2 | 26 |
| 22h | DT2A[7:0] | Start Point Excitation Wait Time (α Stepper Motor) | 19 |
| | PHMODAB[5:0] | Motor Phase Correction (α Stepper Motor) | 21 |

| Address | Register Name/Bit Width | Description | Page |
|---|---|---|---|
| 23h | PPWA[7:0] | Peak Pulse Width of A Channel | 21 |
| | PPWB[7:0] | Peak Pulse Width of B Channel | 21 |
| 24h | PSUMAB[7:0] | Step Number of Stepper Motor (α Stepper Motor) | 22 |
| | CCWCWAB | Motor Rotation Direction (α Stepper Motor) | 23 |
| | BRAKEAB | Motor Brake State (α Stepper Motor) | 23 |
| | ENDISAB | Motor Enable/Disable (α Stepper Motor) | 24 |
| | MICROAB[1:0] | Sine Wave Microstep (α Stepper Motor) | 24 |
| 25h | INTCTAB[15:0] | Microstep Cycle (α Stepper Motor) | 25 |
| 27h | DT2B[7:0] | Start Point Excitation Wait Time (β Stepper Motor) | 19 |
| | PHMODCD[5:0] | Motor Phase Correction (β Stepper Motor) | 21 |
| 28h | PPWC[7:0] | Peak Pulse Width of C Channel | 21 |
| | PPWD[7:0] | Peak Pulse Width of D Channel | 21 |
| 29h | PSUMCD[7:0] | Step Number of Stepper Motor (β Stepper Motor) | 22 |
| | CCWCWCD | Motor Rotation Direction (β Stepper Motor) | 23 |
| | BRAKECD | Motor Brake State (β Stepper Motor) | 23 |
| | ENDISCD | Motor Enable/Disable (β Stepper Motor) | 24 |
| | MICROCD[1:0] | Sine Wave Microstep (β Stepper Motor) | 24 |
| 2Ah | INTCTCD[15:0] | Microstep Cycle (α Stepper Motor) | 25 |
| 2Ch | INSWICH | DC Motor Enable | |
| | IN1 | DC Motor Input Control 1 | |
| | IN2 | DC Motor Input Control 2 | |

All register bit data is initialized at RSTB = 0.

### 1.5 Register Setup Time

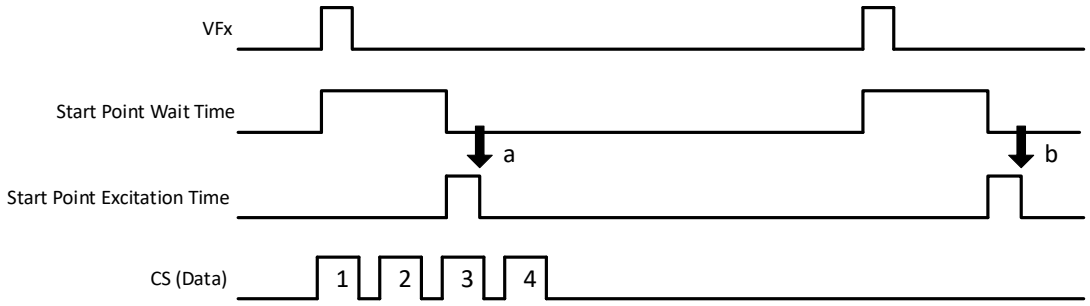
| Address | Name | Setup Time |
|---|---|---|
| 0Bh | MODESEL_FZ | CS |
| 20h | DT1[7:0] | VFx |
| | PWMMODE[4:0] | DT1 |
| | PWMRES[1:0] | DT1 |
| 21h | FZTEST[4:0] | CS |
| | TESTEN2 | CS |

| Address | Name | Setup Time |
|---|---|---|
| 22h | DT2A[7:0] | DT1 |
| | PHMODAB[5:0] | DT2A |
| 23h | PPWA[7:0] | DT1 |
| | PPWB[7:0] | DT1 |
| 24h | PSUMAB[7:0] | DT2A |
| | CCWCWAB | DT2A |
| | BRAKEAB | DT2A |
| | ENDISAB | DT1 or DT2A* |
| | LEDB | CS |
| | MICROAB[1:0] | DT2A |
| 25h | INTCTAB[15:0] | DT2A |
| 27h | DT2B[7:0] | DT1 |
| | PHMODCD[5:0] | DT2B |
| 28h | PPWC[7:0] | DT1 |
| | PPWD[7:0] | DT1 |
| 29h | PSUMCD[7:0] | DT2B |
| | CCWCWCD | DT2B |
| | BRAKECD | DT2B |
| | ENDISCD | DT1 or DT2B* |
| | LEDA | CS |
| | MICROCD[1:0] | DT2B |
| 2Ah | INTCTCD[15:0] | DT2B |

* 0→1: it works on DT1 ; 1→0: it works on DT2x

In principle, the setup of registers for microsteps should be completed during the time period when the start point is delayed (see figure on page 15). Data written outside the start delay can also be stored in registers. However, if the write operation is executed after the refresh time, the written register will not be valid at the scheduled time. For example, if the updated data 1~4 is written as shown in the following figure after the start point excitation delay, data 1 and 2 are immediately updated at time a, and data 3 and 4 are updated at time b. Even if the data is written continuously, the update time interval is 1 VFx cycle.

For the above reasons, in order to update data timely, the establishment of the register data needs to be completed during the start point delay.




**2. VFx Internal Process**

In this system, the reflection time and rotation time of stepper motor are respectively based on the rising edge of VFx. The polarity of VFx is set by the following registers.

**Register Detail**

**MODESEL_FZ (VFx Polarity Select)**

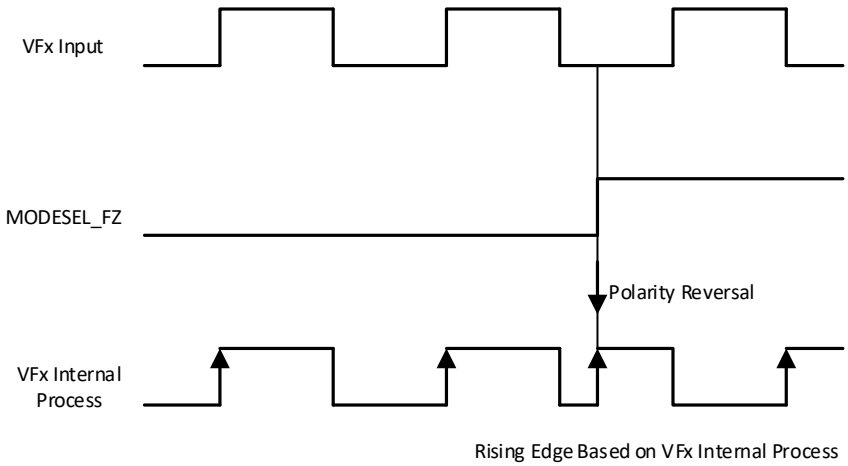
| Address | | | 0Bh | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | MODESEL_FZ | | | | | | | | | |

MODESEL_FZ sets the VFx polarity.

When set to "0", the polarity is based on the rising edge of VFx . When set to "1", the polarity is based on the falling edge of VFx .

MODESEL_FZ selects the polarity of input VFx. When MODESEL_FZ is reversed as follows, a VFx signal would be generated and the moment is independent of VFx edge.

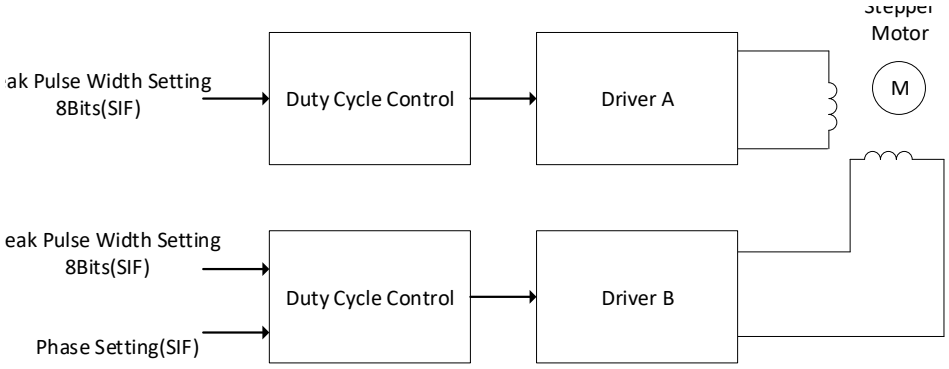
| Set Value | VFx Polarity |
|---|---|
| 0 | Non-inverting |
| 1 | Inverting |




Rising Edge Based on VFx Internal Process

## 3. Stepper Motor Microstep Drive

### 3.1 Block Diagram




The following settings can be used to perform a series of controls. The following is the description of the motor α: driver A/B. C, D perform the same algorithm as the motor α.

Main Setting Parameters:

| | |
|---|---|
| Phase correction: The phase difference between driver A and driver B is targeted on 90°, and can be adjusted from -22.5° to +21.8°. | ——> PHMODAB[5:0] |
| Amplitude Setting: Set the load current of driver A/B independently | ——>PPWA[7:0],PPWB[7:0] |
| PWM Frequency: PWM frequency setting of driver output | ——>PWMMODE[4:0],PWMRES[1:0] |
| Microstep Number: Can be set to 64,128, 256 | ——>MICROAB[1:0] |
| Step cycle: Motor Rotation Speed Setting. It is independent of microstep mode of sine wave. | ——>INTCTAB[15:0] |

### 3.2 Setup Time of Related Settings

The setup time and related time are shown below.

The setting of addresses 27h to 2Ah is the same as 22h to 25h, so the description of 27h to 2Ah is omitted.If the related registers are updated, a setting load refresh is implemented for each VFx cycle. When the same setting is executed with more than 2VFx pulses, it is not necessary to write register data on each VFx pulse.

**DT1[7:0] (Start Point Delay, Address 20h)**

Update data time Setting. It must be set after the system hardware reset (Pin RSTB: Low → High), before starting the excitation and driving motor (DT1 ends).

Since this setting is updated every time a VFx pulse comes, it is not necessary to write during the start point delay.

**PWMMODE[4:0], PWMRES[1:0] (Microstep Output PWM Frequency, Address 20h)**

Set PWM frequency of the microstep output. Need to be set to execute before starting excitation and driving motor (DT1 ends).

**DT2A[7:0] (Start Point Excitation Delay, Address 22h)**

Update data time setting. After reset (Pin RSTB: Low→High), need to be set to execute before starting excitation and driving motor (DT1 ends).

**PHMODAB[5:0] (Phase Correction, Address 22h)**

By correcting the phase difference between coils A and B, the driver produces less noise.The appropriate phase correction must be based on the rotation direction and speed. This setting must be changed with the rotation direction (CCWCWAB) or the rotation speed (INTCTAB).

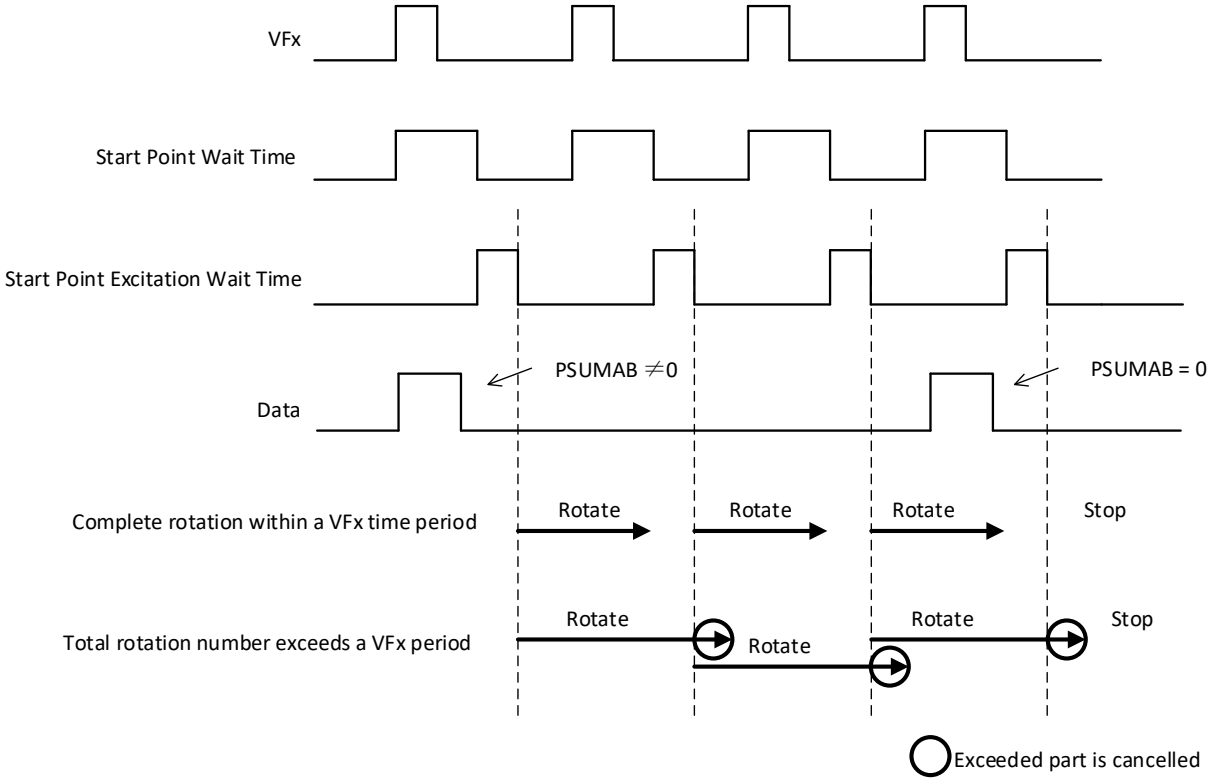
**PPWA[7:0],PPWB[7:0] (Peak Pulse Width, Address 23h)**

Set the PWM maximum duty cycle. Setting needs to be set before starting the excitation and driving motor (DT1ends).

**PSUMAB[7:0] (Step Number of Stepper Motor, Address 24h)**

The rotation number of the motor is set within 1 VFx time interval.

The number of the motor rotation is set when each VFx pulse is input. Therefore, setting the frequency to "0" can stop the motor rotation. When the total number of rotations exceeds the time of 1 VFx pulse, the exceeded part will be canceled.




**CCWCWAB(Rotation Direction, Address 24h)**

Motor rotation direction setting. Just set it before selecting the rotation direction.

**BRAKEAB (Motor Brake Setting, Address 24h)**

Set the current to 0 when braking. This setting is generally used to stop the motor immediately because it is difficult to obtain final position when this setting is performed.

**ENDISAB (Motor Operation Enable/Disable, Address 24h)**

Set the motor work enable. When set to disable, the motor pin outputs high impedance state, and should not be set to disable while the motor is rotating.

**LEDA (LED Setting, Address 24h)**

LED on/off setting. It is set on the falling edge of CS. Realize independent setting and it is regarded independent of motor driver.

**MICROAB[1:0] (Sine Wave Frequency Division, Address 24h)**

Set the frequency division number of sine wave. This setting does not change the number and speed of rotation. It is set only when the rotation speed doesn't reach the demand. After reset (Pin RSTB: Low→High), setting is effective.

**INTCTAB[15:0] (Pulse Period, Address 25h)**

Pulse period setting. The rotation speed depends on this setting.

### 3.3 How to adjust the register value when the stepper motor is driven by microstep

In order to control the stepper motor, it is required to set the number and speed of motor rotation for each VFx.The related registers are:

INTCTxx[15:0]: Set the time of each step (corresponding to the rotation speed)

PSUMxx[7:0]: Total number of rotation steps in each VFx period

When the motor is continuously driven in a continuous VFx period, the continuous rotation time needs to be set to adapt to the VFx period.

The followings are how to calculate INTCTxx[15:0] and PSUMxx[7:0] when the motor is rotating

(1) Calculate INTCTxx[15:0] (determine the motor rotation speed)

$$INTCTxx[15:0] \times 768 = OSCIN\ Frequency/Rotation\ Frequency$$

(2) PSUMxx[7:0] is calculated by INCTxx[15:0]. Don't just only look at the value of PSUMxx[7:0].

When the following equation holds, the continuous rotation time and VFx time are the same, and the motor achieves uniform rotation.

$$INTCTxx[15:0] \times PSUMxx[7:0] \times 24 = OSCIN\ Frequency/\ VFx\ Frequency$$

(3) After the setting of PSUMxx[7:0] is completed, INTCTxx[15:0] is recalculated from above formula.

For example, OSCIN Frequency= 27 MHz, VFx Frequency = 60Hz

Calculate PSUMxx[7:0] and INTCTxx[15:0] to make the motor rotate at 800pps (1-2 phase)

800pps is equal to 100Hz, so

$$INTCTxx[15:0] = 27MHz / (100Hz \times 768) = 352$$

The corresponding

$$PSUMxx[7:0] = 1/(60Hz) \times 27MHz/ (352 \times 24) = 53$$

Recalculate INTCTxx[15:0]

$$INTCTxx[15:0] = 1/(60Hz) \times 27MHz/ (53 \times 24) = 354$$

If the left side of the equation in (2) is smaller than the right side, the rotation time is smaller than the VFx period, which will cause discontinuous rotation. On the contrary, rotation beyond VFx time period will be canceled.

### 3.4 Register Detail

**DT1[7:0] (Start Point Wait Time)**

| Address | | | 20h | | | Initial Value | | | 0Ah | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | | | DT1[7:0] | | | | | | | |

DT1[7:0] sets the delay time of data writing to the system (start point wait time)

The motor can be activated precisely after the start point wait time is flipped from "1" to "0". The start point wait time is calculated from the rising edge of the synchronization video signal (VFx).

Because the start point delay time is mainly used to wait for the serial data to be written. The register value should be set to greater than "0". If it is "0", the corresponding data cannot be updated.

Refer to page 15 for the relationship between VFx and the start point wait time.

| DT1 | Start Point Wait |
|---|---|
| 0 | Prohibit |
| 1 | 303.4μs |
| 255 | 77.4ms |
| n | n×8192/27MHz |

**DT2A[7:0] (Start Point Excitation Wait Time Motor α)**

| Address | | | 22h | | | Initial Value | | | 03h | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | | | DT2A[7:0] | | | | | | | |

**DT2B[7:0] (Start Point Excitation Wait Time Motor β)**

| Address | | | 27h | | | Initial Value | | | 03h | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | | | DT2B[7:0] | | | | | | | |

DT2A[7:0] and DT2B[7:0] set the wait delay time before the motor α and the motor β start to rotate.

The motor starts to rotate after the start point excitation wait time is flipped from "1" to "0". The start point excitation wait time starts to calculate at the end of start point wait time.

This signal is a separate delay for AB.The register value should be set to greater than "0". If it is "0", the corresponding data can't be updated.

Refer to page 15 for the relationship between VFx and the start point excitation wait time.

| DT1 | Start Point Excitation Wait |
|---|---|
| 0 | Prohibit |
| 1 | 303.4μs |
| 255 | 77.4ms |
| n | n×8192/27MHz |

**PWMMODE[4:0] (Microstep Output PWM Frequency)**

| Address | | | 20h | | | Initial Value | | | 1Ch | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | PWMMODE[4:0] | | | | | | | | | | | | |

**PWMRES[1:0] (Microstep Output PWM Resolution)**

| Address | | | 20h | | | Initial Value | | | 1 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | PWMRES[1:0] | | | | | | | | | | | | | | |

PWMMODE[4:0] sets the microstep output PWM frequency by setting the frequency division of system clock OSCIN.

PWMMODE[4:0] can be set in the range of 1 to 31. The frequency of PWM wave is same when PWMMODE = 0 and PWMMODE = 1.

PWM frequency is decided by PWMRES[1:0] and PWMMODE[4:0].

The PWM frequency is calculated by the following formula

$$\text{PWM Frequency} = \text{OSCIN Frequency} \ / \ ((\text{PWMMODE} \times 2^3) \times 2^{\text{PWMRES}})$$

When OSCIN=27MHz, PWM frequency is shown in the following table (kHz) :

| PWMMODE | PWMRES | | | PWMMODE | PWMRES | | |
|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | | 0 | 1 | 2 |
| 1 | 3375.0 | 1687.5 | 843.8 | 17 | 198.5 | 99.3 | 49.6 |
| 2 | 1687.5 | 843.8 | 421.9 | 18 | 187.5 | 93.8 | 46.9 |
| 3 | 1125.0 | 526.5 | 281.3 | 19 | 177.6 | 88.8 | 44.4 |
| 4 | 843.8 | 421.9 | 210.9 | 20 | 168.8 | 84.4 | 42.2 |
| 5 | 675.0 | 337.5 | 168.8 | 21 | 160.7 | 80.4 | 40.2 |
| 6 | 526.5 | 281.3 | 140.6 | 22 | 153.4 | 76.7 | 38.4 |
| 7 | 482.1 | 241.1 | 120.5 | 23 | 146.7 | 73.4 | 36.7 |
| 8 | 421.9 | 210.9 | 105.5 | 24 | 140.6 | 70.3 | 35.2 |
| 9 | 375.0 | 187.5 | 93.8 | 25 | 135.0 | 67.5 | 33.8 |
| 10 | 337.5 | 168.8 | 84.4 | 26 | 129.8 | 64.9 | 32.5 |
| 11 | 306.8 | 153.4 | 76.7 | 27 | 125.0 | 62.5 | 31.3 |
| 12 | 281.3 | 140.6 | 70.3 | 28 | 120.5 | 60.3 | 30.1 |
| 13 | 259.6 | 129.8 | 64.9 | 29 | 116.4 | 58.2 | 29.1 |
| 14 | 241.1 | 120.5 | 60.3 | 30 | 112.5 | 56.3 | 28.1 |
| 15 | 225.0 | 112.5 | 56.3 | 31 | 108.9 | 54.4 | 27.2 |
| 16 | 210.9 | 105.5 | 52.7 | | | | |

**PHMODAB[5:0] (Motor α Phase Correction)**

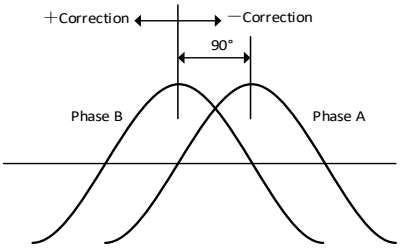
| Address | | | 22h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | PHMODAB[5:0] | | | | | | | | | | | | | |

**PHMODCD[5:0] (Motor β Phase Correction)**

| Address | | | 27h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | PHMODCD[5:0] | | | | | | | | | | | | | |

The current phase difference in motor α and β are set by PHMODAB[5:0] and PHMODCD[5:0] .The default value is 90° and set 1 unit to 0.7°. Meanwhile, the data can be subject to positive and negative deviation.

| PHMODAB | Phase Correction Number |
|---|---|
| 000000 | ±0° |
| 000001 | +0.7° |
| 011111 | +21.80° |
| 100000 | -22.50° |
| 111111 | -0.7° |
| Damping Unit | 360°/512 = 0.70° |




The phase difference between the stepper motor coils is generally 90°. However, due to different motors or process deviations, the phase difference will also be shifted by 90°. Therefore, even if the phase difference of the drive waveform current is 90°, but the motor itself is not 90° difference, it will produce torque ripple, and the noise still exists.

The main purpose of this setting is to reduce the torque ripple caused by motor changes.

**PPWA[7:0] (Peak Pulse Width for Driver A)**

**PPWB[7:0] (Peak Pulse Width for Driver B)**

| Address | | | 23h | | | Initial Value | | | 0,0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PPWB[7:0] | | | | | | | | PPWA[7:0] | | | | | | | |

**PPWC[7:0] (Peak Pulse Width for Driver C)**

**PPWD[7:0] (Peak Pulse Width for Driver D)**

| Address | | | 28h | | | Initial Value | | | 0,0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PPWD[7:0] | | | | | | | | PPWC[7:0] | | | | | | | |

The maximum duty cycle of the PWM wave is set by PPWA[7:0] to PPWD[7:0], which determines the position of the peak output current from driver A to D.

The maximum duty cycle is calculated by the following equation:

*Driver X Maximum Duty Cycle = PPWx/ (PWMMODE × 8)*

When PPWx = 0, coil current is 0.

For example, when PPWA[7:0]=200, PWMMODE[4:0]=28, maximum duty cycle is:

200 / (28 × 8) = 0.89

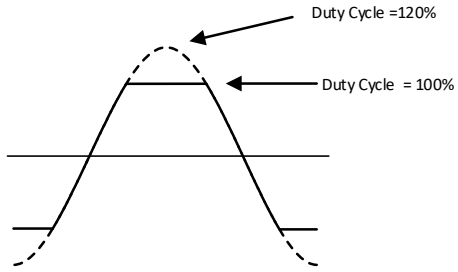
Depending on the values of PWMMODE and PPWx, the maximum duty cycle may exceed 100%.

Of course, the duty cycle cannot exceed 100% in fact and the peak point of sine wave will be truncated as shown in the following figure.

For example, when PWMMODE = 10, PPWx = 96,

Maximum Duty Cycle = 90/(10 × 8) = 120%

The waveform of the target current is shown as follows:




**PSUMAB[7:0] (Step Number of Motor α)**

| Address | | | 24h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | | | PSUMAB[7:0] | | | | | | | |

**PSUMCD[7:0] (Step Number of Motor β)**

| Address | | | 29h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | | | PSUMCD[7:0] | | | | | | | |

PSUMAB[7:0] and PSUMCD[7:0] respectively set the total step number of the motor α and motor β.

If want to stop the motor, set PSUMxx[7:0]=0.

| Register Value | Total Step Number | | |
|---|---|---|---|
| | 64 Microstep | 128 Microstep | 256 Microstep |
| 0 | 0 | 0 | 0 |
| 1 | 2 | 4 | 8 |
| 255 | 510 | 1020 | 2040 |
| n | 2n | 4n | 8n |

As long as the maximum duty cycle of PWM wave is not set as "0", when PSUMxx[7:0]=0, the motor can keep in the release state.

An example to know the meaning of setting :

When PSUMAB[7:0]=8 is set, run 2x8=16 steps in 64 microstep mode, i.e. 16/64=1/4 sine cycle. Similarly, in 128 and 256 microstep modes, it is also a quarter of the period of sine wave.

**CCWCWAB (Rotation Direction of Motor α)**

| Address | | | 24h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | | CCWCWAB | | | | | | | | |

**CCWCWCD (Rotation Direction of Motor β)**

| Address | | | 29h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | | CCWCWCD | | | | | | | | |

CCWCWAB and CCWCWCD respectively set the rotation direction of the motor α and motor β.

Direction Definition:

| Set Value | Motor Rotation Direction |
|---|---|
| 0 | Forward |
| 1 | Reverse |

**BRAKEAB (Brake State of Motor α)**

| Address | | | 24h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | BRAKEAB | | | | | | | | | |

**BRAKECD (Brake State of Motor β)**

| Address | | | 29h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | BRAKECD | | | | | | | | | |

BRAKEAB and BRAKECD set the brake mode of the motor α and β respectively.

| Set Value | Motor Brake |
|---|---|
| 0 | Normal State |
| 1 | Brake State |

In brake state, the two upper-side PMOS FETs of H bridge are all turned on. The brake mode cannot be used in normal operation and can only be used during emergency shutdown.

**ENDISAB (Motor α Enable/Disable)**

| Address | | | 24h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | ENDISAB | | | | | | | | | | |

**ENDISCD (Motor β Enable/Disable)**

| Address | | | 29h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | ENDISCD | | | | | | | | | | |

ENDISAB and ENDISCD respectively set the output control of the motor α and motor β.

When ENDISxx = 0, motor outputs high impedance state. However, internal excitation position counter still keeps counting at ENDISxx=0. Therefore, when you want to stop the motor in normal state, set PSUMxx[7:0] = 0 instead of ENDISxx = 0.

| Set Value | Motor Output State |
|---|---|
| 0 | Output Off (High-impedance State) |
| 1 | Output On |

**MICROAB[1:0] (Sine Wave Frequency Division of Motor α)**

| Address | | | 24h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | MICROAB[1:0] | | | | | | | | | | | | | |

**MICROCD[1:0] (Sine Wave Frequency Division of Motor β)**

| Address | | | 29h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | MICROCD[1:0] | | | | | | | | | | | | | |

MICROAB and MICROCD set the frequency division of sine wave for motor α and motor β respectively.

The 64 division waveform is shown on page 25.

| MICROAB | Frequency Division |
|---|---|
| 00 | 256 |
| 01 | 256 |
| 10 | 128 |
| 11 | 64 |

**INTCTAB[15:0] (Step Cycle of Motor α)**

| Address | | | 25h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| INTCTAB[15:0] | | | | | | | | | | | | | | | |

**INTCTCD[15:0] (Step Cycle of Motor β)**

| Address | | | 2Ah | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| INTCTCD[15:0] | | | | | | | | | | | | | | | |

INTCTAB[15:0] and INTCTCD[15:0] respectively set a microstep cycle of the motor α and motor β .

| Register Value | Total Step Number | | |
|---|---|---|---|
| | 64 Microstep | 128 Microstep | 256 Microstep |
| 0 | 0 | 0 | 0 |
| 1 | 444ns | 222ns | 111ns |
| Max | 29.1ms | 14.6ms | 7.3ms |
| n | 12n/27MHz | 6n/27MHz | 3n/27MHz |

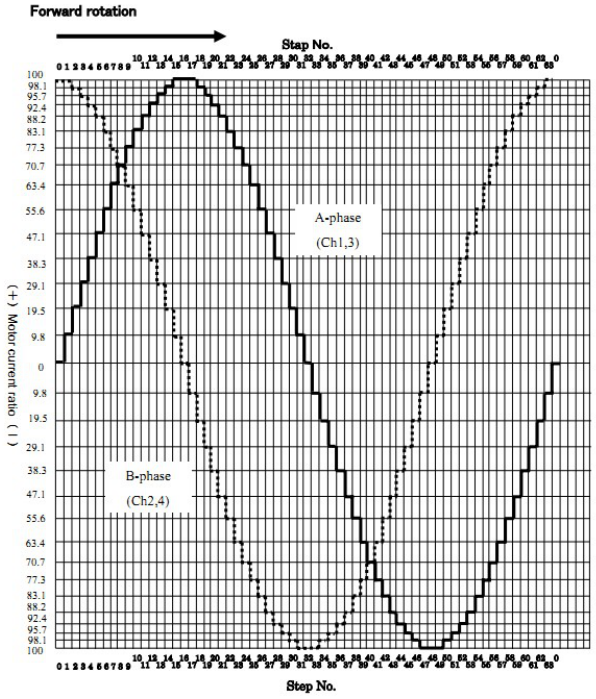
When INTCTAB[15:0]=0, as long as PWM maximum duty cycle is not 0, the motor will remain in release state .

Examples: When INTCTAB[15:0]=400, step cycle in 64 microstep:

$$12\times400/27MHz=0.178ms$$

Therefore, the period of each sine wave is 0.178x64=11.4ms (87.9Hz). Similarly, in 128 microstep or 256 microstep, it is also 11.4ms.

**Stepper Motor Drive (64 Microstep Current Curve)**



**4. Test Signal**

**FZTEST[4:0] (Test Signal Output Setting of Motor A,B)**

| Address | | | 21h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | | | | | | FZTEST[4:0] | | | | |

**TESTEN2 (Test Setting 2)**

| Address | | | 21h | | | Initial Value | | | 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | | | | | | | | TESTEN2 | | | | | | | |

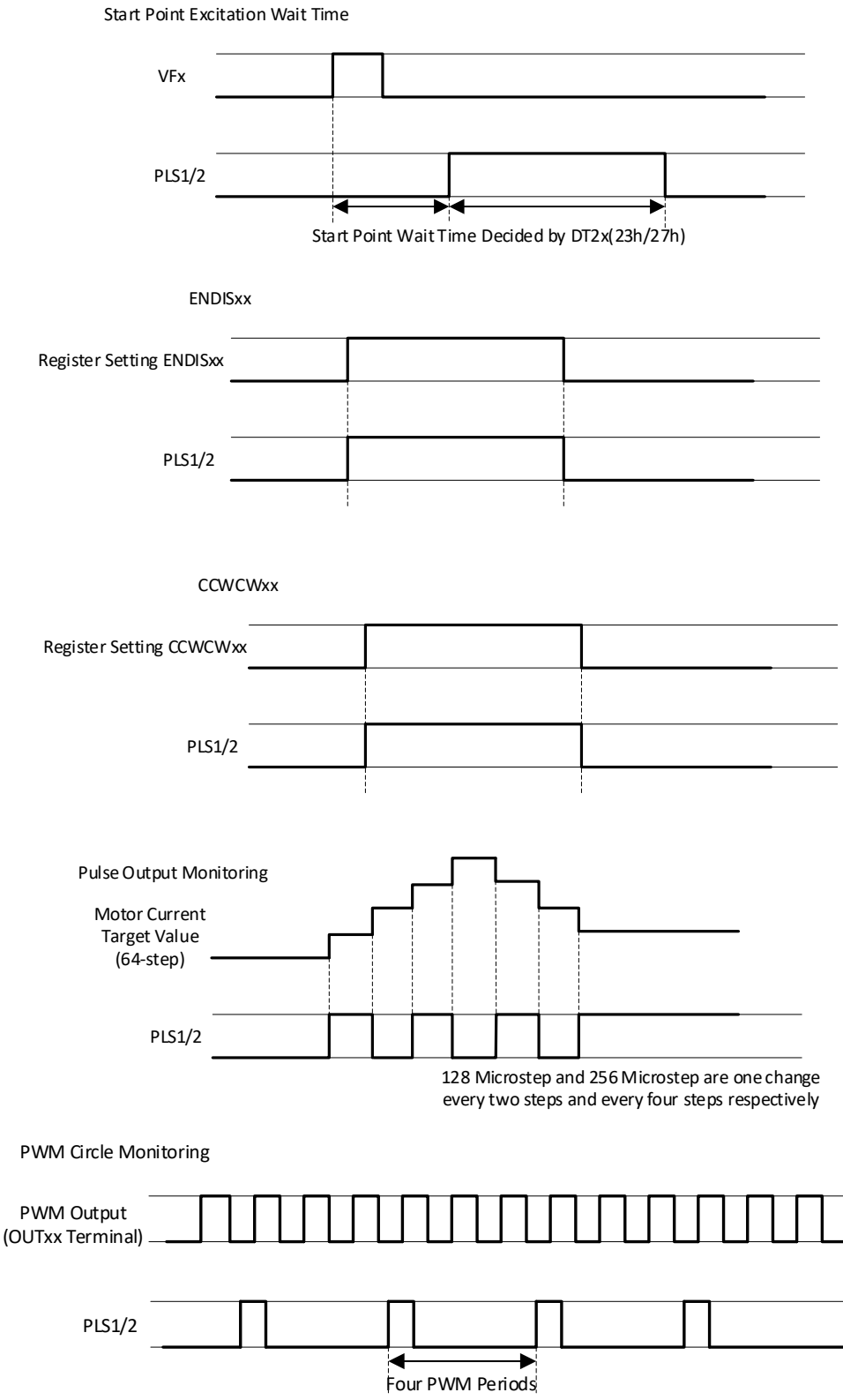
FZTEST[4:0] selects the test signals output by PLS1 and PLS2.

TESTEN2 need to be set to "1" to allow the test signal output.

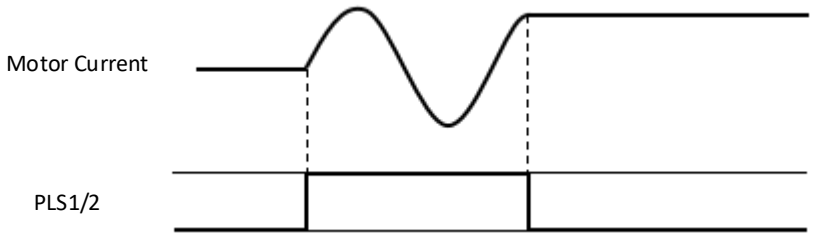
The following table is the output setting signal.

| Setting | A Cycle | | Description |
|---|---|---|---|
| | PLS1 | PLS2 | |
| 1 | Start Point Wait Time | 0 | H Bridge Output for Start Point Wait Time |
| 2 | Start Point Excitation Wait Time A | Start Point Excitation Wait Time B | H Bridge Output for Start Point Excitation Wait Time |
| 3 | ENDISAB | ENDISCD | ENDISxx Setting |
| 4 | CCWCWAB | CCWCWCD | CCWCWxx Setting |
| 5 | Monitor Output Pulse A | Monitor Output Pulse B | "H"/"L" change in 64 microstep when motor is rotating |
| 6 | PWM Cycle Monitoring | 0 | PWM Period Signal of Motor Output |
| 7 | Complete Pulse Output for Driver A | Complete Pulse Output for Driver B | H Bridge Output when Motor Rotating |
| 11 | "H" Bridge PMOS1 A | "H" Bridge NMOS1 A | Monitor Driver A |
| 12 | "H" Bridge PMOS2 A | "H" Bridge NMOS2 A | |
| 13 | "H" Bridge PMOS1 B | "H" Bridge NMOS1 B | Monitor Driver B |
| 14 | "H" Bridge PMOS2 B | "H" Bridge NMOS2 B | |
| 15 | "H" Bridge PMOS1 C | "H" Bridge NMOS1 C | Monitor Driver C |
| 16 | "H" Bridge PMOS2 C | "H" Bridge NMOS2 C | |
| 17 | "H" Bridge PMOS1 D | "H" Bridge NMOS1 D | Monitor Driver D |
| 18 | "H" Bridge PMOS2 D | "H" Bridge NMOS2 D | |

The relevant waveforms are described as follows:

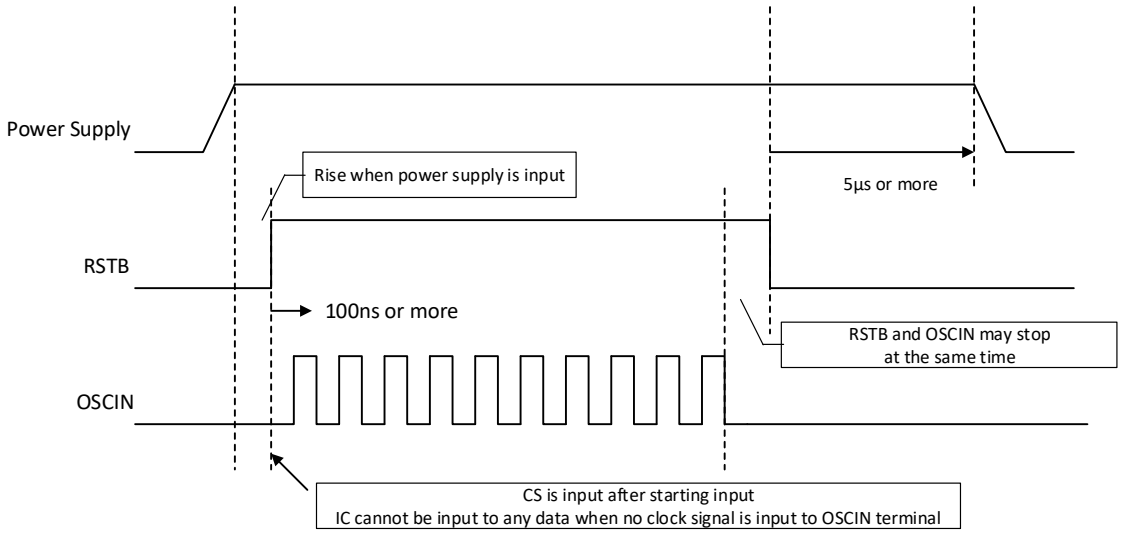


Complete Pulse Output




**(1) Start and Finish Timing**

The start and finish timing of power signal, RSTB and OSCIN are shown in the following figure.




**(2) Input Capacitance of Input Pin**

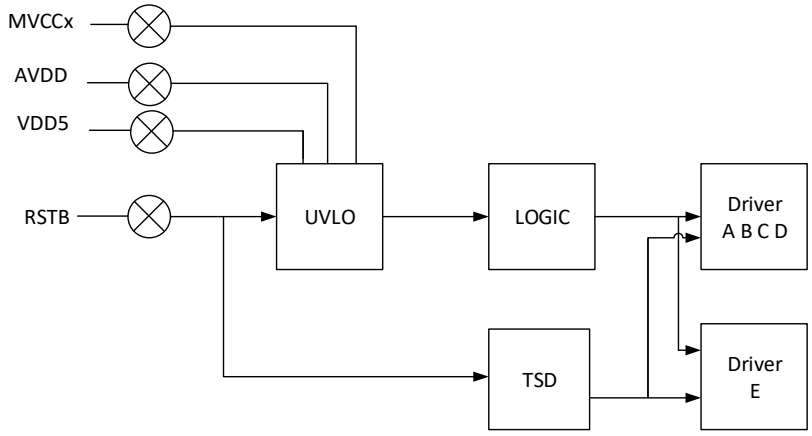
The capacitance of input pin is 10pF or less.

**(3) OSCIN, VFx Moment**

Once VFx signal is synchronized with OSCIN, the VFx and OSCIN signals have no constraint on input time.

**5. Reset/Protection Circuit**

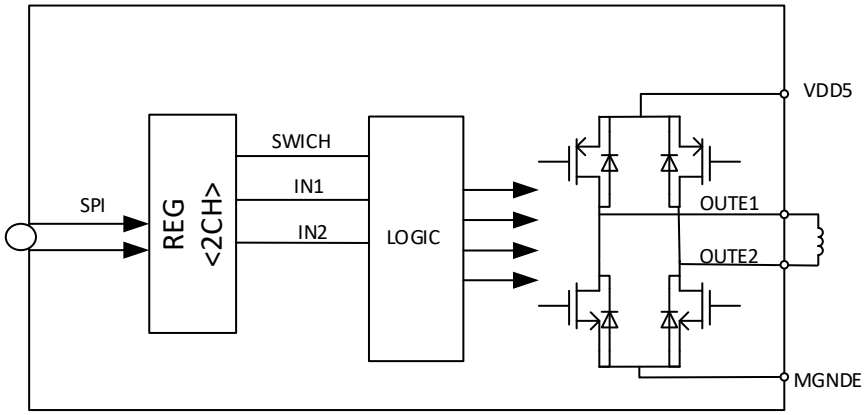
The following figure shows the relationship between RSTB, UVLO, TSD and other circuits.



The corresponding specifications are shown in the following table.

| | Function | Logic | Motor Output |
|---|---|---|---|
| RSTB | Disable | Logic Reset->Disable | Logic Reset->Output Shutdown |
| Thermal Shutdown (TSD) | × | × | Output Shutdown |
| Undervoltage Lockout (UVLO) | × | Logic Reset->Disable | Logic Reset->Output Shutdown |

**6. DC Driver E Circuit**




DC motor (used in IR-CUT in camera) driver adopts SPI input control method. H bridge output id controlled by writing register 2CH.

SWICH Register: Register REG_2CH<2> bit2, Power-up Default '0''

IN1 Register: Register REG_2CH<1> bit1, Power-up Default '0'

IN2 Register: RegisterREG_2CH<0> bit0, Power-up Default '0'

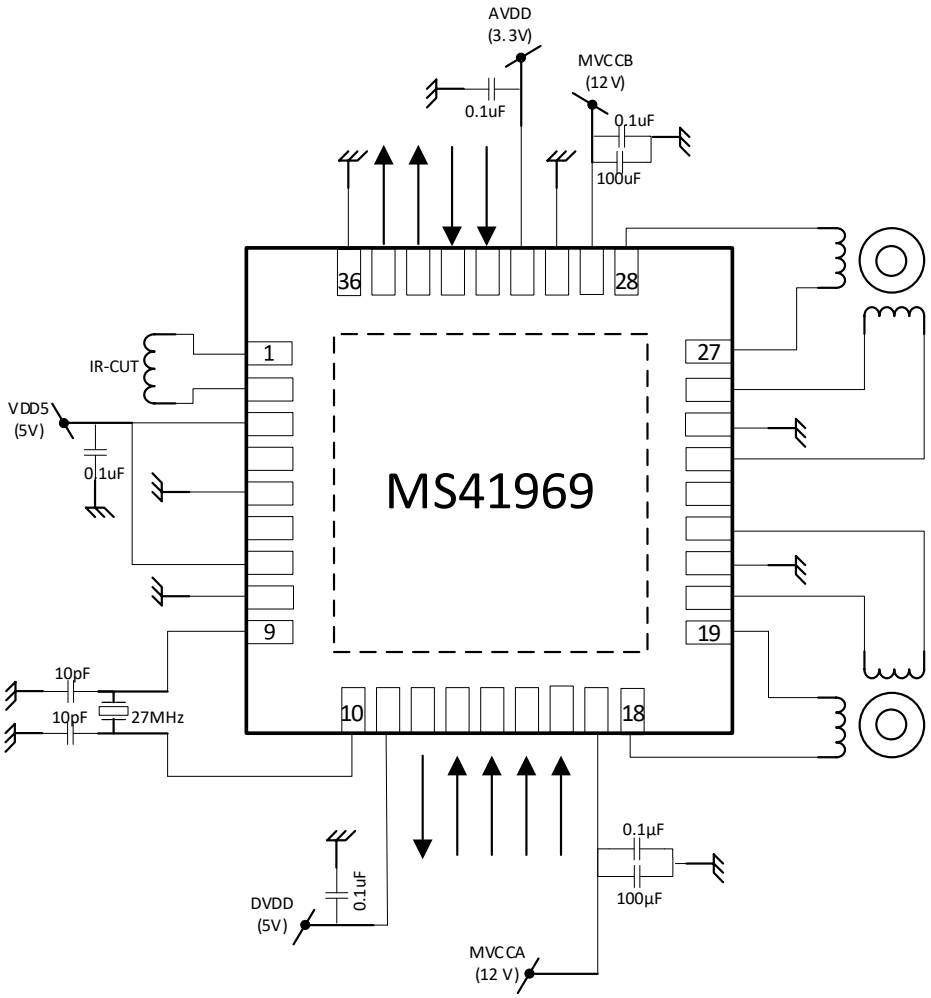
Truth table of input and output is as follows:

| Equivalent Control Signal for Internal Signal | | Register Control Mode | Output | | |
|---|---|---|---|---|---|
| IN1 | IN2 | Lower 8bits of 2CH Register | OUTE1 | OUTE2 | Motor State |
| 0 | 0 | 0004h | L | L | Brake |
| 0 | 1 | 0005h | L | H | Reverse |
| 1 | 0 | 0006h | H | L | Forward |
| 1 | 1 | 0007h | Z | Z | High -impedance |

**Delay Time of DC Motor in SPI Mode**

22 data and 3 control bits are written every writing in SPI mode. The transmission delay is about tsclk×25 from writing register2CH to actual work of control time. If the serial clock of writing data is 0.5MHz, the delay time is 25×1/0.5M=50μs. And the maximum output frequency of H bridge is 10kHz.

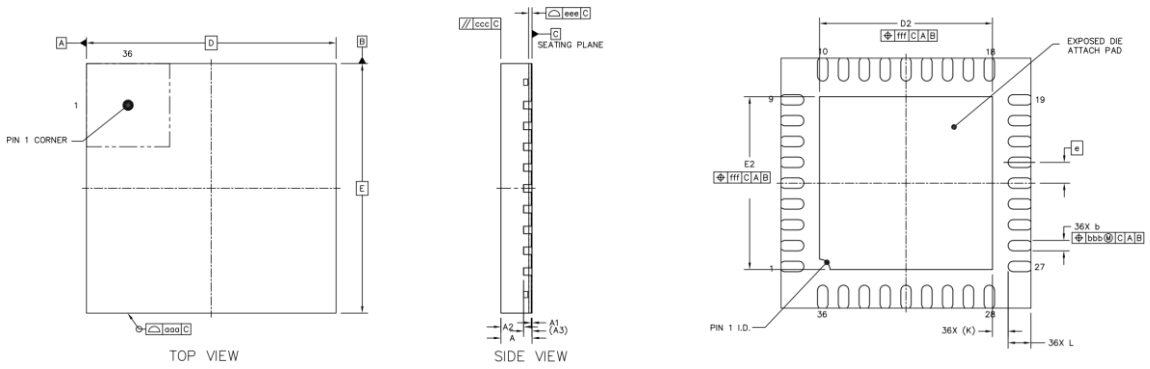
## TYPICAL APPLICATION DIAGRAM




1. The MS41969 has back thermal pad and it must be grounded in large power applications.
2. Amplification and SMIT circuits are built between OSCIN pin (PIN9) and OSCOUT(PIN10). Therefore, low-cost passive crystal oscillator can be used between OSCIN and OSCOUT. OSCIN pin is connected with active crystal oscillator output or other CLK output of MCU (OSCOUT floating) . The demands for DC and AC inputs are differential. The detailed parameters refer to page 8.

## PACKAGE OUTLINE DIMENSIONS

**QFN36 (0606X0.75_0.5)**




| Symbol | Dimensions in Millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.7 | 0.75 | 0.8 |
| A1 | 0 | 0.02 | 0.05 |
| A2 | - | 0.55 | - |
| A3 | 0.203 REF | | |
| b | 0.2 | 0.25 | 0.3 |
| D | 6 BSC | | |
| E | 6 BSC | | |
| e | 0.5 BSC | | |
| D2 | 4.05 | 4.15 | 4.25 |
| E2 | 4.05 | 4.15 | 4.25 |
| L | 0.45 | 0.55 | 0.65 |
| K | 0.375 REF | | |
| aaa | 0.1 | | |
| ccc | 0.1 | | |
| eee | 0.08 | | |
| bbb | 0.1 | | |
| fff | 0.1 | | |

## MARKING and PACKAGING SPECIFICATION

### 1. Marking Drawing Description


Product Name: MS41969

Product Code： XXXXXXX

### 2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

### 3. Packaging Specification

| Device | Package | Piece/Reel | Reel/Box | Piece /Box | Box/Carton | Piece/Carton |
|---|---|---|---|---|---|---|
| MS41969 | QFN36 | 2000 | 1 | 2000 | 8 | 16000 |

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com