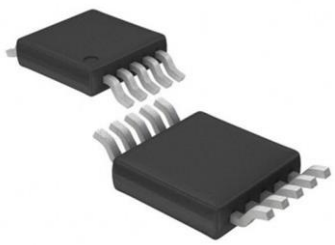
16-Bit, Four-Input, Built-in Reference ADC

PRODUCT DESCRIPTION

The MS5175 is a high-precision, continuously converting ADC with four single-ended input channels. It integrates 2.048V reference and uses I^2C compatible interface. The power supply range is from 2.7V to 5.5V. The MS5175 can perform conversions at rates of 15, 30, 60 or 240 samples per second (SPS). It integrates programmable gain amplifier(PGA). In single conversion mode, the MS5175 automatically enters into power-down state after conversion, greatly reducing power dissipation.

The MS5175 is designed for applications requiring high-resolution measurement and where space and power dissipation are major considerations, such as portable instrument, industry control and smart transmitter.



MSOP10

FEATURES

- Four Single-ended Input Channels
- I^2C Interface, Eight Programmable Addresses
- On-board Reference : 2.048V±0.1%
- Temperature Drift : 20ppm/℃
- Internal Integrated PGA : 1 to 8
- 16Bit No Missing Codes
- INL (Integral Nonlinearity) : 0.004%
- Operating Voltage : 2.7V to 5.5V
- Low Current Consumption : 270μA@VDD=3V

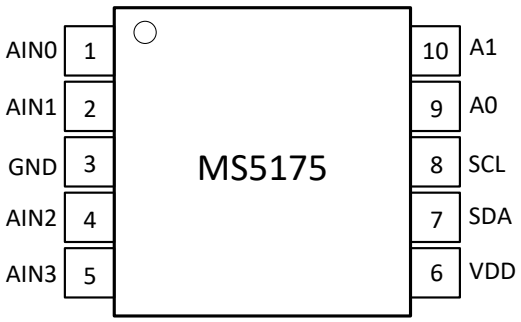
APPLICATIONS

- Portable Instrument
- Industrial Control
- Smart Transmitter
- Factory Automation
- Temperature Measurement

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5175	MSOP10	MS5175

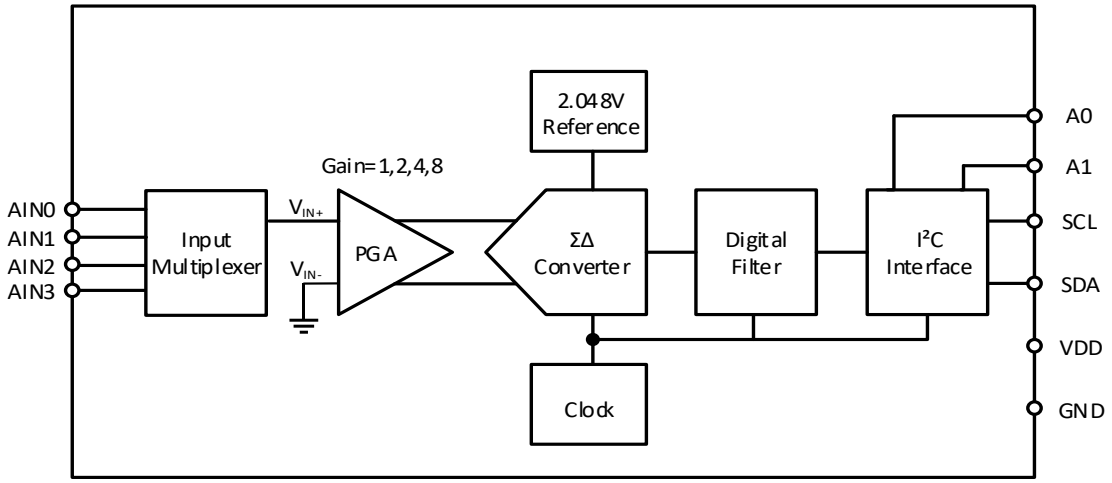
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	AIN0	I	Single-ended Input 1
2	AIN1	I	Single-ended Input 2
3	GND	-	Ground
4	AIN2	I	Single-ended Input 3
5	AIN3	I	Single-ended Input 4
6	VDD	-	Power Supply
7	SDA	I/O	Serial Data Transmitting and Receiving Terminal
8	SCL	I/O	Serial Clock Input, Clock Output Terminal
9	A0	I	I^2C Salve Address Selection 1
10	A1	I	I^2C Salve Address Selection 2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	V_{DD}	-0.3 ~ 6	V
Input Current	I_{IN}	100mA, Momentary	mA
		10mA, Continuous	mA
Analog Input (ASEL0, ASEL1 to GND)	V_{IN}	-0.3 ~ V_{DD}+0.3	V
SDA, SCL Voltage to GND	V	-0.5 ~ 6	V
Maximum Junction Temperature	T_{JMAX}	150	°C
Operating Temperature	T_A	-40 ~ 125	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C
Lead Temperature	T	260	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A= -40°C to 85°C, V_{DD}=5V.

Parameter	Condition	Min	Typ	Max	Unit
Analog Input					
Positive Full-scale Input Voltage	V_{IN+}		+2.048/PGA		V
Analog Input Voltage	V_{IN+} to GND	GND-0.3		V_{DD}+0.2	V
Input Impedance	PGA=1		3.5		MΩ
	PGA=2		3.5		MΩ
	PGA=4		1.8		MΩ
	PGA=8		0.9		MΩ
System Performance					
Resolution and No Missing Codes	DR=00		11		Bits
	DR=01		13		Bits
	DR=10		14		Bits
	DR=11		16		Bits
Output Rate	DR=00	216	240	264	SPS
	DR=01	54	60	66	SPS
	DR=10	27	30	33	SPS
	DR=11	13.5	15	16.5	SPS
Integral Nonlinearity	DR=11, PGA=1, End Point[1]		±0.004		% of FSR[2]
Offset Error	PGA=1		1	3	mV
	PGA=2		1	3	mV
	PGA=4		1	3	mV
	PGA=8		1	3	mV
Offset Drift	PGA=1		1.2		µV/°C
	PGA=2		0.6		µV/°C
	PGA=4		0.3		µV/°C
	PGA=8		0.3		µV/°C
Offset VS. VDD	PGA=1		800		µV/V
	PGA=2		400		µV/V
	PGA=4		200		µV/V
	PGA=8		150		µV/V

Parameter	Condition	Min	Typ	Max	Unit
System Performance					
Gain Error		-0.5	±0.1	+0.5	%
PGA Gain Match Error [3]	Any two gains match		0.02		%
Gain Error Drift			20		ppm/°C
Gain VS. VDD			80		ppm/V
Common-mode Rejection Ratio	DC Input, PGA=8		105		dB
	DC Input, PGA=1		100		dB
Digital Input/Output					
Input High Level		$0.7\times V_{DD}$		$V_{DD}+0.5$	V
Input Low Level		GND-0.5		$0.3\times V_{DD}$	V
Output Low Level	I_{OL}=3mA	GND		0.4	V
Input High Peak Current				10	μA
Input Low Peak Current		-10			μA
Power Performance					
Operating Voltage	VDD	2.7		5.5	V
Supply Current	Power down		0.05	3	μA
	Operation@V_{DD}=3V		270	300	μA
Power Dissipation	V_{DD}=5.0V		1.5		mW
	V_{DD}=3.0V		0.81	0.9	mW

Note:

1. 99% of full-scale.
2. FSR = full-scale range = 2.048V/PGA.
3. Includes all errors from PGA and reference.

FUNCTION DESCRIPTION

The MS5175 is a 16-bit, four input channels, delta-sigma A/D converter. It has easy design and configuration, so users can easily achieve accurate measurement.

Analog-to-Digital Converter

The A/D converter core consists of a switched-capacitor Σ-Δ modulator and a digital filter.

Input Multiplexer

The MS5175 can provide four single-ended input channels. The two bits of configuration register control the input multiplexer.

Voltage Reference

The MS5175 contains an on-board 2.048V voltage reference without need for external reference.

Output Code Calculation

The number of bits for the MS5175 depends on update rate, as shown in Table 1.

Table 1. Maximum Code

Update Rate	Number Of Bits	Maximum Code (MSB Sign Bit)
15SPS	16	32767
30SPS	15	16383
60SPS	14	8191
240SPS	12	2047

The output code of the MS5175 is in binary two's complement format, right-justified and sign-extended. Table 2 shows the output codes for various input levels.

Table 2. Output Codes for Different Input Signals

Update Rate	Input Signal		
	0 (Ideal)	+1LSB	+2.048V
15SPS	0000_H	0001_H	$7FFF_H$
30SPS	0000_H	0001_H	$3FFF_H$
60SPS	0000_H	0001_H	$1FFF_H$
240SPS	0000_H	0001_H	$07FF_H$

Note 1: Do not drive the input voltage below GND.

The output code is given by the expression:

$$\text{Output Code} = 1\times\text{Maximum Code}\times\text{PGA}\times\frac{(V_{IN+})-(V_{IN-})}{2.048V} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (V_{IN+}\geqslant V_{IN-})$$

The maximum code is 2^{n-1}-1.

Clock Oscillator

The MS5175 features an on-board clock oscillator, which drives the modulator and digital filter without need for external clock.

Input Impedance

The input stage of the MS5175 uses switched-capacitor. The equivalent resistance value depends on the capacitor value and switching frequency. The capacitor value depends on the PGA setting. The clock is generated by the on-board clock oscillator. The typical operating frequency is 275kHz.

For input source with high output impedance, buffer may be necessary externally on input terminal.

Aliasing

If the input signal frequency of the MS5175 exceeds half of the update rate, aliasing will occur. To prevent aliasing, the input signal must be band-limited. The digital filter of the MS5175 provides some attenuation of high-frequency noise to some extent, but sinc filter cannot completely replace an anti-aliasing filter. For a few applications, external filtering also is needed.

When designing input filter circuit, remember to take into account the impedance match between the filter and the MS5175 input.

Operation Mode

The MS5175 has two conversion modes : continuous conversion and single conversion.

In continuous conversion mode, after a conversion has been completed, the MS5175 places the result in the result register and immediately begins another conversion.

In single conversion mode, the MS5175 will wait until the ST/DRDY bit in the configuration register is set to 1. Then the MS5175 start a conversion. After the conversion is completed, the MS5175 places the result in the result register, resets the ST/DRDY bit to 0 and powers down.

When switched from continuous conversion mode to single conversion mode, the MS5175 completes the current conversion, resets the ST/DRDY bit to 0 and powers down.

Reset and Power-up

When the MS5175 powers up, it automatically performs one reset. All of the bits in the configuration register are set to their default settings.

The MS5175 responds to the I^2C General Call Reset command. When the MS5175 receives a General Call Reset, it performs a reset.

I^2C Interface

The MS5175 communicates through I^2C interface. A timing diagram is shown in Figure 1. The related parameters for this diagram are given in Table 3.

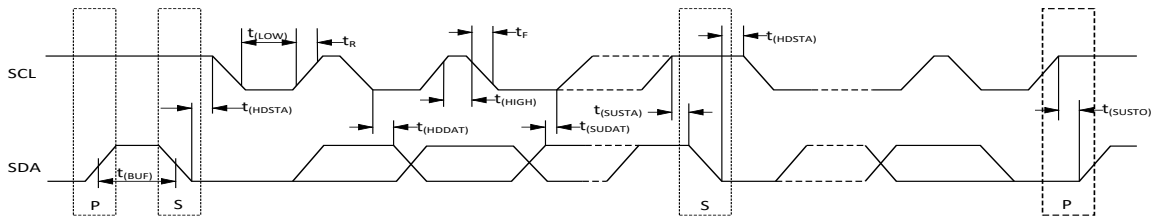


Figure 1. I^2C Timing Diagram

Table 3. Related Parameters For Timing Diagram

Parameter		Min	Max	Unit
$t_{(SCLK)}$	SCLK Operating Frequency		0.4	MHz
$t_{(BUF)}$	Bus START to STOP Idle Time	600		ns
$t_{(HDSTA)}$	START Hold Time	600		ns
$t_{(SUSTA)}$	Repeated START Setup Time	600		ns
$t_{(SUSTO)}$	STOP Setup Time	600		ns
$t_{(HDDAT)}$	Data Hold Time	0		ns
$t_{(SUDAT)}$	Data Setup Time	100		ns
$t_{(LOW)}$	SCLK Clock Low Level Period	1300		ns
$t_{(HIGH)}$	SCLK Clock High Level Period	600		ns
t_F	Clock/Data Fall Time		300	ns
t_R	Clock/Data Rise Time		300	ns

Serial Bus Address

In order to read from and write to the MS5175, the master must address to the slave. The slave address includes seven address bits and one operation bit.

The MS5175 has two address pins, ASEL0 and ASEL1, setting I^2C address. The pin could be set as logic low, logic high or Float. Eight different addresses can be set by the two pins, as shown in Table 4. After power-up reset or I^2C General Call Reset command, ASEL0 and ASEL1 pin states are sampled.

Table 4. MS5175 Address Pin and Slave Address

A0	A1	Slave Address
0	0	1001000
0	Float	1001001
0	1	1001010
1	0	1001100
1	Float	1001101
1	1	1001110
Float	0	1001011
Float	1	1001111
Float	Float	Invalid

I²C General Call

If the eight address is 0, the MS5175 would respond to general call. The device acknowledges and responds to the second byte command. If the command is 04h, the MS5175 would latch the states of address pins ASEL0,ASEL1 without reset. If the command is 06h, the MS5175 would latch the state of address pin and reset configuration register.

I²C Data Rate

I²C bus has three speed modes : standard mode, allowing the clock frequency up to 100kHz; fast-speed mode, allowing the clock frequency up to 400kHz; high-speed mode, allowing the clock frequency up to 3.4MHz.

About more information about high-speed mode, please refer to I²C specification.

Result Register

The 16-bit result register contains the conversion result in binary two's complement format. After reset or power-up, the result register is cleared 0, and remains until the first conversion is completed. The format of result register is shown in Table 5.

Table 5. Result Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Configuration Register

The 8-bit configuration register can be used to control the operation mode, update rate and PGA. The format of configuration register is shown in Table 6. The default setting is 8CH.

Table 6. Configuration Register

Bit	7	6	5	4	3	2	1	0
Name	ST/DRDY	INP1	INP0	SC	DR1	DR0	PGA1	PGA0
Default	1	0	0	0	1	1	0	0

Bit 7: ST/DRDY

The meaning of the ST/DRDY bit depends on whether it is being written to or read from.

In single conversion mode, writing 1 to the ST/DRDY bit indicates a conversion to start, and writing 0 has no effect. In continuous mode, the MS5175 ignores the value written to ST/DRDY.

In continuous conversion mode, use ST/DRDY bit to determine whether new conversion data is ready. If ST/DRDY is 1, the data in the result register has already been read. If it is 0, the data in the result register is new, and has not yet been read.

In single conversion mode, use ST/DRDY bit to determine whether a conversion has completed. If ST/DRDY is 1, the data in the result register is old, and the conversion is still in process. if it is 0, the data in the result register is the new conversion result.

The MS5175 first outputs the value of result register, then the value of configuration register. The state of the ST/DRDY bit applies to the data just read from the result register, rather than the data from the next read operation.

Bit 6-5: INP

Input signal select bits. The MS5175 can select four single-ended input channels by the two bits, as shown in Table 7.

Table 7. INP Bit Setting

INP1	INP0	VIN
0 (Default Value)	0 (Default Value)	AIN0
0	1	AIN1
1	0	AIN2
1	1	AIN3

Bit 4: SC

Conversion mode select bit. When SC is 1, the MS5175 is in single conversion mode; when SC is 0, it is in continuous conversion mode. The default setting is 0.

Bit 3-2: DR

Update rate select bits, as shown in Table 8.

Table 8. DR Bit Setting

DR1	DR0	Update Rate	Resolution
0	0	240SPS	12Bit
0	1	60SPS	14Bit
1	0	30SPS	15Bit
1(Default Value)	1 (Default Value)	15SPS	16Bit

Bit 1-0: PGA

Gain setting select bits, as shown in Table 9.

Table 9. PGA Bit Setting

PGA1	PGA0	Gain
0 (Default Value)	0 (Default Value)	1
0	1	2
1	0	4
1	1	8

Reading from the MS5175

Read the value in the result register and the configuration register. First address the MS5175, then read three bytes from the device. The first two bytes are the result register's contents, and the third byte is the configuration register's contents.

It is not required to read the configuration register. It is permissible to read fewer than three bytes during a read operation. Reading more than three bytes from the MS5175 has no effect. All bytes from the fourth byte will be FFH.

The timing diagram of typical read operation for the MS5175 is shown in Figure 2.

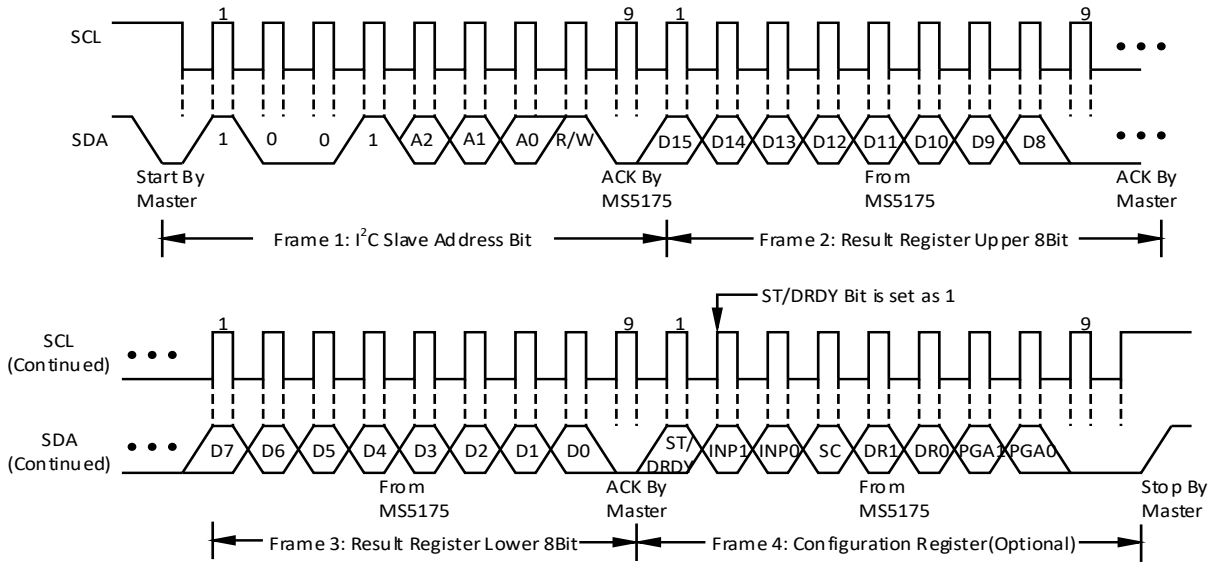


Figure 2. Timing Diagram of the MS5175 Read Operation

Writing to the MS5175

Write to the configuration register. First address the MS5175, then write into one byte. The byte will be written to the configuration register.

Writing more than one byte to the MS5175 has no effect. The MS5175 will ignore any byte after the first byte. The timing diagram of typical write operation for the MS5175 is shown in Figure 3.

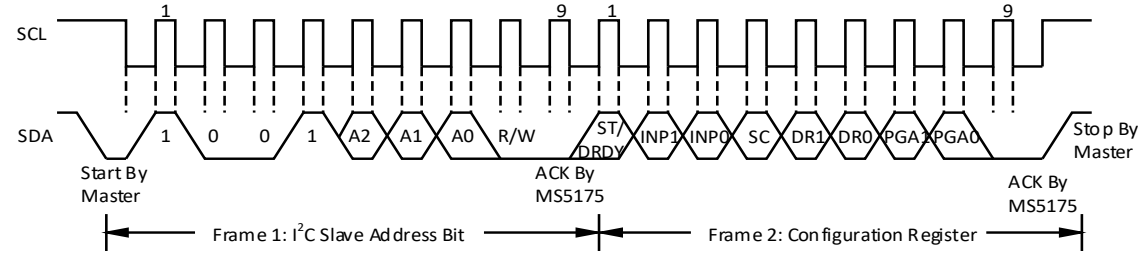


Figure 3. Timing Diagram of the MS5175 Write Operation

APPLICATION DESCRIPTION

Basic Connection

For many applications, the basic connection diagram of the MS5175 is shown in Figure 4.

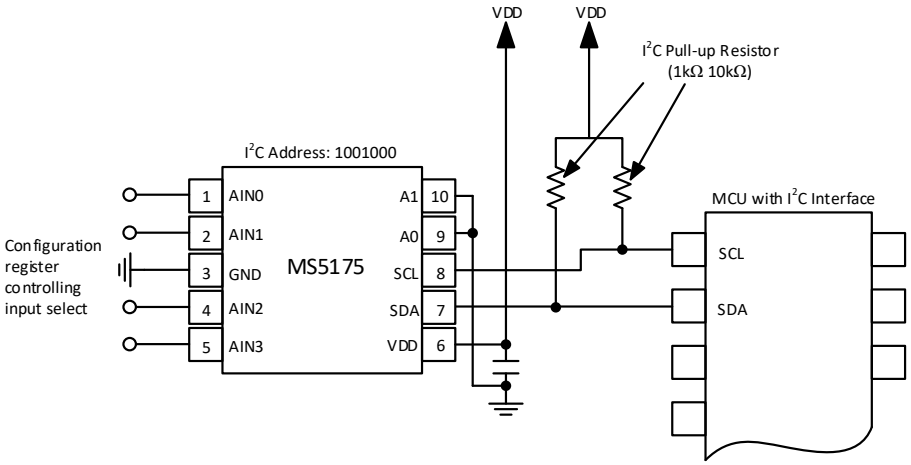


Figure 4. Typical Connection of the MS5175

Connecting Multiple Devices

Multiple MS5175s can be connected to a I²C bus. The MS5175 is available in different eight versions by ASEL1 and ASEL0 pins. An example showing three MS5175s connected on a same bus is shown in Figure 5. Up to eight MS5175s (controlled by differential states of ASEL1 and ASEL0 pins) can be connected to one I²C bus.

Note that I²C bus only needs one set of pull-up resistors.

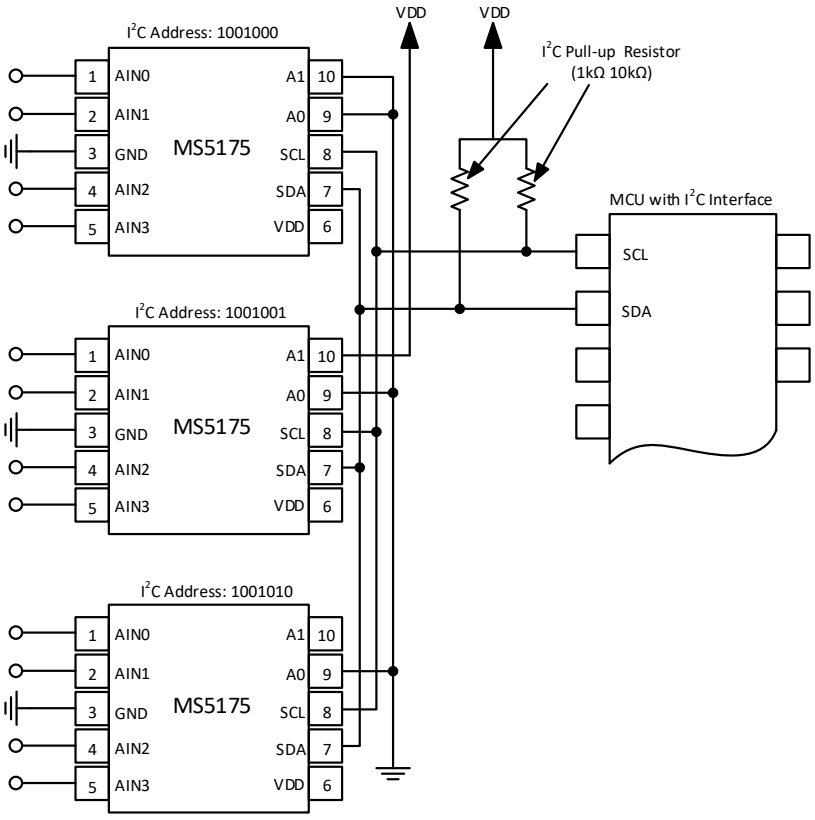


Figure 5. Connecting Multiple MS5175s

Low-Side Current Monitor

Figure 6 shows a circuit for a low-side current monitor. The circuit reads the voltage across a shunt resistor, the voltage of which is amplified by the MS8552, and the result is read by the MS5175.

It is suggested that the MS5175 be operated at a gain of 8. The gain of the MS8552 can be reduced. For a gain of 8, the op amp should provide output voltage of no greater than 0.256V. Therefore, the shunt resistor is sized to provide a maximum voltage drop of 64mV at full-scale current.

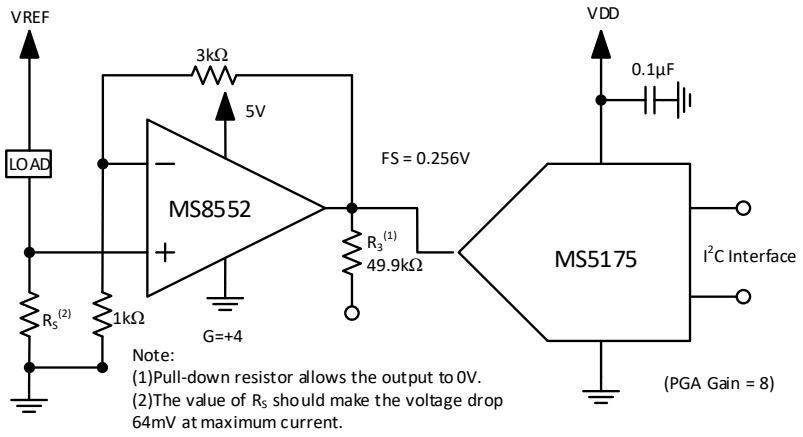
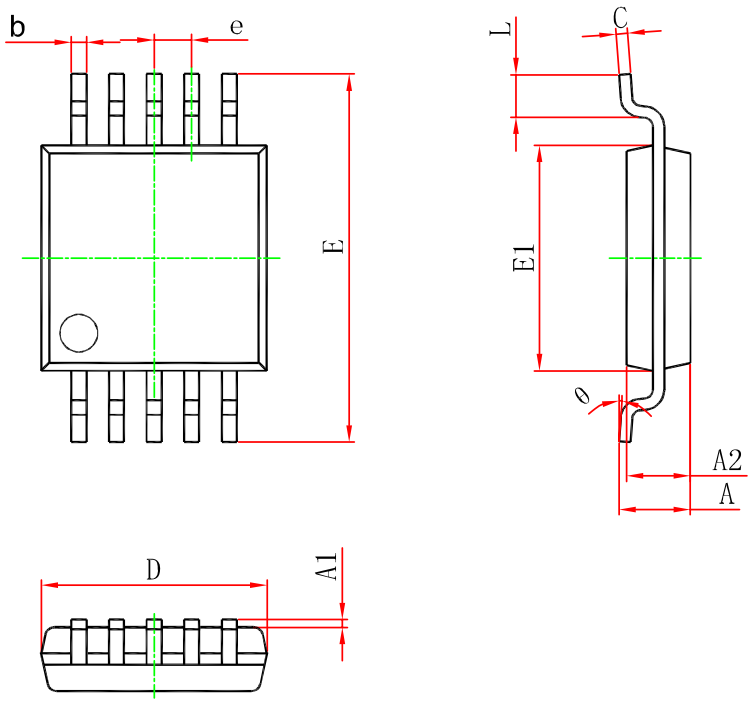


Figure 6. Low-side Current Measurement

PACKAGE OUTLINE DIMENSIONS

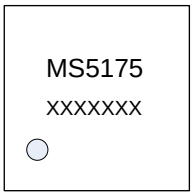
MSOP10



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	-	1.100	-	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.330	0.007	0.013
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50BSC		0.020BSC	
E	4.750	5.050	0.187	0.199
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031
θ	0º	6º	0º	6º

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name : MS5175

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5175	MSOP10	3000	1	3000	8	24000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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