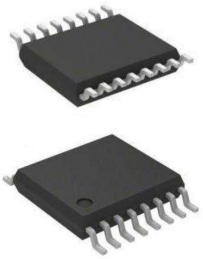
16-bit Σ-Δ Analog to Digital Converter

PRODUCT DESCRIPTION

The MS5213T is an analog-to-digital converter for low-frequency measurement. It uses Σ-Δ conversion technology to realize 16-bit no missing code feature. The operating voltage range is 2.7V-3.3V or 4.75V-5.25V. And the MS5213T has two fully differential analog input channels.

The MS5213T is ideal for intelligent, micro-controller, or DSP-based systems. It can set gain, signal polarity and output rate via serial interface. Self-calibration and system calibration can be applied to eliminate gain and offset errors of the system. The typical power dissipation is 20uW in standby mode.



TSSOP16

FEATURES

- Two Fully Differential Input Channels
- 16-bit No Missing Codes
- 0.003% Non-linearity
- PGA: Gain from 1 to 128
- 3-Wire Serial Port: SPI, QSPI, MICROWIRE, DSP Compatible
- Operating Voltage : 2.7V to 3.3V or 4.75V to 5.25V
- Maximum Power Dissipation : 1mW under 3V Power Supply
- Maximum Standby Current : 8μA
- TSSOP16 Package

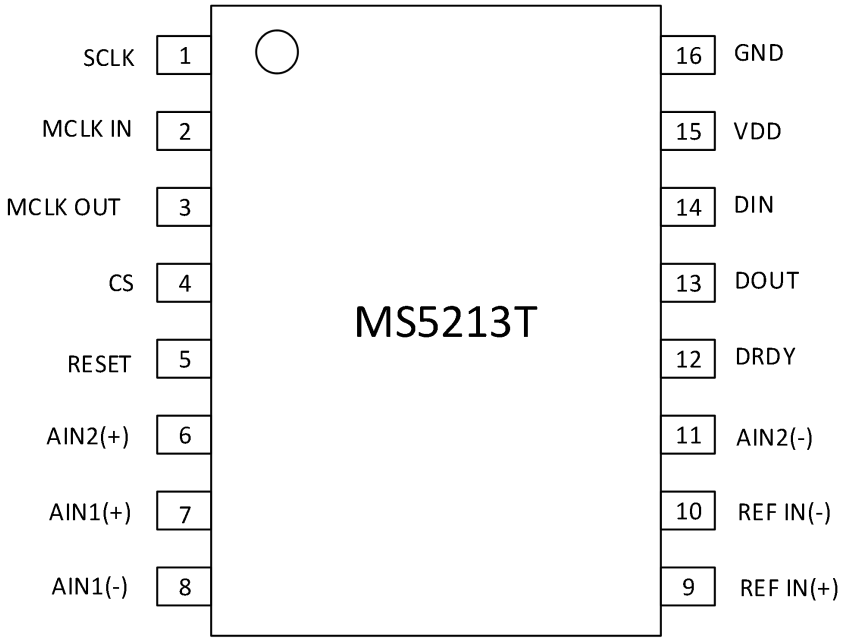
APPLICATIONS

- Stress Measurement
- Temperature Measurement
- Battery Monitoring
- Smart Transmitter

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5213T	TSSOP16	MS5213T

PIN CONFIGURATION

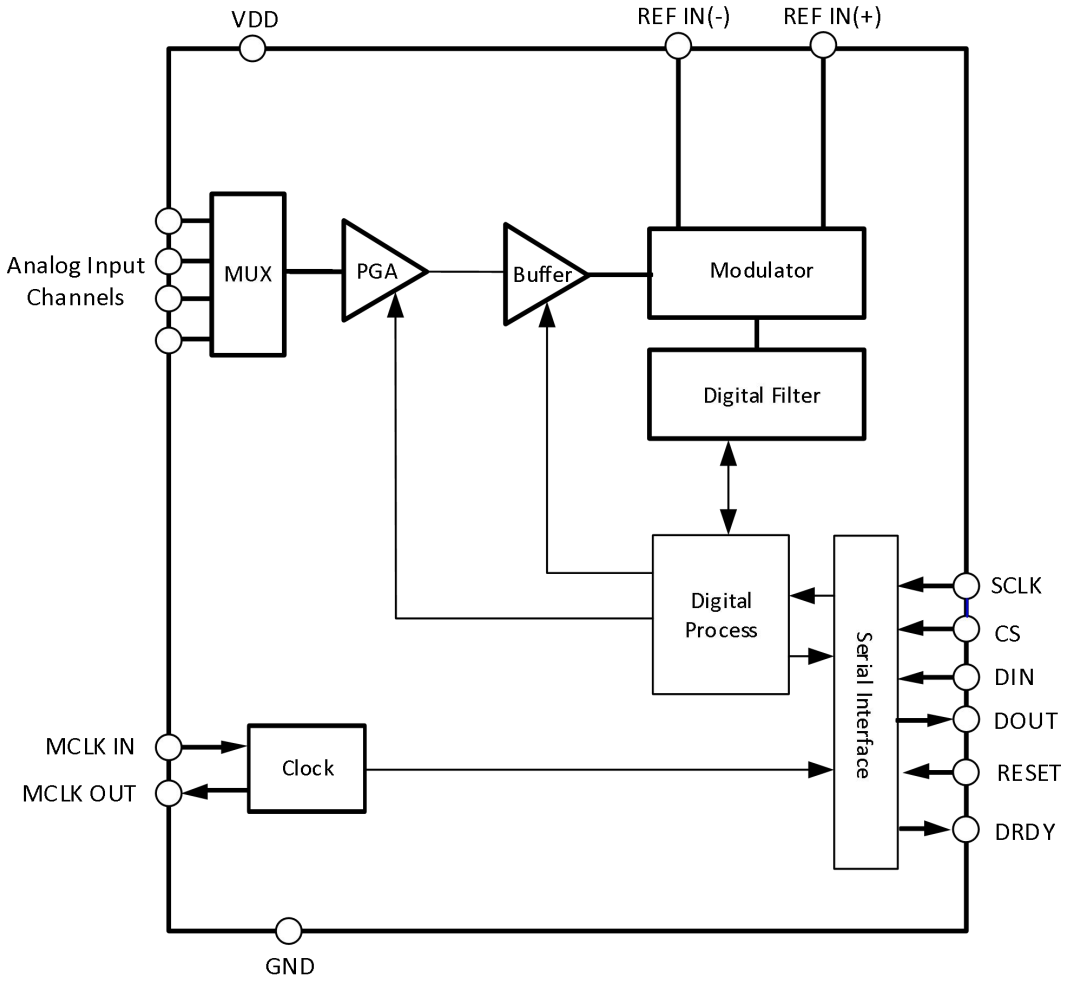


PIN DESCRIPTION

Pin	Name	Type	Description
1	SCLK	I	Serial Clock Input
2	MCLK IN	I	Master Clock Signal. It can be provided in the form of crystal/ resonator or external clock. The crystal/resonator can be connected between MCLK IN and MCLK OUT pins. MCLK IN can also be driven by CMOS compatible clock, but MCLK OUT is not connected. The clock frequency ranges from 500kHz to 5MHz.
3	MCLK OUT	O	When master clock is crystal/ resonator, it is connected between MCLK IN and MCLK OUT pins. If one external clock is connected on MCLK IN, MCLK OUT will provide an inverted clock signal. This clock can be used to provide clock source for external circuit and drive a CMOS load. MCLK OUT can be turned off by CLKDIS bit in clock register. Thus, the device doesn't consume unnecessary power driving capacitance load on MCLK OUT pin.
4	CS	I	Chip Select, Active Low Logic Input. When communicating with the MS5213T, CS can be used as frame synchronous signal.
5	RESET	I	Reset Input. Active Low Input.
6	AIN2(+)	I	Positive Input of Differential Analog Input Channel 2
7	AIN1(+)	I	Positive Input of Differential Analog Input Channel 1
8	AIN1(-)	I	Negative Input of Differential Analog Input Channel 1
9	REF IN(+)	I	Reference Input Terminal, Positive Input of Differential Reference. The reference input is differential and requires that REFIN (+) must be more than REFIN (-). REFIN (+) can be any value between VDD and GND.
10	REF IN(-)	I	Reference Input Terminal, Negative Input of Differential Reference. REFIN(-) can be any value between VDD and GND. And REFIN (+) must be more than REFIN (-).
11	AIN2(-)	I	Negative Input of Differential Analog Input Channel 2

Pin	Name	Type	Description
12	DRDY	O	Logic Output. The low logic level on this output terminal indicates that the newest results can be obtained from data register. After completing a read operation of complete output word, DRDY immediately returns to high level. If there is no data readout between two output updates, DRDY will return to high level for 500× tCLKIN before the next update occurs . When DRDY is high level, it can not read data, for fear that data in the data register is read when it is updating. After data is updated, DRDY returns to low level. DRDY is also used to indicate when the MS5213T has completed the on-chip calibration sequence
13	DOUT	O	Serial Data Output Terminal.
14	DIN	I	Serial Data Input Terminal.
15	VDD	-	Power Supply, + 2.7V to + 5.25V.
16	GND	-	Ground Reference Point of Internal Circuit.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability.The absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VDD	-0.3 ~ +7.0	V
Analog Input Voltage	V_{IN}	-0.3 ~ VDD+0.3	V
Reference Input Voltage	V_{REF}	-0.3 ~ VDD+0.3	V
Digital Input Voltage	V_{DIN}	-0.3 ~ VDD+0.3	V
Digital Output Voltage	V_{OUT}	-0.3 ~ VDD+0.3	V
Operating Temperature	T_A	-40 ~ 85	°C
Storage Temperature	T_{stg}	-60 ~ 150	°C
Lead Temperature(10s)		260	°C
Electrostatic Protection	ESD	>4000	V

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, VDD=3V, 5V or 2.5V, REF(+)=1.225V, REF(-)=GND, MCLK IN=2.4576MHz.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristic						
No Missing Codes				16		Bits min
Output Noise				See Table 2 and Table 4		
Integral Nonlinearity [1]				±0.003		% of FSR MAX
Unipolar Offset Error [2]						
Unipolar Offset Drift [3]				0.5		μV/°C
Bipolar Offset Error [2]						
Bipolar Offset Drift [3]		Gain=1~4		0.5		μV/°C
		Gain=8~128		0.1		
Positive Full-Scale Error [2,4]						
Full-Scale Drift [3,5]				0.5		μV/°C
Gain Error [2,6]						
Gain Drift [3,7]				0.5		ppm of FSR/°C
Negative Full-Scale Error						
Bipolar Negative Full-Scale Error [1]				±0.001	±0.003	% of FSR
Bipolar Negative		Gain =1~4		1		μV/°C
Full-Scale Drift [3]		Gain =8~128		0.6		μV/°C
Analog Input / Reference Input (unless otherwise noted, only for AIN and REF IN)						
Common-mode Rejection [1]	CMR	VDD=5V, Gain=1		96		dB
		VDD=5V, Gain=2		105		
		VDD=5V, Gain=4		110		
		VDD=5V, Gain=8~128		130		
		VDD=3V, Gain=1		105		
		VDD=3V, Gain=2		110		
		VDD=3V, Gain=4		120		
		VDD=3, Gain=8~128		130		

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Normal-mode 50 Hz Rejection [1]		Filter Notch 25Hz,50Hz, ± 0.02 × f_{NOTCH}		98		dB
		Filter Notch 20Hz,60Hz, ± 0.02 × f_{NOTCH}		98		dB
		Filter Notch 25Hz,50Hz, ± 0.02 × f_{NOTCH}		150		dB
		Filter Notch 20Hz,60Hz, ± 0.02 × f_{NOTCH}		150		dB
Absolute/Common-mode REF IN Voltage [1]			GND		VDD	V
Absolute/Common-mode AIN Voltage [1,8,9]		BUF=0	GND-0.1		VDD+0.03	V
Absolute/Common-mode AIN Voltage [1,8]		BUF=1	GND+0.05		VDD-1.5	V
AIN DC Input Current [1]					1	nA
AIN Sample Capacitance [1]					10	pF
AIN Differential Voltage [10]		BUF=1		0 to $+V_{REF}$/Gain		V
		BUF=0		$\pm V_{REF}$/Gain [11]		
AIN Input Sample Rate	f_s			Gain×f_{CLKIN}/64		MHz
				f_{CLKIN}/8		
Reference Input		VDD=2.7~3.3V V_{REF}=1.225±1%	1		1.75	V
		VDD=4.75~5.25V V_{REF}=2.5±1%	1		3.5	
Reference Input Sample Rate				f_{CLKIN}/64		MHz
Logic Input						
Input Current		All Inputs Except MCLK IN		±1nA	±1μA	μA
		MCLK IN		±2	±10	

Input Low Voltage, Except SCLK and MCLK IN	V_{INL}	VDD=5V			0.8	V
		VDD=3V			0.4	
Input High Voltage, Except SCLK and MCLK IN	V_{INH}	VDD=3V or 5V	2.0			V
Only SCLK (Schmitt-Triggered Input)	V_{T+}	VDD=5V	1.4		3	V
	V_{T-}		0.8		1.4	
	V_{T+}- V_{T-}		0.4		0.8	
	V_{T+}	VDD=3V	1		2	
	V_{T-}		0.4		1.1	
	V_{T+}- V_{T-}		0.375		0.8	
MCLK IN Low Voltage		VDD=5V			0.8	V
		VDD=3V			0.4	
Logic Output (including MCLK OUT)						
Output Low Voltage		VDD=5V, I_{SINK}=800μA (Except MCLK OUT) [12]			0.4	V
		VDD=3V, I_{SINK}=100μA (Except MCLK OUT) [12]			0.4	
Output High Voltage		VDD=5V, I_{SOURCE}=200μA (Except MCLK OUT) [12]	4			V
		VDD=3V, I_{SOURCE}=100μA (Except MCLK OUT) [12]	VDD-0.6			
Leakage Current, Floating State					±10	μA
Output Capacitance, Floating State [13]				9		pF
Data Output Code		Unipolar Mode	Binary			
		Bipolar Mode	Offset Binary			
System Calibration						
Positive Full-Scale Limit [14]		Gain=1~128			$(1.05\times V_{REF})$/Gain	V
Negative Full-Scale Limit [14]		Gain=1~128			$-(1.05\times V_{REF})$/Gain	V
Offset Limit [14]		Gain=1~128			$-(1.05\times V_{REF})$/Gain	V
Input Range [15]		Gain=1~128	$(0.8\times V_{REF})$/Gain		$(2.1\times V_{REF})$/Gain	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Dissipation (Apply External Clock , CLKDIS =1, Digital I/Ps = 0V or VDD)						
Power Supply Current [16]		VDD=2.7~3.3V				
	I_{DD}	BUF=0, f_{CLKIN}=1MHz, Gain=1~128			0.32	mA
		BUF=1, f_{CLKIN}=1MHz, Gain=1~128			0.6	
		BUF=0, f_{CLKIN}=2.4576MHz, Gain=1~4			0.4	
		BUF=0, f_{CLKIN}=2.4576MHz, Gain=8~128			0.6	
		BUF=1, f_{CLKIN}=2.4576MHz, Gain=1~4			0.7	
		BUF=1, f_{CLKIN}=2.4576MHz, Gain=8~128			1.1	
Power Supply Current [16]		VDD=4.75~5.25V				
	I_{DD}	BUF=0, f_{CLKIN}=1MHz, Gain=1~128			0.45	mA
		BUF=1, f_{CLKIN}=1MHz, Gain=1~128			0.7	
		BUF=0, f_{CLKIN}=2.4576MHz, Gain=1~4			0.6	
		BUF=0, f_{CLKIN}=2.4576MHz, Gain=8~128			0.85	
		BUF=1, f_{CLKIN}=2.4576MHz, Gain=1~4			0.9	
		BUF=1, f_{CLKIN}=2.4576MHz, Gain=8~128			1.3	
Standby Power Dissipation[17]		MCLK IN = 0 V or VDD, VDD = 3 V		8		uA
		MCLK IN = 0 V or VDD, VDD = 5 V		16		
Power Supply Rejection [18,19]						dB

1. These data has been determined at initial design.
2. Calibration is one conversion, Table 2 and Table 4 show these noise error. This is suitable for after calibration under expected temperature.
3. These drift error would be eliminated after re-calibration under any temperature.
4. Full-scale error includes zero-scale error (unbipolar drift error or bipolar zero-scale error) and it is applicable for unbipolar and bipolar input ranges.
5. Full-scale drift includes zero-scale drift (unbipolar offset drift or bipolar zero-scale drift). It is applicable for unbipolar and bipolar input ranges.
6. Gain error doesn't include zero-scale error. The calculation method : unbipolar range (full-scale error-unbipolar offset error); bipolar range (full-scale error-bipolar zero-scale error).
7. Gain drift doesn't include unbipolar offset drift and bipolar zero-scale drift. When zero-scale calibration is executed, gain drift is the system drift value.
8. Common-mode voltage range: analog input voltage (GND-100mV) to (VDD+30mV).
9. The analog input voltage of the MS5213T can low to GND-200mV, but leakage current would be increased.

10. The voltage range on AIN(+) is respective to AIN(-).
11. V_{REF} = REF IN(+) - REF IN(-)。
12. Only when one CMOS load is loaded, these logic output levels are applicable for MCLK OUT.
13. Test sample at +25°C to ensure consistency.
14. After calibration, if analog input is more than positive full-scale, converter would output all 1; if less than negative full-scale, converter would output all 0.
15. Calibration voltage limit shouldn't more than VDD+30mV or less than GND-100mV applied on analog input terminal. Offset calibration limit is suitable for unbipolar point and bipolar zero point.
16. When use crystal or ceramic oscillator as clock source of MCLK, the current and power dissipation of VDD depend on the type of crystal and ceramic oscillator (see "clock and oscillator").
17. In standby mode, if external master clock works continuously, the typical value of standby current would increase to 150μ(VDD=5V) or 75μA(VDD=3V). When use crystal or ceramic oscillator as clock source, internal oscillator would work continuously work in standby mode, and the power supply current would vary with the type of crystal and ceramic oscillator (see "standby mode").
18. The measurement in DC only apply to the selected passband frequency. PSRR exceeds 120dB at 50Hz (filter notch is 25Hz or 50Hz). PSRR exceeds 120dB at 60Hz (filter notch is 20Hz or 60Hz).
19. PSRR is decided by gain and power as follows

Gain	1	2	4	8~128
VDD=3V	86	78	85	93
VDD=5V	90	78	84	91

TIMING CHARACTERISTICS

Unless otherwise noted, VDD=2.7 to 5.25V, GND=0V; f_{CLKIN}=2.4576MHz,i

input logic low is 0V, input logic high is VDD.

Table 1. Timing Characteristic [1,2]

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Master Clock Frequency [3,4]	f_{CLKIN}		0.4		2.5	MHz
Master Clock Cycle	t_{CLKIN}		2500		400	ns
Master Clock Low Level Time	$t_{CLK\ LO}$		0.4×t_{CLKIN}			ns
Master Clock High Level Time	$t_{CLK\ HI}$		0.4×t_{CLKIN}			ns
CS High Level Time	t1			500×t_{CLKIN}		ns
RESET Pulse Width	t2		100			ns
Read Operation						
DRDY to CS Setup Time	t3		0			
CS Falling Edge to SCLK Rising Edge Setup Time	t4		120			ns
SCLK Falling Edge to Data Valid Delay [5]	t5	VDD=5V	0		80	ns
		VDD=3V	0		100	
SCLK High Pulse Width	t6		100			ns
SCLK Low Pulse Width	t7		100			ns
CS Rising Edge to SCLK Rising Edge Hold Time	t8		0			ns
Bus Release Time after SCLK Rising Edge [6]	t9	VDD=5V	10		60	ns
		VDD=3V	10		100	
SCLK Falling Edge to DRDY High Level [7]	t10				100	ns
Write Operation						
CS Falling Edge to SCLK Rising Edge Setup Time	t11		120			ns
Data Valid to SCLK Rising Edge Setup Time	t12		30			ns
Data Valid to SCLK Falling Edge Setup Time	t13		20			ns
SCLK High Pulse Width	t14		100			ns
SCLK Low Pulse Width	t15		100			ns
CS Rising Edge to SCLK Rising Edge Hold Time	t16		0			ns

1. Test at 25°C. All input signals meet: t_R=t_F =5ns (VDD 10%~90%), start timing from 1.6V.
2. See Figure 7 and Figure 8.
3. f_{CLKIN} duty cycle is 45%~55%. As long as the MS5213T is not in standby mode, f_{CLKIN} must be provided. If clock is not provided, the device would extract higher current more than rating value and may become uncalibrated.
4. When the MS5213T in manufacture test, use f_{CLKIN}=2.4576MHz (1MHz is used for some tests of I_{DD}) to ensure that device operates at 400kHz.
5. These values are measured in load shown in Figure 1. It is defined that the time required for output crossing V_{OL} or V_{OH}.
6. These values are measured when data output is 0.5V (load situation is shown in Figure 1). Then backstep by measured data to remove the effect of charging and discharging 50pF capacitor. It indicates all time values in parameter table are real bus release time and are independent of external load capacitors.
7. After result data is updated, DRDY returns high level after the first read. When DRDY is high level, read operation can be performed again. However, it is noted that following read operations couldn't too close to next update.

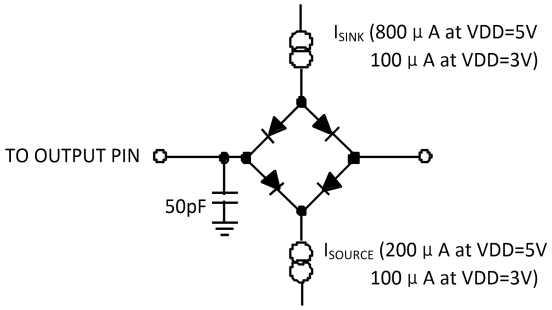


Figure 1. Load Circuit (excess time and bus release time)

OUTPUT NOISE

Table 2 and 4 show the output noise (RMS) of the MS5213T at the selectable notch and -3dB frequencies, selected by the clock registers FS0 and FS1. Data is at bipolar input, VREF=+2.5V/1.225, VDD=5V/3V. These values are typical values when the device operates in buffered or unbuffered mode and the analog input voltage is 0V.

Table 3 and Table 5 show the peak to peak output noise. Note that the resolution represented by these numbers is not code blinking. These values apply to the bipolar input range in buffered and unbuffered modes (VREF = + 2.5V / + 1.225). These values are typical and close to the nearest LSB. It's required that CLKDIV bit in clock register is set 0.

Table 2. Output Noise VS. Gain and Output Rate @ 5V

Filter Notch and Data Rate	-3dB Freq	Gain1	Gain2	Gain4	Gain8	Gain16	Gain32	Gain64	Gain128
MCLK IN = 2.4576MHz									
50Hz	13.1Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
60Hz	15.72Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
250Hz	65.5Hz	110	49	31	17	8	3.6	2.3	1.7
500Hz	131Hz	550	285	145	70	41	22	9.1	4.7
MCLK IN = 1MHz									
20Hz	5.24Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
25Hz	6.55Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
100Hz	26.2Hz	110	49	31	17	8	3.6	2.3	1.7
200Hz	52.4Hz	550	285	145	70	41	22	9.1	4.7

Table 3. Effective Bits VS. Gain and Output Rate @5V

Filter Notch and Data Rate	-3dB Freq	Gain1	Gain2	Gain4	Gain8	Gain16	Gain32	Gain64	Gain128
MCLK IN = 2.4576MHz									
50Hz	13.1Hz	16	16	16	16	16	16	15	14
60Hz	15.72Hz	16	16	16	16	15	14	14	13
250Hz	65.5Hz	13	13	13	13	13	13	12	12
500Hz	131Hz	10	10	10	10	10	10	10	10
MCLK IN = 1MHz									
20Hz	5.24Hz	16	16	16	16	16	16	15	14
25Hz	6.55Hz	16	16	16	16	15	14	14	13
100Hz	26.2Hz	13	13	13	13	13	13	12	12
200Hz	52.4Hz	10	10	10	10	10	10	10	10

Table 4. Output Noise VS. Gain and Output Rate @ 3V

Filter Notch and Data Rate	-3dB Freq	Gain1	Gain2	Gain4	Gain8	Gain16	Gain32	Gain64	Gain128
MCLK IN = 2.4576MHz									
50Hz	13.1Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
60Hz	15.72Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
250Hz	65.5Hz	50	25	14	9.9	5.1	2.6	2.3	2.0
500Hz	131Hz	270	135	65	41	22	9.7	5.1	3.3
MCLK IN = 1MHz									
20Hz	5.24Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
25Hz	6.55Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
100Hz	26.2Hz	50	25	14	9.9	5.1	2.6	2.3	2.0
200Hz	52.4Hz	270	135	65	41	22	9.7	5.1	3.3

Table 5. Effective Bits VS. Gain and Output Rate @3V

Filter Notch and Data Rate	-3dB Freq	Gain1	Gain2	Gain4	Gain8	Gain16	Gain32	Gain64	Gain128
MCLK IN = 2.4576MHz									
50Hz	13.1Hz	16	16	15	15	14	13	13	12
60Hz	15.72Hz	16	16	15	14	14	13	13	12
250Hz	65.5Hz	13	13	13	13	12	12	11	11
500Hz	131Hz	10	10	10	10	10	10	10	10
MCLK IN = 1MHz									
20Hz	5.24Hz	16	16	15	15	14	13	13	12
25Hz	6.55Hz	16	16	15	14	14	13	13	12
100Hz	26.2Hz	13	13	13	13	12	12	11	11
200Hz	52.4Hz	10	10	10	10	10	10	10	10

FUNCTIONAL DESCRIPTION

On-chip Register

The MS5213T contains eight on-chip registers, accessed via serial interface. The first register is communication register, managing channel selection to decide next operation is read or write, and which register is operated. All communications with device must start with writing to communication register. After power-up or reset, device wait for one write operation to communication register. The written data decides the next operation is read or write and which register is operated. Therefore, first write to communication register before write to any other registers. Before all registers (including communication register itself and output data register) perform read operation, must first write to communication register, then read selected register. In addition, communication register also controls wait mode and channel selection. And DRDY can be read from communication register.

The second register is setting register, deciding calibration mode, gain setting, unbipolar/bipolar input and buffer mode. The third register is clock register, including filter select bit and clock control bit.

The fourth register is data register. And output data is read from the register. Last register is calibration register, storing channel calibration data. Next would describe in detail.

Communication Register

(RS2,RS1,RS0=0,0,0)

Communication register is an 8-bit register, which can read and write data. The written data determines which register the next read or write occurs on. Once the next read or write operation is completed on the selected register, the interface would return to the communication register to receive a write operation. This is interface default state. After power on or reset, the MS5213T is in this default state, waiting for a write operation to the communication register. Under the condition of interface sequence loss, if write operation at DIN level persists for enough long time (at least 32 serial clock cycles), the MS5213T will go back to default state.

Table 6. Communication Register

BIT	7	6	5	4	3	2	1	0
NAME	0/DRDY(0)	RS2(0)	RS1(0)	RS0(0)	R/W(0)	STBY(0)	CH1(0)	CH0(0)

Note: The content in bracket is the default value of power on reset.

Table 7. Function Description of Each Bit in Communication Register

Register	Description
0/DRDY	To write to the communication register, a "0" must be written to this one. If "1" is written to this bit, subsequent bits will not be able to write to the register. It will stay in this bit until a "0" is written to it, and the next seven bits will be loaded into the communication register. For read operation, this bit provides DRDY flag of the device. The state of the bit is the same as the state of DRDY output pin.
RS2-RS0	Register Select Bit. These three bits choose which register to read / write next.
R/W	Read / Write Selection. "0" indicates that the next operation is write, and "1" indicates that the next operation is read.
STBY	Standby Mode. If "1" is written to this bit, it is in wait or power down mode. In this mode, the power supply current consumed by the device is only 10μA. In standby mode, the device will maintain its calibration coefficient and control word information. Write "0" and the device is in normal operation mode.

Register	Description
CH1, CH0	Channel Selection. These two bits select a channel for data conversion or access calibration coefficient, as shown in Table 9. Three pairs of calibration registers in the device are used to store the calibration coefficients. Table 9 indicates which channel combinations have independent calibration coefficients. When CH1 is logic 1 and CH0 is logic 0, AIN (-) input pin of the MS5213T is shorted to itself. This can be used as a test method to evaluate the noise performance (without external noise source). In this mode, the AIN1 (-) /COMMON input terminal must be connected to an external voltage and within the allowable common-mode voltage range.

Table 8. Register Selection

RS2	RS1	RS0	Register	Register bits
0	0	0	Communication Register	8bits
0	0	1	Setting Register	8bits
0	1	0	Clock Register	8bits
0	1	1	Data Register	16bits
1	0	0	Test Register	8bits
1	0	1	None	
1	1	0	Offset Register	24bits
1	1	1	Gain Register	24bits

Table 9. MS5213T Input Channel Selection

CH1	CH0	AIN (+)	AIN (-)	Calibration Register Pair
0	0	AIN1(+)	AIN1(-)	Calibration Register Pair 0
0	1	AIN2(+)	AIN2(-)	Calibration Register Pair 1
1	0	AIN1(-)	AIN1(-)	Calibration Register Pair 0
1	1	AIN1(-)	AIN2(-)	Calibration Register Pair 2

Setting Register

(RS2,RS1,RS0=0,0,1); Power On / Reset Status: 01Hex

The setting register is an 8-bit register, which can read and write data.

Table 10. Setting Register

BIT	7	6	5	4	3	2	1	0
NAME	MD1(0)	MD0(0)	G2(0)	G1(0)	G0(0)	B/U(0)	BUF(0)	FSYNC(1)

Table 11. Function Description of Each Bit in Setting Register

Register	Description
MD1, MD0	MSC Operation Mode Control. These two bits control the operation mode of MSC, as shown in Table 12.
G2-G0	Gain Select Bit. These three bits control the gain of on-chip PGA , as shown in Table 13.
B/U	Bipolar / Unipolar Control. "0" indicates bipolar operation and "1" indicates unipolar operation.
BUF	Buffer Control. This bit is "0", the on-chip buffer is short, and VDD consumption current is reduced. When this bit is "1", the on-chip buffer is connected with analog input, and it can connect to input source with higher impedance .
FSYNC	Filter Synchronization. At high level, the node of digital filter, filter control logic and calibration control logic are in reset state, and the analog modulator is also controlled in reset state. At low level, modulator and filter begin to process data and produce a valid word within 3×(1/output rate) time (i.e. filter setup time). Fsync doesn't affect digital interface and reset the DRDY output(if it is low).

Table 12. Operation Mode Selection

MD1	MD0	Operation Mode
0	0	Normal Mode. In this mode, converter performs normal analog-to-digital conversion.
0	1	Self Calibration. Self calibration is activated on the channels selected by CH1 and CH2 in the communication register. This is a step calibration. After completing this task, it returns to normal mode, that is, MD1 and MD0 are 0. At the beginning of calibration, the DRDY output pin or DRDY bit is high level and returns to low level after self calibration. At this time, a new valid word is generated in the data register. The zero-scale calibration is short-circuit in input terminal internally (zero input), and the full-scale calibration is performed at the selected gain and internally generated VREF / selected gain conditions.
1	0	Zero-scale System Calibration. Activate zero-scale system calibration on the channel selected by CH1 and CH2 in the communication register. When this calibration sequence is used, the input voltage on the analog input is calibrated at the selected gain. During calibration, the input voltage should be stable. At the beginning of calibration, DRDY output or the DRDY bit is high, and zero-scale system returns to low level after the calibration is completed. At this time, a new valid word is generated in the data register. At the end of calibration, the device returns to normal mode, that is, MD1 and MD0 are 0.
1	1	Full-scale System Calibration. Activates full-scale system calibration on the selected input channel. In this calibration sequence, the input voltage on the analog input terminal completes the calibration at the selected gain. The input voltage should be stable during calibration. At the beginning of calibration, DRDY output or DRDY bit is high level, and after the full-scale system calibration is completed, it returns to low level. At this time, a new valid word is generated in the data register. At the end of calibration, the device returns to normal mode, that is, MD1 and MD0 are 0.

Table 13. Gain Selection

G2	G1	G0	Gain Selection
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Clock Register

(RS2,RS1,RS0 = 0,1,0; Power On / Reset Status: 05Hex

The clock register is an 8-bit read / write register.

Table 14. Clock Register

BIT	7	6	5	4	3	2	1	0
NAME	ZERO(0)	ZERO(0)	ZERO(0)	CLKDIS(0)	CLKDIV(0)	CLK(1)	FS1(0)	FS0(0)

Table 15. Function Description of Each Bit in Clock Register

Register	Description
ZERO	Write 0. Must write 0 to these bits to ensure the correct operation. Otherwise, result in unspecified operation.
CLKDIS	Master Clock Inhibit Bit. Logic "1" indicates the master clock outputting on from MCLK OUT pin. When prohibited, MCLK OUT output pin is at low level. This feature enables users to flexibly use MCLK OUT pin. For example, MCLK OUT can be used as the clock source of other devices in the system, and MCLK OUT can be turned off, so that the device has the power saving performance. When an external master clock is connected to MCLK IN, the MS5213T keeps the internal clock and performs normal conversion when CLKDIS bit is valid. When a crystal oscillator or a ceramic resonator is connected between MCLK IN and MCLK OUT, so when the CLKDIS bits are valid, the MS5213T clock will stop and no analog-to-digital conversion will be performed.
CLKDIV	Clock Divider Bit. When set to logic 1, the clock frequency on the MCLK IN pin is divided by 2 before used by the MS5213T. For example, set CLKDIV to logic 1, and users can use one 4.9152MHz crystal between MCLK IN and MCLK OU. However, perform operation with specified 2.4576MHz in internal device. When set CLKDIV to logic 0, the frequency on MCLK IN pin is actually the internal frequency.
CLK	Clock Bit. CLK bit should be set according to operation frequency of the MS5213T. If master clock frequency of converter is 2.4576MHz (CLKDIV=0) or 4.9152MHz (CLKDIV=1), CLK should be set "1". If master clock frequency of the device is 1MHz (CLKDIV= 0) or 2MHz (CLKDIV= 1), this bit should be set "0". This bit sets appropriate scale current for given operation frequency and also selects the output update rate of the device (along with FS1 and FS0). If CLK doesn't set correctly according to master clock frequency, the MS5213T will not be able to achieve the target.

FS1,FS0	Filter Select Bit, which together with CLK determine the output update rate of the device. Table 16 shows the first notch and - 3dB frequency of the filter. On-chip digital filter generates sinc3 (or (sinx/x)3) filter response. Along with gain select, it also determines the output noise. The change of filter notch and selected gain would have effect on resolution. Table 2 and Table 5 show the filter notch frequency and gain VS. output noise and resolution. The output data rate (or valid conversion time) is equal to the selected frequency of first notch. For example, if the first notch is selected in 50Hz, the output rate of each word is 50Hz, that is, output one new word every 2ms. When these bits are changed, one calibration must be performed. In worst condition, the settle time of filter, reaching full-scale stepping input, is 4×(1/Output data rate). For example, the first notch is in 50Hz, and the settle time of filter is 80ms (max) for reaching full-scale input. If the first notch is in 500Hz, the settle time is 8ms (max). According to the synchronous stepping input, the settle time could be reduced to 3×(1/Output data rate). In other words, if stepping input occurs when FSYNC bit is high, it needs 3×(1/Output data rate) to settle after FSYNC bit returns to low. -3dB frequency depends on the programmable first notch frequency,according to the equation below: Filter -3dB frequency=0.262×first notch frequency.

Table 16. Output Rate Selection

CLK[1]	FS1	FS0	Output Rate	-3dB Cut-off Frequency of Filter
0	0	0	20 Hz	5.24 Hz
0	0	1	25 Hz	6.55 Hz
0	1	0	100 Hz	26.2 Hz
0	1	1	200 Hz	52.4 Hz
1	0	0	50 Hz	13.1 Hz
1	0	1	60 Hz	15.7 Hz
1	1	0	250 Hz	65.5 Hz
1	1	1	500 Hz	131 Hz

Note 1: Assuming that the clock frequency of MCLK IN is correct, the setting of CLKDIV bit is also appropriate.

Data Register

(RS2,RS1,RS0 = 0,1,1)

Data register is a 16-bit read-only register, which contains the latest conversion results from the MS5213T. If communication register sets device to write to the register, must perform one write operation to make device return the state, ready to perform write operation to communication register. But the written 16-bit data would be ignored by the MS5213T.

Test Register

(RS2,RS1,RS0 = 1,0,0);Power On / Reset Status: 00Hex

Test register is used to test device. It is suggested that user should not change the default value of any bit in the test register.

Zero-Scale Calibration Register

(RS2,RS1,RS0 = 1,1,0);Power On / Reset Status: 1F4000Hex

The MS5213T contains several independent zero-scale registers, each of which is responsible for one input channel. They are all 24-bit read/write registers. 24-bit data must be written before it can be transferred to the zero-scale calibration register. Zero-scale register is used together with full-scale register and form one register pair. And each pair responds to one pair of channel, see Table 9.

When device is set to allow access to these registers via digital interface, device itself doesn't access register coefficient in order to make output data correct scale. Therefore, after accessing to calibration register (whether read or write operation), the first output data read from device may contain uncorrected data. In addition, during data calibration, calibration register can't perform write operation. This type of events could be avoided by following method: Before calibration register starts operation, FSYNC bit in the mode register would be set as high level. After task is finished, FSYNC bit is set as low level.

Full-Scale Calibration Register

(RS2,RS1,RS0 = 1,1,1); Power on / Reset Status: 5761ABHex

The MS5213T contains several independent full-scale registers, each of which is responsible for one input channel. They are all 24-bit read / write registers. 24-bit data must be written before it can be transferred to the full-scale calibration register. Full-scale register is used together with zero-scale register and form one register pair. And each pair responds to one pair of channel, see Table 9.

When device is set to allow access to these registers via digital interface, device itself doesn't access register coefficient in order to make output data correct scale. Therefore, after accessing to calibration register (whether read or write operation), the first output data read from device may contain uncorrected data. In addition, during data calibration, calibration register can't perform write operation. This type of events could be avoided by following method: Before calibration register starts operation, FSYNC bit in the mode register would be set as high level. After task is finished, FSYNC bit is set as low level.

Calibration Process

Table 17 summarizes these calibration types, operation contents and operation time. There are two ways to judge whether the calibration is over. The first method is to monitor DRDY. If DRDY returns to low level, it indicates that the calibration process has finished and that there is a new valid data in the data register. The second method is to monitor MD1 and MD0 bits in the setting register. If MD1 and MD0 return to "0" (after calibration, MD1 and MD0 return to "0"), it indicates that the calibration process has finished. This method can not prompt whether there is a new conversion result in the data register, but it's earlier than the first judgment method in time, that is, that is, it can quickly know whether the calibration has finished. The duration time when Mode bits (i.e. MD1, MD0) return to "0" is shown in Table 17. The process of DRDY returning to low level includes a normal conversion time and a delay time tp with correct scale for the first conversion result. tp shall not exceed 2000×tCLKIN. The time required for these two methods is shown in the table below.

Table 17. Calibration Process

Calibration Type	MD1,MD0	Calibration Sequence	Setting Time	DRDY Setting Time
Self Calibration	0,1	Zero-scale Calibration@ Selected Gain+Full-scale Calibration @Selected Gain	6×1/Output Rate	9×1/Output Rate+tP
Zero-scale Calibration	1,0	Zero-scale Calibration @Selected Gain	3×1/Output Rate	4×1/Output Rate+tP
Full-Scale Calibration	1,1,	Full-scale Calibration @Selected Gain	3×1/Output Rate	1×1/Output Rate+tP

Analog Input Range

In non-buffered mode, the common-mode input range is from GND to VDD. The absolute value of analog input voltage is between GND-30mV and VDD+30mV. In non-buffer mode, the analog input connects directly to a 7pF sampling capacitor, C_{SAMP}. As a result, the analog input connects a dynamic load that is converted at the input sampling rate. The typical value of the effective on-off resistance (R_{SW}) of the switch is 7kΩ. Table 18 lists the allowable external resistance/capacitance values in non-buffer mode.

Table 18. External Resistance and Capacitance Values without 16-Bit Gain Error (Non-buffer Mode)

Gain	External Capacitance (pF)					
	10	50	100	500	1000	5000
1	152kΩ	53.9kΩ	31.4kΩ	8.4kΩ	4.76kΩ	1.36kΩ
2	75.1kΩ	26.6kΩ	15.4kΩ	4.14kΩ	2.36kΩ	670Ω
4	34.2kΩ	12.77kΩ	7.3kΩ	1.95kΩ	1.15kΩ	320Ω
8~128	16.7kΩ	5.95kΩ	3.46kΩ	924Ω	526Ω	150Ω

Sample Rate

The sample frequency of the MS5213T modulator maintains at fCLKIN/128 (fCLKIN=2.4576MHz at 19.2kHz), regardless of the selected gain. However, gain greater than 1 is a combination of multiple input sampling in each modulator cycle and the ratio of the reference capacitance to the input capacitance. So the input sample rate varies with the selected gain (see Table 19).

Table 19. Relationship between Input Sample Frequency and Gain

Gain	Input Sample Frequency(fs)
1	$f_{CLKIN}/64$(38.4kHz@f_{CLKIN}=2.4576MHz)
2	$2\times f_{CLKIN}/64$(76.8kHz@f_{CLKIN}=2.4576MHz)
4	$4\times f_{CLKIN}/64$(153.6kHz@f_{CLKIN}=2.4576MHz)
8~128	$8\times f_{CLKIN}/64$(307.2kHz@f_{CLKIN}=2.4576MHz)

Digital Interface

The serial interface of MS5213T includes five signals: CS, SCLK, DIN, DOUT and DRDY. DIN line is used to transmit data to on-chip registers, while DOUT line is used to access data in registers. SCLK is serial clock input. All data transmissions are related to SCLK signal. The DRDY acts as status signal to indicate when the data is ready to read from registers. DRDY becomes low when there are new data words in the output register. If DRDY becomes high before the output register data is updated, it is prompted not to read the data at this time to avoid reading data during the register update process. CS is used to select devices.

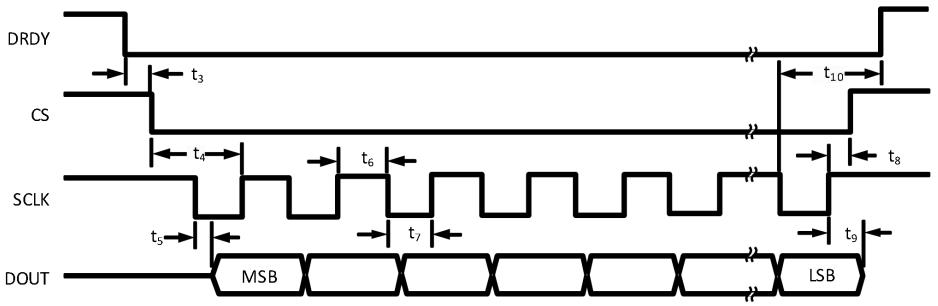


Figure 1. Read Cycle Timing Diagram

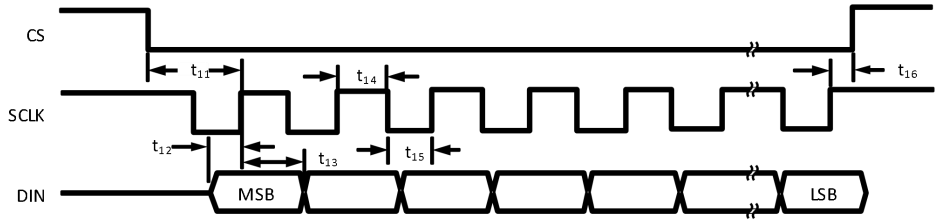
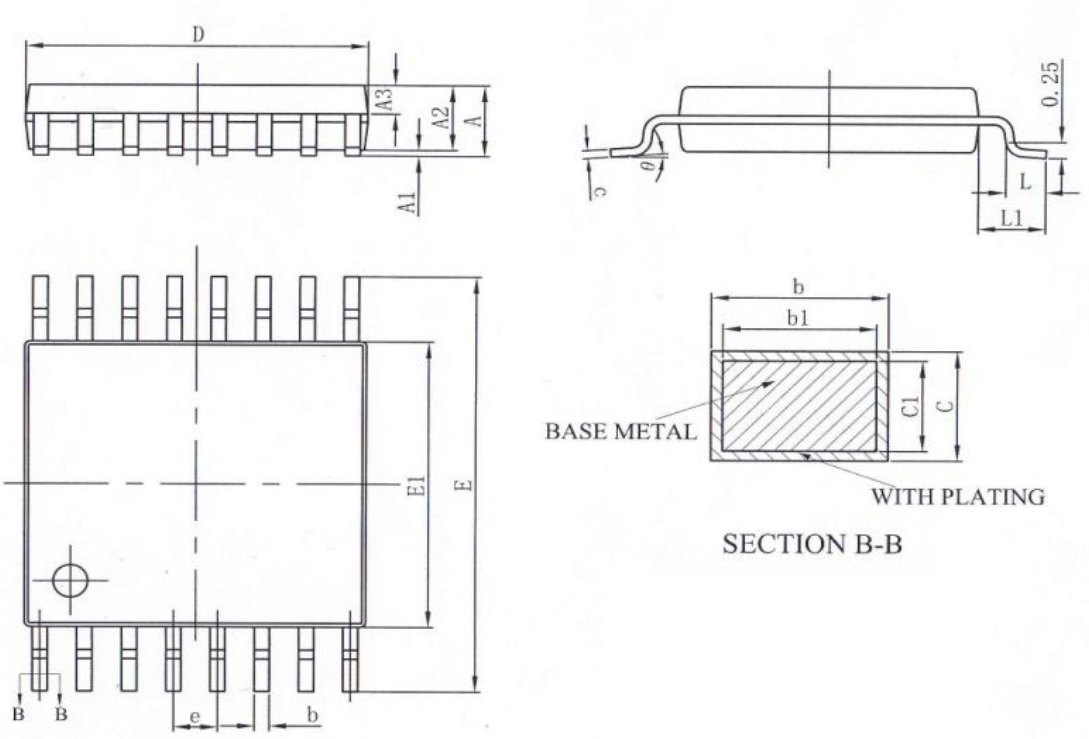


Figure 2. Writing Cycle Sequence Diagram

PACKAGE OUTLINE DIMENSIONS

TSSOP16



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	--	0.28
b1	0.19	0.22	0.25
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	--	8°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name : MS5213T

Product Code : XXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5213T	TSSOP16	3000	1	3000	8	24000

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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