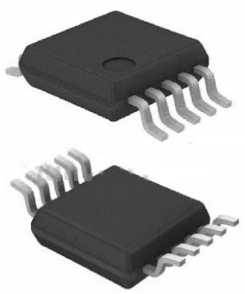
2.7V to 5.5V, 12Bit Dual DAC

PRODUCT DESCRIPTION

The MS5612M is a 12bit two-channel output voltage DAC. The interface uses three-wire serial port mode, and it can be compatible with TMS320, SPI, QSPI and Microwire serial ports. The MS5612M has 16bit control data, including control byte and 12bit DAC data. The power supply range is 2.7V to 5.5V. The output of integrated resistor string is connected to a class AB rail-to-rail buffer with 6dB gain. The output buffer improves stability and reduces the setup time.

The MS5612M is available in a 10-pin MSOP package.



MSOP10

FEATURES

- 12bit Resolution
- Programmable Setup Time: 3μs or 9μs
- Compatible with TMS320, SPI, QSPI and Microwire Interfaces
- Internal Power on Reset
- Low Power Dissipation: 8mW at 5V, 3.6mW at 3V
- Integrated REF Buffer
- Output Range: Twice the Reference Voltage
- Not Sensitive to Temperature
- Software, Hardware Power down
- Power Supply: 2.7V~5.5V

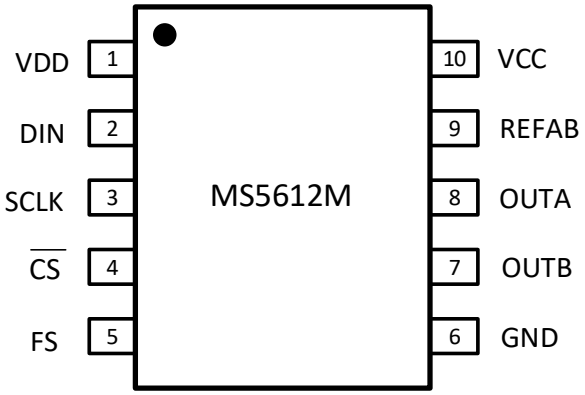
APPLICATIONS

- Digital Servo System Control
- Digital Compensation and Gain Adjustment
- Industrial Process Control
- Mechanical and Mobile Control Equipment
- High Capacity Storage Device

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5612M	MSOP10	MS5612M

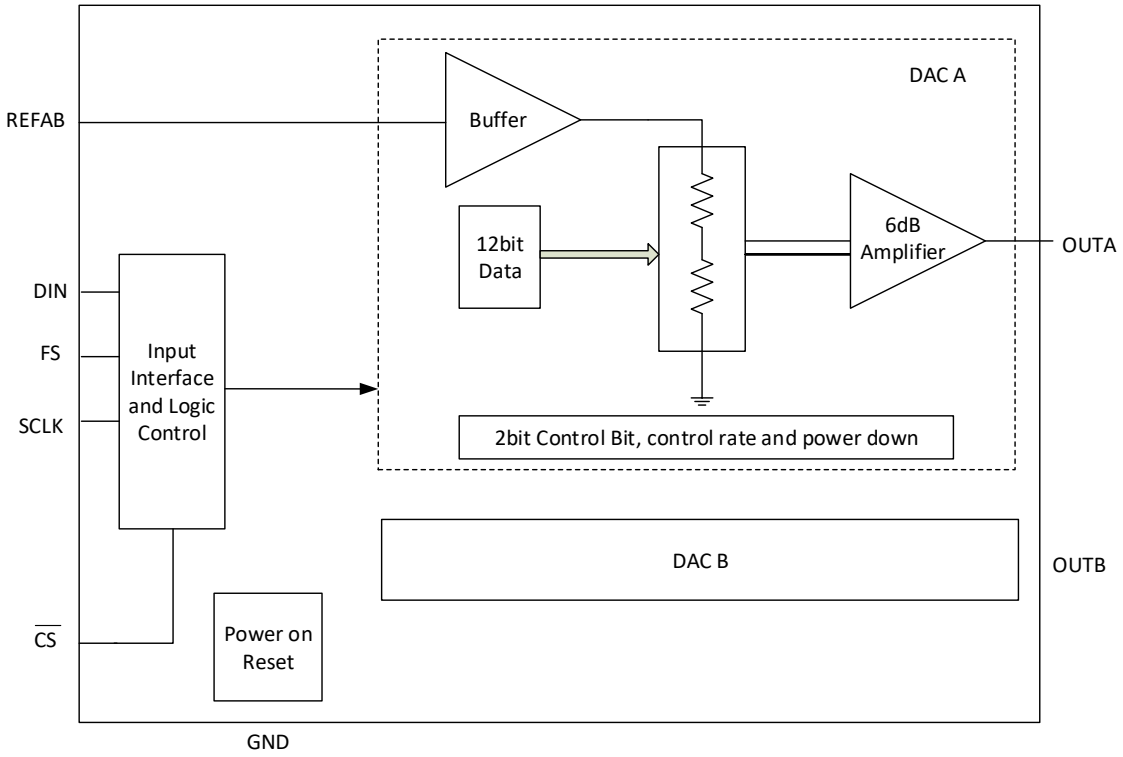
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	VDD	-	Digital Power Supply
2	DIN	I	Serial Data Input
3	SCLK	I	Serial Digital Clock Input
4	$\overline{CS}$	I	Chip Select, Active Low
5	FS	I	Frame Synchronization Input Signal
6	GND	-	Ground
7	OUTB	O	Analog Output for Channel B
8	OUTA	O	Analog Output for Channel A
9	REFAB	I	Reference Input Voltage for Channel A and B
10	VCC	-	Analog Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	-0.3 ~ +7	V
Power Supply	V_{CC}	-0.3 ~ +7	V
Digital Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V
Reference Input Voltage	V_{REFIN}	-0.3 ~ V_{CC}+0.3	V
Operating Temperature	T_A	-40 ~ +105	°C
Storage Temperature	T_{STG}	-60 ~ +150	°C
Maximum Junction Temperature	T_{JMAX}	150	°C
Lead Temperature(10s)	T_{SOLDER}	260	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Condition	Min	Typ	Max	Unit
Power Supply (V_{DD},V_{CC})	5V Supply	4.5	5	5.5	V
	3V Supply	2.7	3	3.3	
Digital Input High(V_{IH})	V_{DD}＝2.7V	2			V
	V_{DD}＝5.5V	2.4			
Digital Input Low(V_{IL})	V_{DD}＝2.7V			0.6	V
	V_{DD}＝5.5V			1	
Reference Voltage (V_{REF})	5V Supply (Note 1)	0	2.048	V_{CC}-1.5	V
	3V Supply (Note 1)	0	1.024	V_{CC}-1.5	
Load Resistance		2	10		kΩ
Load Capacitance				100	pF
SCLK Rate				20	MHz

Note 1: The input voltage more than V_{CC}/2 will result in saturated output at large DAC input codes.

ELECTRICAL CHARACTERISTICS

Static DAC

Parameter		Condition	Min	Typ	Max	Unit
Resolution			12			Bits
Integral Non-linearity(INL)		See Note 1		±1.5	±4	LSB
Differential Non-linearity(DNL)		See Note 2		±1	±4	LSB
Zero Scale Offset		See Note 3			±12	mV
Zero Scale Offset Temperature Drift		See Note 4		10		ppm/°C
Gain Error		See Note 5			±0.6	%of FS Voltage
Gain Error Temperature Drift		See Note 6		10		ppm/°C
PSRR	Zero Scale	See Note 7 and 8		-80		dB
	Full Scale			-80		dB

Note:

1. Integrated non-linearity (INL) refers to linearity error, which is the maximum deviation of the output from the ideal output by eliminating zero and full scale errors.
2. Differential non-linearity (DNL), differential error, refers to maximum amplitude change adjacent to LSB.
3. Zero scale offset refers to the analog output of zero digital input.
4. Zero scale temperature drift refers to change of analog output with temperature when digital input is zero.
5. Gain error refers to deviation between analog output and ideal output after zero scale offset is removed.
6. Gain error temperature drift refers to the variation of the deviation between analog output and ideal output with temperature after zero scale offset is removed.
7. Zero scale power supply rejection ratio refers to the ratio of change in output caused by a change in VDD of 5±0.5 V and 3±0.3 V when the digital input is zero.
8. Full scale power supply rejection ratio refers to the ratio of change in output caused by a change in VDD of 5±0.5 V and 3±0.3 V when the digital input is high.

DAC Output

Parameter	Condition	Min	Typ	Max	Unit
Output Voltage	R_L=10kΩ	0		V_{CC}-0.4	V
Output Load Adjustment Resolution	R_L=2kΩ to 10kΩ		0.1	0.25	%of FS

Reference Input Voltage

Parameter	Condition		Min	Typ	Max	Unit
Input Voltage	See Note 9		0		V_{CC}-1.5	V
Input Resistance				10		MΩ
Input Capacitance				5		pF
Reference Feedthrough	V_{REFIN} = 1Vpp(1 kHz)+ 1.024V (See Note 10)			-75		dB
Reference Input Bandwidth	V_{REFIN} = 0.2Vpp+ 1.024 V (Large Signal)	Slow		0.5		MHz
		Fast		1		

Note:

9. Reference input voltage more than VCC/2 will cause output saturation distortion.

10. Reference feedthrough refers to the analog output rejection ratio when the output is zero and V_{REFIN}= 1Vpp(1 kHz)+1.024V.

Digital Input

Parameter	Condition	Min	Typ	Max	Unit
Digital Input High-level Current	$V_I=V_{DD}$			±1	μA
Digital Input Low-level Current	V_I=0V			±1	μA
Input Capacitance			3		pF

Power Dissipation

Parameter	Condition		Min	Typ	Max	Unit
Power Supply Current	5V supply, no load, add CLOCK, all inputs 0V or VDD	Slow		1.6	2.4	mA
		Fast		3.8	5.6	
	3V supply, no load, add CLOCK, all inputs 0V or VDD	Slow		1.2	1.6	mA
		Fast		3.2	4.8	
Power Down Current				10		nA

Analog Output Dynamic

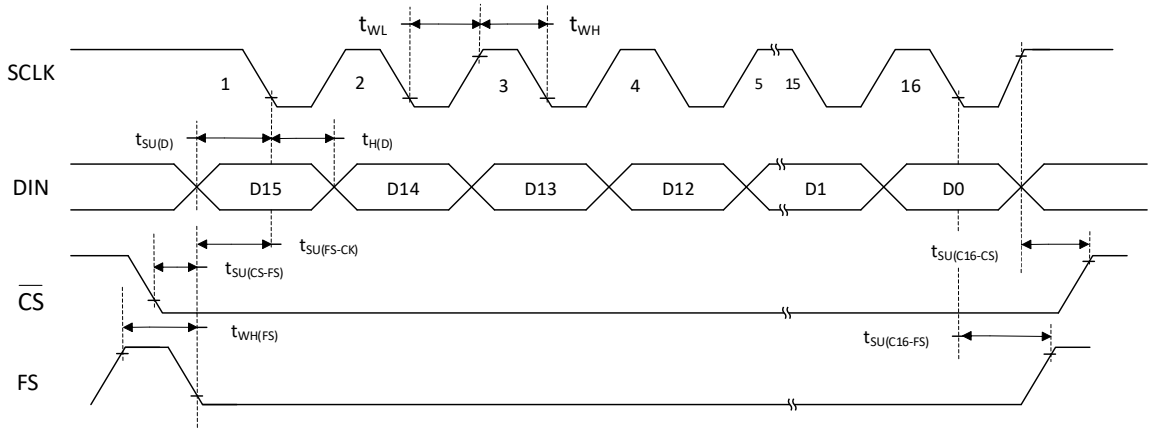
Parameter	Condition		Min	Typ	Max	Unit
SR	C_L=100pF, R_L=10kΩ, V_O=10% to 90%, V_{REF}=2.048,1.024	Fast		5		V/μs
		Slow		1		
t_S	To ±0.5LSB, C_L=100pF, R_L=10kΩ	Fast		3	5.5	μs
		Slow		9	20	
$t_{S(C)}$	To ±0.5LSB, C_L=100pF, R_L=10kΩ	Fast		1		μs
		Slow		2		
Glitch Energy	From 7FF to 800			10		nV-sec
SNR	V_{REF}=1.024 at 3V; V_{REF}=2.048 at 5V, f_S=400kSPS, f_{OUT}=1.1kHz sine wave, C_L=100pF, R_L=10kΩ, BW=20kHz			74		dB
S/(N+D)				66		
THD				-68		
SFDR				70		

Digital Input Timing

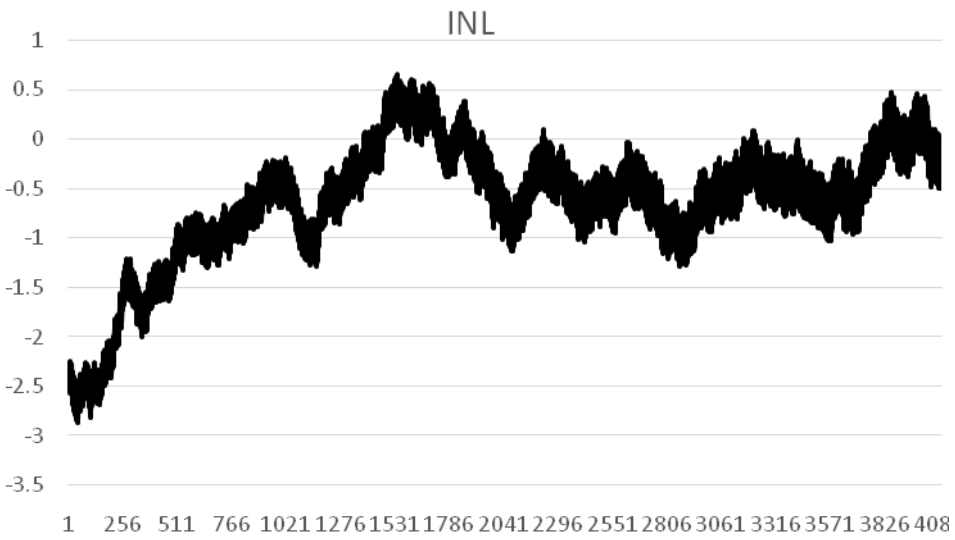
Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ Low to FS Falling Edge	$t_{SU(CS–FS)}$	10			ns
Setup time, FS to the first SCLK Falling Edge	$t_{SU(FS–CK)}$	8			ns
Setup time, the sixteenth SCLK falling edge after FS low on which bit D0 is sampled before rising edge of FS	$t_{SU(C16–FS)\ OF\ FS}$	10			ns

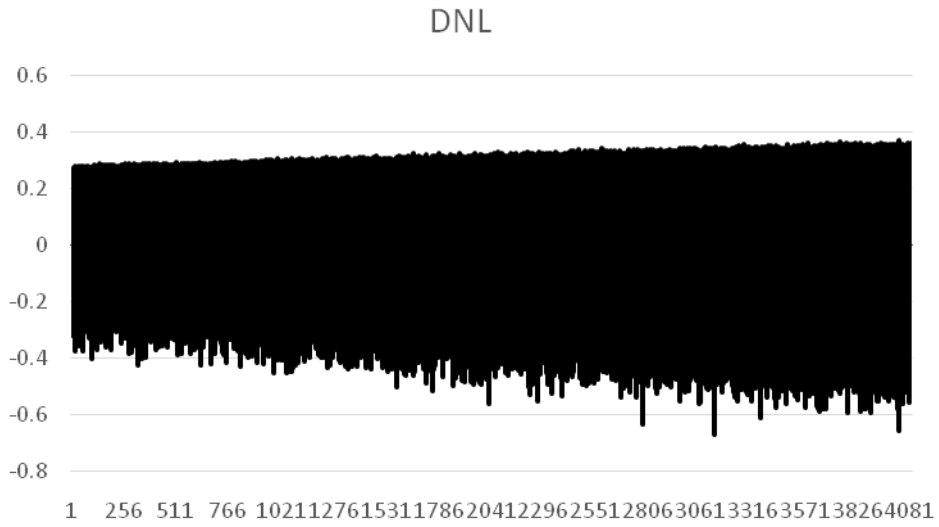
Parameter	Symbol	Min	Typ	Max	Unit
Setup time, next SCLK rising edge to $\overline{CS}$ high after the sixteenth SCLK of sampled D0	$t_{SU(C16–CS)}$	10			ns
SCLK high-level duration	t_{WH}	25			ns
SCLK low-level duration	t_{WL}	25			ns
Setup time, data ready before SCLK falling edge	$t_{SU(D)}$	8			ns
Hold time, data held valid after SCLK falling edge	$t_{H(D)}$	5			ns
FS high-level duration	$t_{WH(FS)}$	20			ns

Timing Diagram



TYPICAL CURVES





APPLICATION DESCRIPTION

The MS5612M is a 12-bit single-power digital-to-analog converter. Its architecture uses resistance array structure. It integrates serial interface, rate and power down logic control, reference input buffer, resistor string and output rail-to-rail amplifier.

The output voltage can be expressed as:

$$V_{OUT}=2\times\frac{V_{REF}\times D}{2^{12}}$$

Serial Interface

The MS5612M starts to input data bit-per-bit at the FS falling edge(active high at first). After 16 bits have been transferred or when FS becomes high, the internal DAC updates the corresponding output level.

Data Format

The data word of the MS5612M consists of two parts: control bits (D15~D12) and data bits(D11~D0).

MSB LSB

A1	A0	PWR	SPD	D11~D0

Data Bits

PWR: Power dissipation control, 1 for off mode, 0 for normal mode;

SPD: Rate control, 1 for fast mode, 0 for slow mode;

A1, A0 are the address selection bits of the internal DAC channels, the truth table is as follows:

A1	A0	DAC Address
0	0	DAC-A
0	1	DAC-B

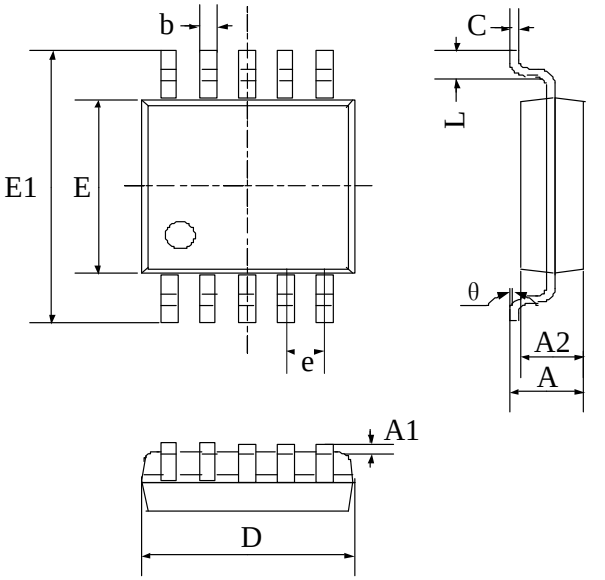
Power Supply Bypassing and Ground Management

In order to improve system performance, the analog and digital ground should be connected to different ground planes, which are linked together at low impedance node. It's better to connect the DAC AGND to system analog ground. Thus the current of analog ground is managed well , and the voltage drop on traces of analog ground could be ignored.

The 0.1μF ceramic decoupling capacitance should be connected between power supply and ground. And it is placed as near to the chip as possible. If magnet ring is used, the analog and digital power supply could be further separated.

PACKAGE OUTLINE DIMENSIONS

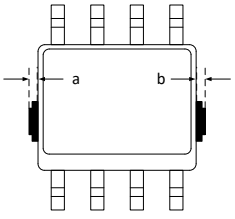
MSOP10



Symbol	Dimensions In Millimeters	
	Min	Max
A	0.800	1.200
A1	0.000	0.200
A2	0.760	0.970
b	0.30 TYP	
c	0.152 TYP	
D	2.900	3.100
e	0.50 TYP	
E	2.900	3.100
E1	4.700	5.100
L	0.410	0.650
θ	0°	6°

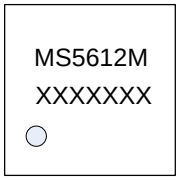
Note: In addition to the package size, a and b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.



MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name : MS5612M

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS5612M	MSOP10	3000	1	3000	8	24000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com