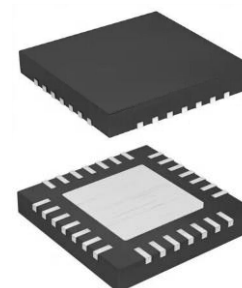


24bit, 192kHz Dual Channel Differential Digital to Analog Converter

PRODUCT DESCRIPTION

The MS5282N is a stereo digital-to-analog converter, which contains interpolation filter, a multi-bit modulator, differential output analog filter. The MS5282N supports most of audio data formats. It is based on a fourth order multi-bit Δ - Σ modulator with linear analog low pass filter. The MS5282N can automatically adjust the sample rate from 2kHz and 200kHz by detecting signal frequency and master clock frequency. The MS5282N can operate at 3.3V and 5V. These features make it ideal for wireless devices such as DVD player, decoders and digital communication devices.

The MS5282N is available in QFN28 package.



QFN28

FEATURES

- Multi-bit Δ - Σ Modulator
- 24bit D/A Converter
- Dual Channel
- Automatic Detection of Signal Frequencies up to 192kHz
- DR: 110dB
- THD: 0.003%
- Low Clock Jitter Sensitivity
- Operating Voltage : 3.3V or 5V
- Linear Filtering Output
- QFN28 Package

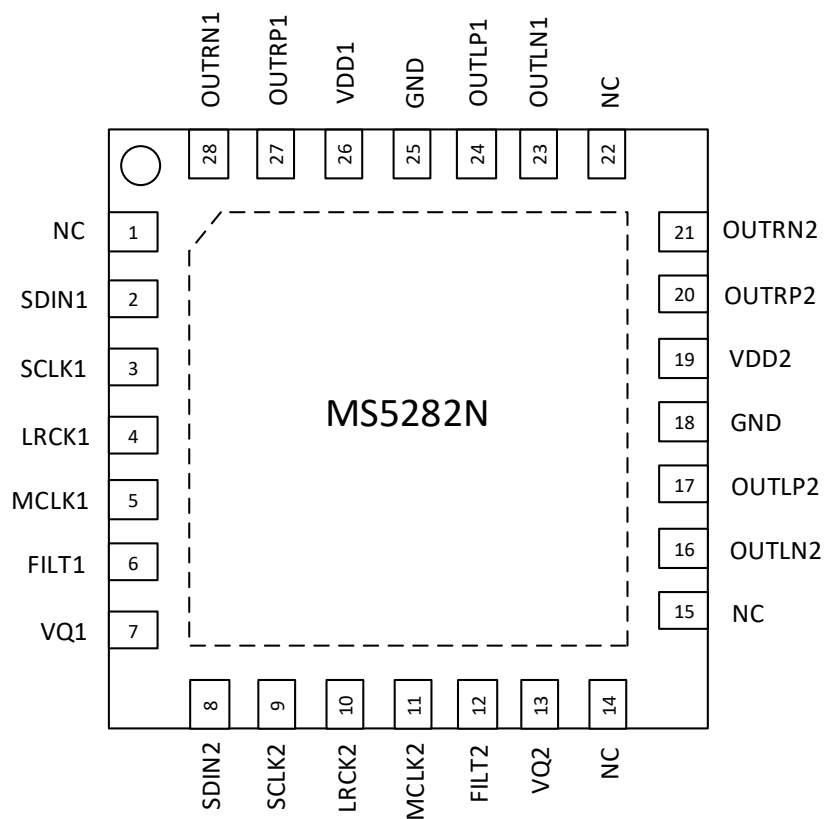
APPLICATIONS

- Digital Communication Device
- Car Audio System
- DVD Audio System

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5282N	QFN28	MS5282N

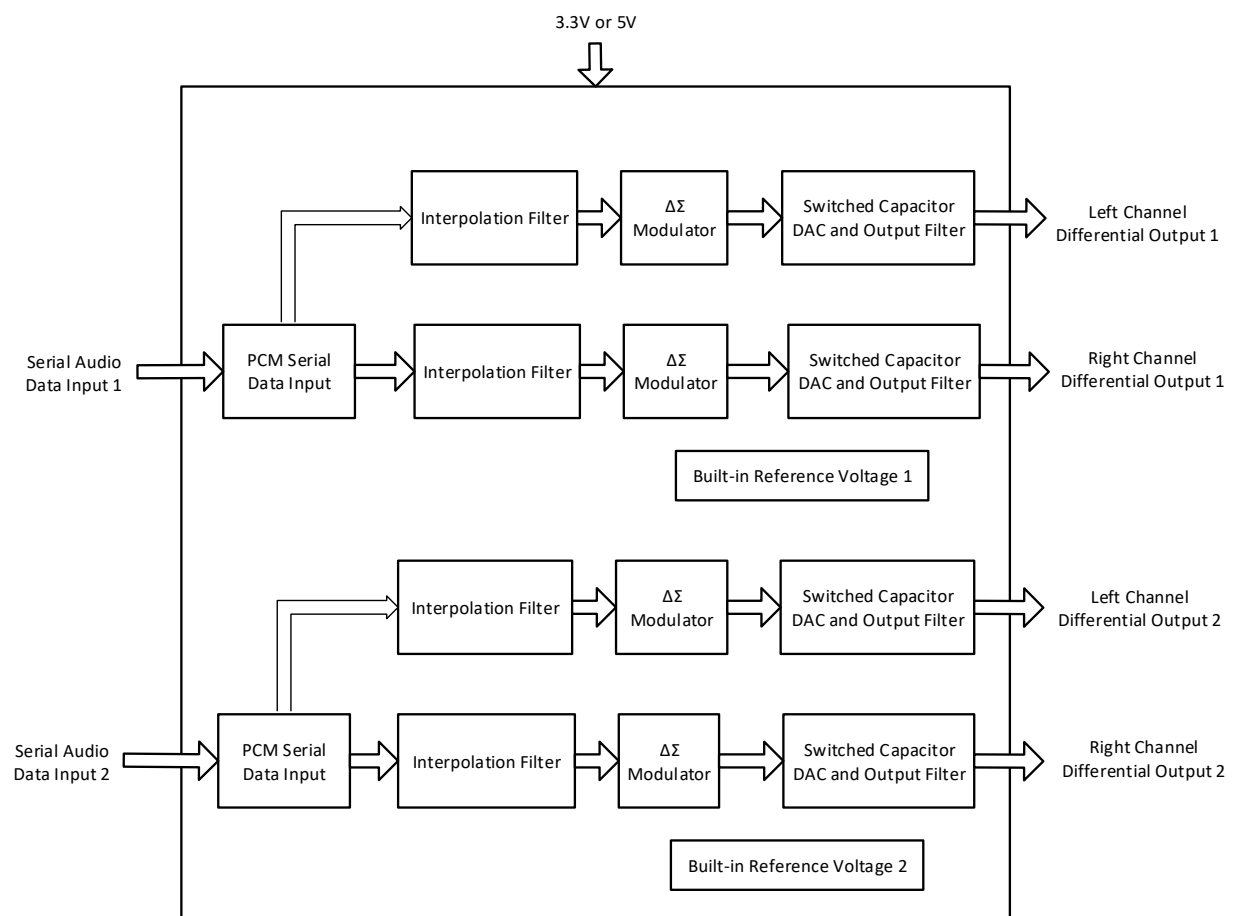
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1,14,15,22	NC	-	Not Connection
2	SDIN1	I	Serial Audio Data Input for Channel 1
3	SCLK1	I	External Serial Clock Input for Channel 1
4	LRCK1	I	Left/Right Clock for Channel 1
5	MCLK1	I	Master Clock for Channel 1
6	FILT1	IO	Positive Reference Voltage for Channel 1
7	VQ1	IO	DC Voltage for Channel 1
8	SDIN2	I	Serial Audio Data Input for Channel 2
9	SCLK2	I	External Serial Clock Input for Channel 2
10	LRCK2	I	Left/Right Clock for Channel 2
11	MCLK2	I	Master Clock for Channel 2
12	FILT2	IO	Positive Reference Voltage for Channel 2
13	VQ2	IO	DC Voltage for Channel 2
16	OUTLN2	O	Left Channel Analog Negative Output for Channel 2
17	OUTLP2	O	Left Channel Analog Positive Output for Channel 2
18	GND	-	Ground for Channel 2
19	VDD2	-	Analog Power Supply for Channel 2
20	OUTRP2	O	Right Channel Analog Positive Output for Channel 2
21	OUTRN2	O	Right Channel Analog Negative Output for Channel 2
23	OUTLN1	O	Left Channel Analog Negative Output for Channel 1
24	OUTLP1	O	Left Channel Analog Positive Output for Channel 1
25	GND	-	Ground for Channel 1
26	VDD1	-	Analog Power Supply for Channel 1
27	OUTRP1	O	Right Channel Analog Positive Output for Channel 1
28	OUTRN1	O	Right Channel Analog Negative Output for Channel 1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	V_{DD1}, V_{DD2}	-0.3 ~ 7	V
Input Current	I_{in}	-10 ~ +10	μA
Digital Input Voltage	V_{IND}	-0.3~ $V_{DD}+0.3$	V
Operating Temperature	T_A	-55 ~ 125	$^{\circ}C$
Storage Temperature	T_{STG}	-65 ~ 150	$^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Range			Unit
		Min	Tyo	Max	
Power Supply	V_{DD1}, V_{DD2}	3.0		5.5	V
Operating Temperature	T_A	-40		+85	$^{\circ}C$

ELECTRICAL CHARACTERISTICS

DAC Analog Characteristics

TA=25°C, Full-scale output sinusoidal signal, 997Hz, Fs=48/96/192kHz;

RL = 3kΩ, CL = 10pF, Test bandwidth 10 Hz to 20kHz.

Parameter			3.3V			Unit
			Min	Typ	Max	
Dynamic Performance						
Dynamic Range	24 bit	A-weighted	100	102		dB
Total Harmonic Distortion	24 bit	0dB	0.003			%
		-60dB	0.1	0.3		%
Isolation						
Channel Isolation (1kHz)			95	100		dB
DAC Accuracy						
Channel-to-Channel Gain Match Error				0.1	0.2	dB
Analog Output						
Full-scale Output Voltage			0.63×V _{DD}	0.66×V _{DD}	0.69×V _{DD}	V _{pp}
DC Voltage (V _Q)				0.5×V _{DD}		V _{DC}
Maximum DC Current at AOUT (I _{OUTmax})				3.3		mA
Maximum Current at VQ (I _{Qmax})				1		mA
Maximum Resistive Load (R _L)				1		kΩ
Maximum Capacitive Load (C _L)				1000		pF
Output Impedance (Z _{OUT})				110		Ω

Filtering Characteristics

Parameter		Min	Typ	Max	Unit
Single-Speed Mode					
Pass-Band	to -0.1dB Corner			0.35	f _s
	to -3dB Corner			0.4992	f _s
Frequency Response from 40Hz to 15kHz		-0.07		+0.55	dB
Stop-band		0.54			f _s
Stop-band Attenuation		55			dB
Group Delay(t _{GD})			10/f _s		s

Parameter		Min	Typ	Max	Unit
Double-Speed Mode					
Pass-Band	to -0.1dB Corner	0		0.22	f_s
	to -3dB Corner	0		0.501	f_s
Frequency Response from 40Hz to 15kHz		-0.02		+0.2	dB
Stop-band		0.54			f_s
Stop-band Attenuation		55			dB
Group Delay (t_{GD})			$5/f_s$		s
Quad-Speed Mode					
Pass-Band	to -0.1dB Corner	0		0.11	f_s
	to -3dB Corner	0		0.469	f_s
Frequency Response from 40Hz to 15kHz		-0.01		+0.1	dB
Stop-band		0.54			f_s
Stop-band Attenuation		55			dB
Group Delay(t_{GD})			$2.5/f_s$		s

Digital Input Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input High-level Voltage	V_{IH}	$0.7 \times V_{DD}$			V
Input Low-level Voltage	V_{IL}			0.6	V
Input Leakage Current	I_{in}		0.02		μA
Input Capacitance			3	8	pF

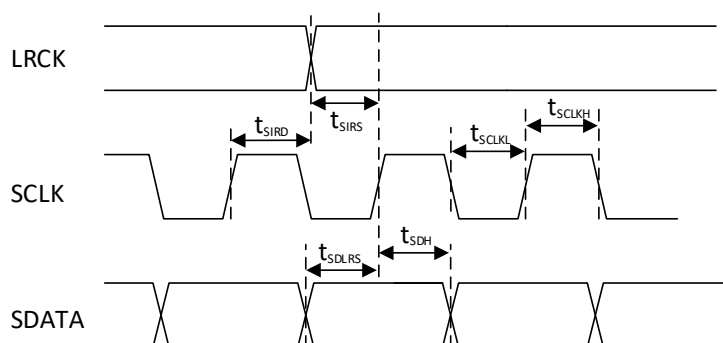
Power Dissipation

Parameter		Symbol	Min	Typ	Max	Unit
Operating Current	Normal Operation (3.3V)	I_A		32	50	mA
	Power Down state (3.3V)			200		μA
Power Supply Rejection Ratio	1kHz (3.3V)	PSRR		70		dB
	60Hz (3.3V)			50		dB

Switching Characteristics (Serial Interface)

Parameter		Symbol	Min	Typ	Max	Unit
MCLK Frequency			2		50	MHz
MCLK Duty Cycle			45		55	%
Input Sample Rate (MCLK/LRCK)	256x,384x,1024x	f_s	8		50	kHz
	256x,384x		84		134	kHz
	512x,768x		42		67	kHz
	1152x		30		34	kHz
	128x,192x		50		100	kHz
	64x,96x		100		200	kHz
	128x,192x		168		200	kHz
LRCK Duty Cycle			45	50	55	%
SCLK Pulse Width Low		t_{SCLKL}	20			ns
SCLK Pulse Width High		t_{SCLKH}	20			ns
SCLK Duty Cycle			45	50	55	%
Delay Time, SCLK Rising to LRCK Edge		t_{SLRD}	20			ns
Setup Time, SCLK Rising to LRCK Edge		t_{SLRS}	20			ns
Setup Time, SDIN Valid to SCLK Rising Edge		t_{SDLRS}	20			ns
Hold Time, SCLK Rising Edge to SDIN		t_{SDH}	20			ns

External Serial Interface Input Timing



FUNCTIONAL DESCRIPTION

The MS5282N accepts standard audio sampling frequency, including 48, 44.1, 32kHz in QSM mode; 96, 88.2 and 64kHz in DSM mode; 192, 176.4, 128kHz in SSM mode. Audio data is input through serial input data terminal (SDIN). LRCK determines the present channel of the input data. Serial clock is a clock where audio data enters the input data buffer.

Master Clock

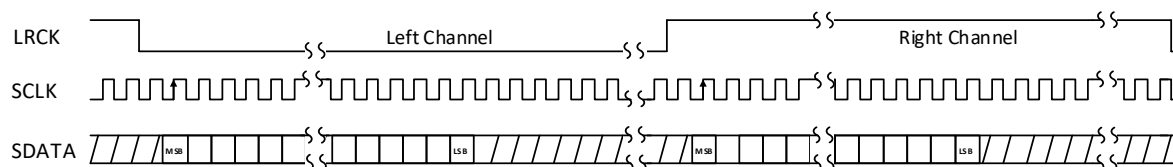
The MCLK/LRCK ratio must be an integer as shown in following table 1. The LRCK frequency is equal to F_s , the frequency of input data for each channel. The ratio of MCLK to LRCK and the speed mode are initialized by calculating the number of MCLK cycles and the value of MCLK within an LRCK cycle. A built-in divider will generate a proper clock. The following table lists some audio sampling frequencies, corresponding MCLK and LRCK frequencies. Note that even if there is no phase requirement, the LRCK and MCLK must be synchronized.

Table 1. Clock Frequency

Mode	LRCK (kHz)	MCLK(MHz)					
		128x	256x	384x	512x	768x	1024x
QSM	32	-	8.192	12.288	16.384	24.576	32.768
	44.1	5.6448	11.2896	16.9344	22.5792	33.868	45.158
	48	6.144	12.288	18.432	24.576	36.864	49.152
DSM	64	8.192	16.384	24.576	32.768	49.152	-
	88.2	11.2896	22.5792	33.868	45.1584	-	-
	96	12.288	24.576	36.864	49.152	-	-
SSM	128	24.576	32.768	49.152	-	-	-
	176.4	22.5792	45.1584	-	-	-	-
	192	24.576	49.152	-	-	-	-

Serial Input Clock

When 16 rising edge pulses are detected continuously at SCLK port during an LRCK cycle, external serial input clock is entered.



I²S, Up to 24-bit data, data valid on SCLK rising edge

MS5282N Data Format (I²S)

Initialization and Power Down

When system is initially powered up, it enters the power-down state. At this time, the interpolation filter and $\Delta-\Sigma$ modulator are reset. The internal reference voltage, digital-to-analog converter, switched-capacitor filter, and low-pass filter are shut down until system detects MCLK and LRCK clock. Once MCLK and LRCK are detected, the system starts to calculate the ratio of MCLK to LRCK, then powers up the internal reference

voltage, finally powers up the digital-to-analog converter, switched-capacitor filter, and outputs the quiescent voltage VQ.

Output Transient Control

The MS5282N uses specified technology to reduce transient response during power-up and power-down.

Power Up

The DC level at the output terminal is provided by VQ pin, which is low when system is initially powered up. When MCLK detects this, VQ generates normal DC voltage. The start-up time is 400ms when a 10uF capacitor is connected to VQ pin.

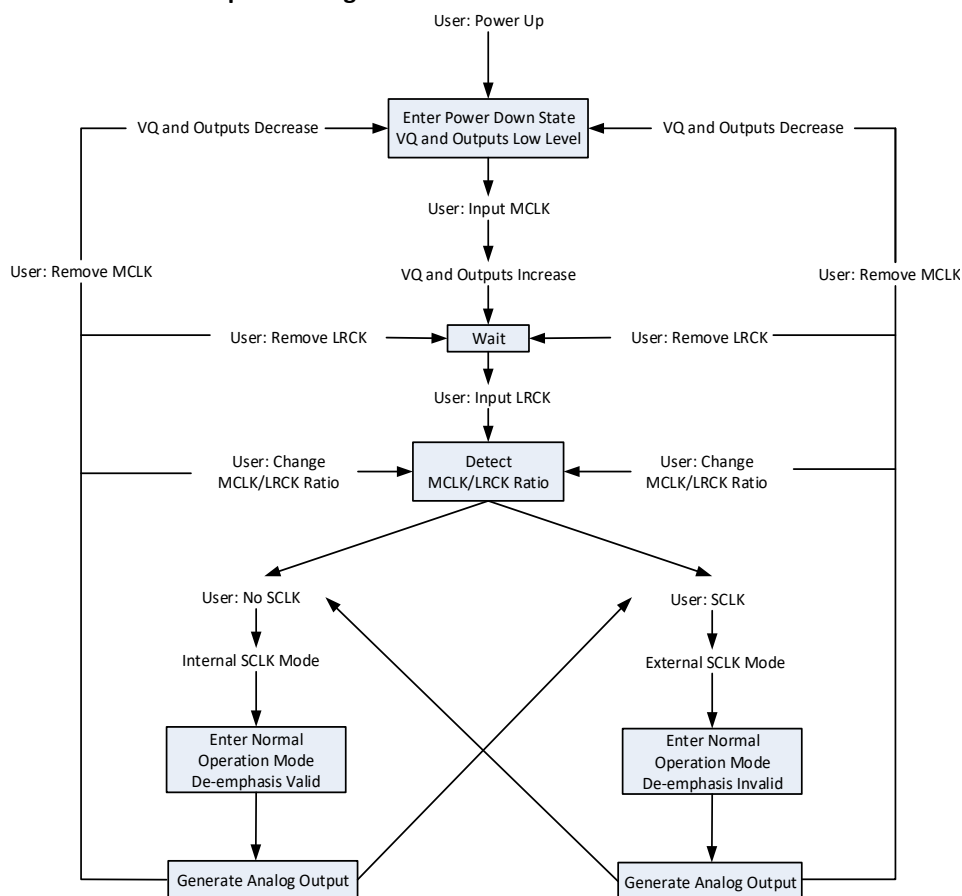
Power Down

To prevent transient pulses at the output terminal during power down, a 10uF capacitor is connected to VQ pin. During this time, the voltage on VQ pin and output pin gradually descend to GND. When it is necessary to change clock frequency or sample frequency, it is better to keep 10 LRCK cycles low level. The DAC keeps low level output during clock change.

Ground and Power Supply Decoupling

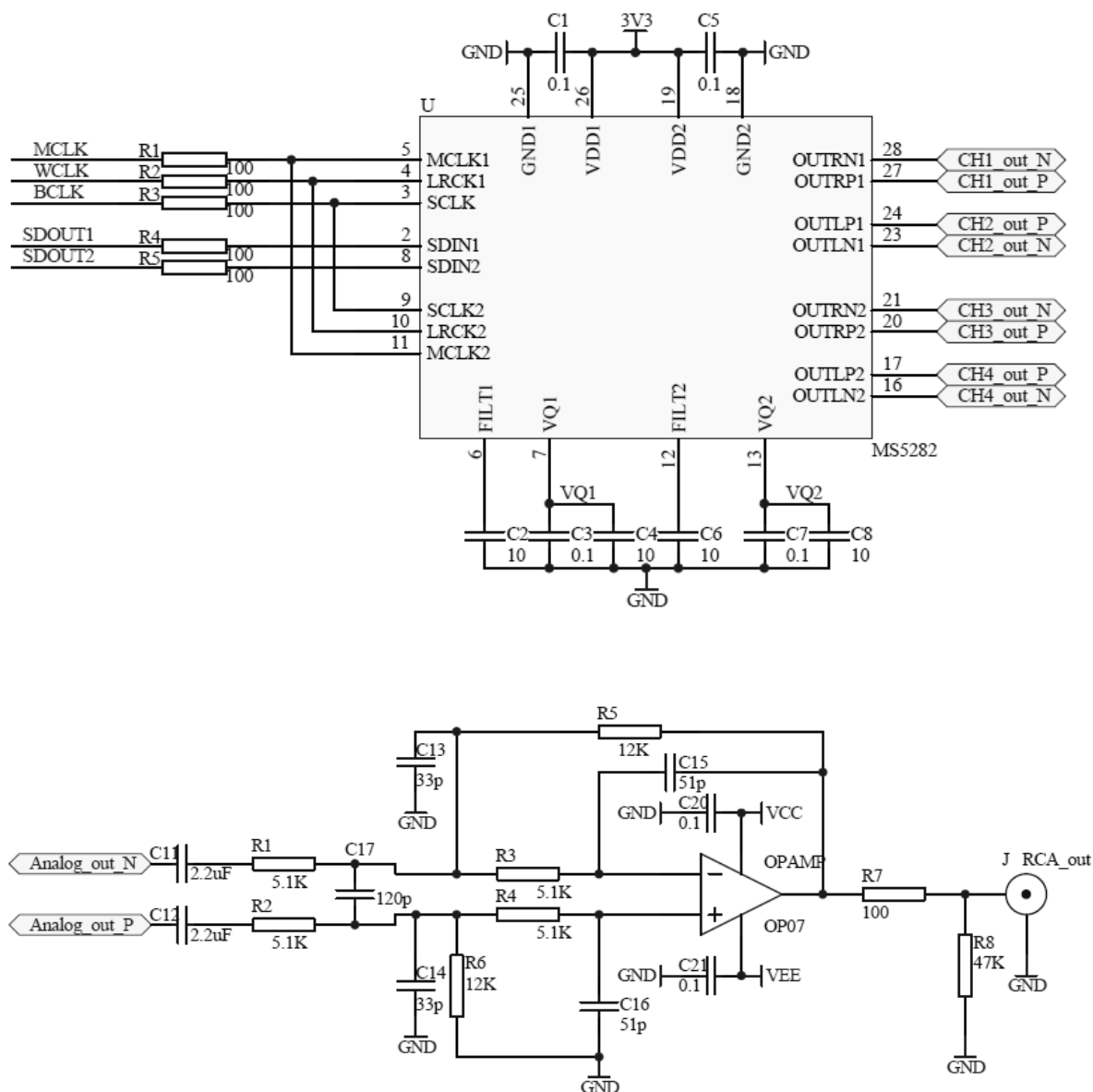
Be careful with connection between ground and power to achieve the ideal performance. For best performance, the decoupling and filtering capacitors must be placed as close to chip as possible.

Initiation and Power-Down Sequence Diagram



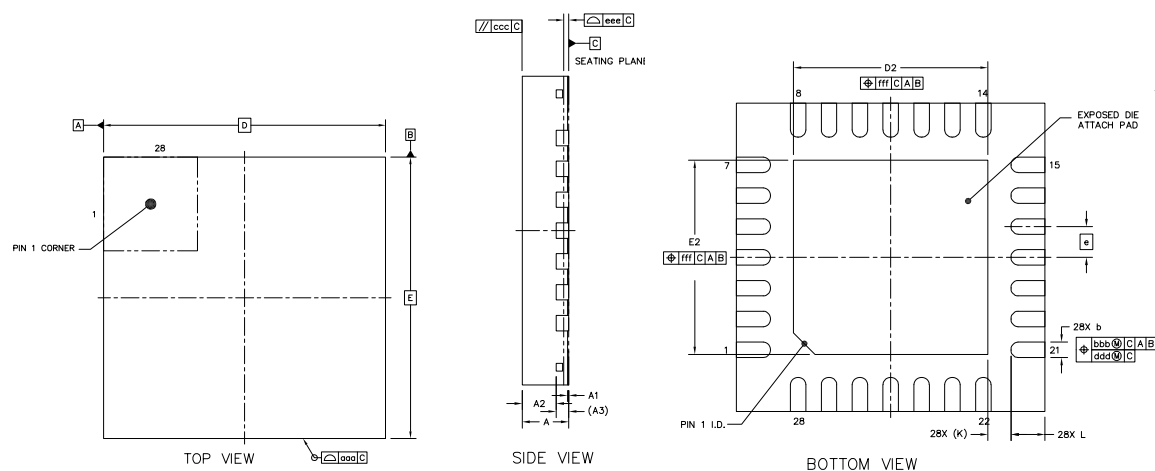
Initiation and Power Down Sequence Diagram

TYPICAL APPLICATION



PACKAGE OUTLINE DIMENSIONS

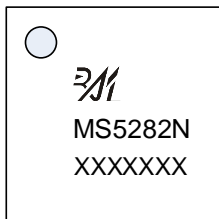
QFN28



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.2	0.25	0.3
D	5 BSC		
E	5 BSC		
e	0.5 BSC		
D2	3.05	3.15	3.25
E2	3.05	3.15	3.25
L	0.45	0.55	0.65
K	0.375 REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
ddd	0.05		
fff	0.1		

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS5282N

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5282N	QFN28	1000	8	8000	4	32000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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