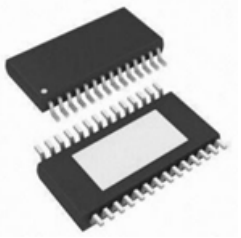
Dual DMOS Full Bridge Driver

PRODUCT DESCRIPTION

The MS35656/MS35656N is a dual DMOS full bridge driver, which can drive a stepper motor or two DC motors. The driving current of each full bridge can be up to 1.4A with 24V power supply. The MS35656/MS35656N integrates a fixed off-time PWM current regulator and a 2bit nonlinear DAC that allow stepper motor to operate in full, half and quarter steps, and DC motor to operate in forward, reverse, and standby modes. PWM current regulator can choose fast decay, slow decay and mixed decay modes, so it can meet different motors to reduce audio motor noise. The MS35656/MS35656N also has an internal synchronous rectification control circuit to reduce the power dissipation during PWM operation.

The MS35656/MS35656N integrates protection circuits, such as undervoltage protection (UVLO), short-circuit protection, overturn current protection and thermal shutdown.

QFN28



eTSSOP28

FEATURES

- Peak Current: 2A
- Dual Full Bridge
  Drive a Stepper Motor or Two DC Motors
- Synchronous Rectification
- Built-in UVLO
- Thermal Shutdown
- Overturn Current Protection
- Ultra-low Power Dissipation for Sleep Mode
- Short-circuit Protection (Short to Power, Ground and Output)

APPLICATIONS

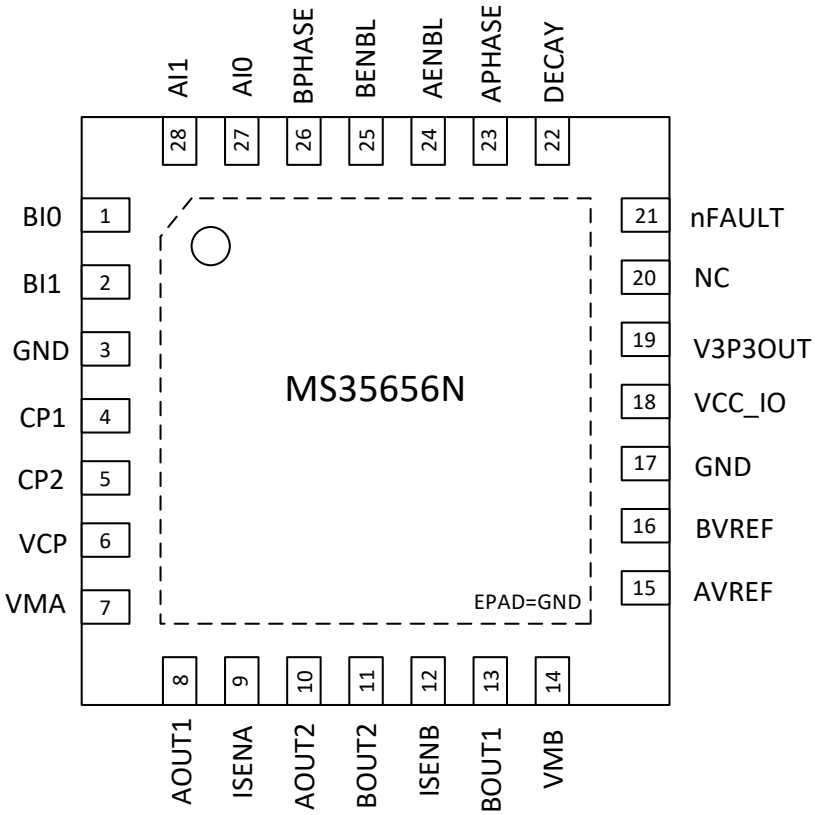
- Security Monitoring
- Stage Light
- Toy
- Robotic Technology
- Medical Equipment

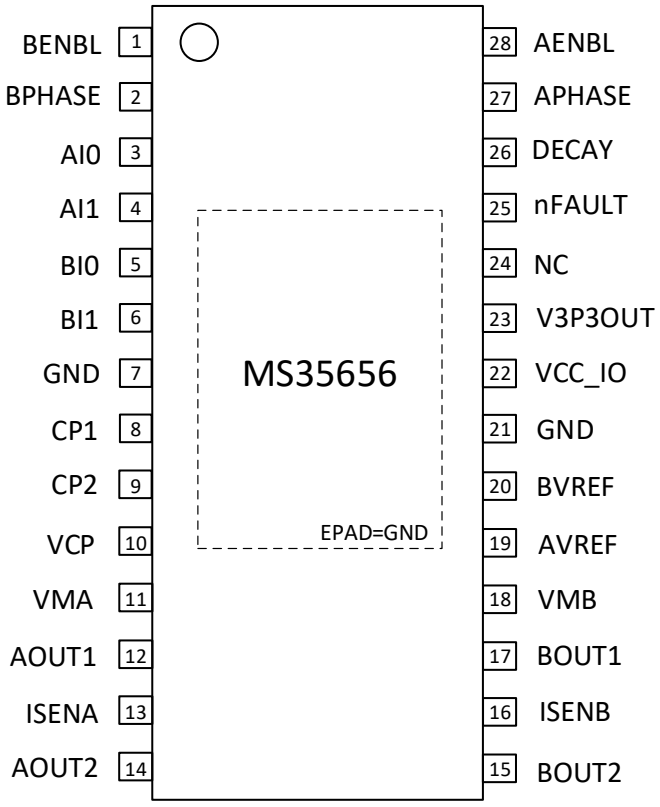
PRODUCT SPECIFICATION

Part Number	Package	Marking
MS35656N	QFN28	MS35656N
*MS35656	eTSSOP28	MS35656

*The package is not available temporarily. If necessary, please contact Hangzhou Ruimeng Sales Department Center.

PIN CONFIGURATION

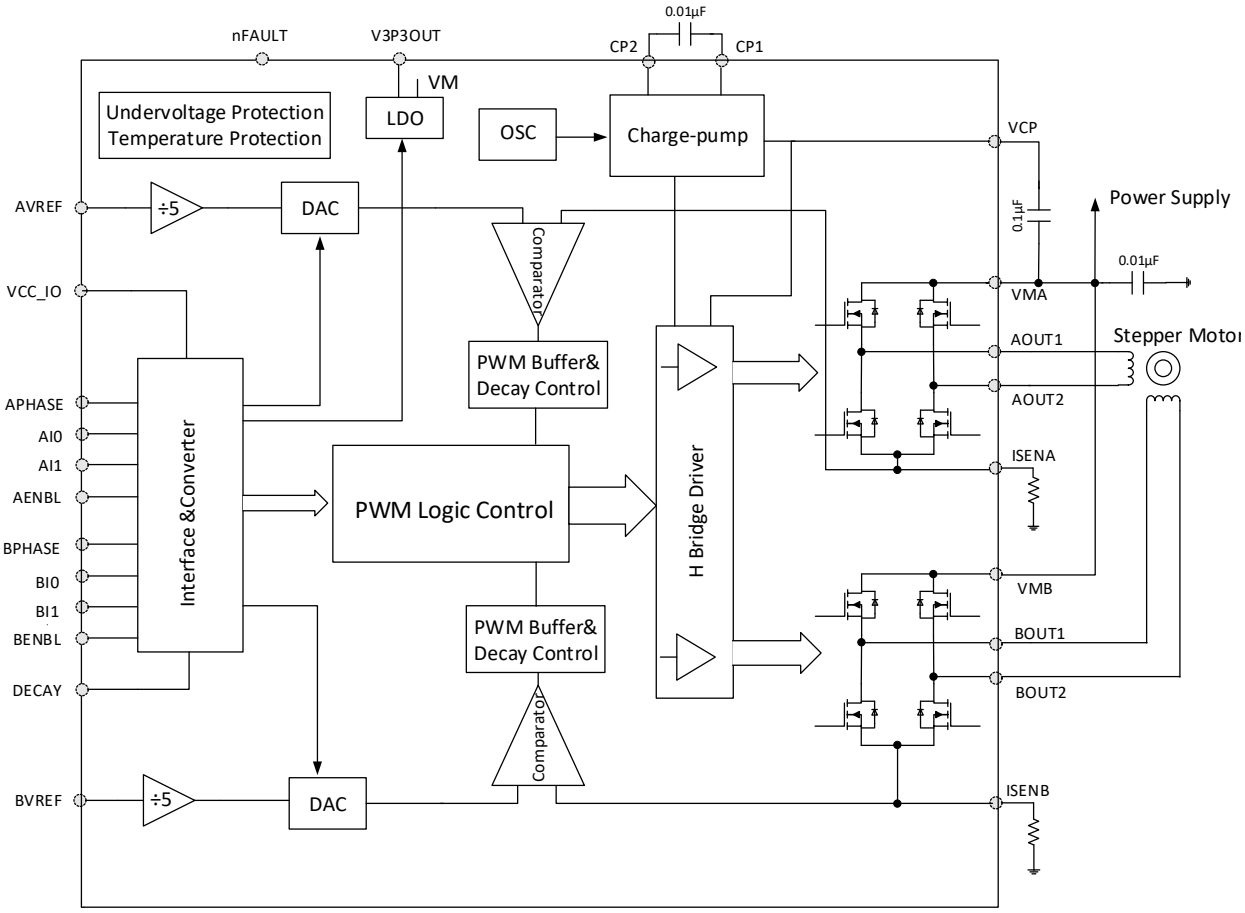




PIN DESCRIPTION

Pin		Name	Description
MS35656N	MS35656		
1	5	BI0	Control Input Pin
2	6	BI1	Control Input Pin
3	7	GND	Ground
4	8	CP1	Charge-pump Capacitor Pin
5	9	CP2	Charge-pump Capacitor Pin
6	10	VCP	High-side Gate Drive Voltage
7	11	VMA	Power Supply
8	12	AOUT1	Bridge A Out1
9	13	ISENA	Bridge A Sense
10	14	AOUT2	Bridge A Out2
11	15	BOUT2	Bridge B Out2
12	16	ISENB	Bridge B Sense
13	17	BOUT1	Bridge B Out1
14	18	VMB	Power Supply
15	19	AVREF	Analog Control Input Pin
16	20	BVREF	Analog Control Input Pin
17	21	GND	Ground
18	22	VCC_IO	Digital Logic Interface Power Supply
19	23	V3P3OUT	Internal 3.3V LDO Output
20	24	NC	Not Connection
21	25	nFAULT	Fault Indication Signal Pin
22	26	DECAY	Decay Mode Selection
23	27	APHASE	Control Input Pin
24	28	AENBL	Control Input Pin
25	1	BENBL	Control Input Pin
26	2	BPHASE	Control Input Pin
27	3	AI0	Control Input Pin
28	4	AI1	Control Input Pin
-	-	EPAD	Thermal Pad, Must Connect to GND

BLOCK DIAGRAM



Note: VMA is shorted to VMB internally.

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VM	-0.5 ~ 38	V
Logic Voltage	VCC_IO	-0.4 ~ 7	V
Output Current	I_{OUT}	2	A
Logic Input Voltage Range	V_{in}	-0.3 ~ 7	V
ISENx Pin Voltage	V_{SENSEx}	± 0.5	V
xVREF Pin Voltage Range	V_{xREF}	2.5	V
Operating Temperature	T_A	-40 ~ 85	℃
Junction Temperature	T_J	150	℃
Storage Temperature	T_{stg}	-40 ~ 150	℃
ESD	HBM	> ± 3k	V

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ELECTRICAL CHARACTERISTICS

Ta = 25°C±2°C, VM = 24V, unless otherwise noted.

Power Supply

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Driving Power Supply	VM		7		30	V
IO Power Supply	VCC_IO		1.4		5.5	V
Power Supply Current during Operation	I_M			2.5		mA
Power Supply Current during Sleep	I_{MQ}	Enter sleep mode			1	μA

Internal Regulator Power Supply

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Internal Voltage Output	V_{3P3OUT}	IOUT=1mA, Tj=25°C		3.3		V
Drive Current Capability	I_{3P3OUT}				10	mA

Output FET

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-side FET On-resistance	R_{DSONH}	IOUT=100mA, Tj=25°C		0.24		Ω
Low-side FET On-resistance	R_{DSONL}	IOUT=100mA, Tj=25°C		0.25		Ω
Output Leakage Current	I_{DSS}	at Z state		280		μA

Logic and Low Voltage Input

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Logic Input High Level	$V_{in(H)}$	VCC_IO=3.3V		2.0		V
Logic Input Low Level	$V_{in(L)}$	VCC_IO=3.3V		1.4		V
xVREF Input Voltage	V_{xREF}		0		2.5	V
xVREF Input Current	I_{XREF}	VREF=1.5V			±1	μA
Standby Detection Time	$t_{standby}$	APHASE=AENBL=BPHASE=BENBL=0		2.8		ms

Timing

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay	td1	PWM conversion, HS FET open	350	550	1000	ns
	td2	PWM conversion, HS FET closed	35		300	ns
	td3	PWM conversion, LS FET open	350	550	1000	ns
	td4	PWM conversion, FET closed	35		250	ns
Crossover Delay	tcod		300	425	1000	ns
Blank Time	tblank			3.75		µs
Fixed Off-time	toff	Current decay time after triggering I_{Trip}		18		µs

Protection Circuit

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VM Undervoltage Protection	$V_{UV(VM)}$	VM rising	6.5	6.8	7.1	V
VM Undervoltage Hysteresis	$V_{UV(VM)HYS}$		300	400	500	mV
Overcurrent Protection Trip Level	I_{OCP}			3.5		A
Overcurrent Protection Detection Time	t_{OCP}			2.5		µs
Auto Restart Close Time for Overcurrent Protection	t_{pro}	Trigger overcurrent protection		20		ms
Thermal Shutdown Protection	T_{JTSD}	Temperature rising	155	165	175	°C
Thermal Shutdown Protection Hysteresis	T_{JTSD_HYS}			15		°C

FUNCTION DESCRIPTION

Device Characteristics

The MS35656/MS35656N can drive a stepper motor or two DC motors. Each full bridge consists of four N-channel MOS FETs and controlled by pulse width modulation (PWM). Output peak current of each full bridge is decided by ISENX and xVREF.

Full Bridge Control Logic

xPHASE input pin controls the current direction of H bridge. When xENBL pin is high, the corresponding full bridge output will be turned on. The following table shows the logic of full bridge control:

xENBL	xPHASE	xOUT1	xOUT2
0	X	Z	Z
1	1	H	L
1	0	L	H

Internal PWM Current Control Principle

Each full bridge has PWM current control circuit with fixed off-time, which makes the load current not more than setting value, I_{Trip}. One H-bridge diagonal pair of source and drain DMOS FETs are enabled, and current flows into motor and Rsense resistor. When the voltage on Rsense is equal to one fifth of VREF voltage, current detection comparator would reset the PWM latch and disable source DMOS FET.

The maximum current limit is determined by the resistance of Rsense (Rs) and the voltage on VREF terminal. The maximum current formula is as follows:

$$I_{TripMax}=V_{REF}/(5\times Rs)$$

Note that the maximum voltage value on RSENSE shall not exceed ±500mV in application.

In addition, xI1 and xI0 are used to control the proportion of full-scale current set by VREF and Rsense. The functions are as follows:

xI1	xI0	Current Proportion(Percentage of Full-scale)
1	1	0%
1	0	33%
0	1	66%
0	0	100%

Full, half and quarter step modes can be realized by control. Detail in ”Step Sequencing Diagram” .

Fixed Off-time

Internal PWM control circuit integrates one fixed-time pulse to disable FETs. The off-time, toff is set as 18μs.

Blank Time

When internal circuit control changes the output, this function can turn off the output current detection comparator to prevent output false detection, such as overshoot current, reverse recovery current of clamp diode, reverse transmission caused by output capacitance and so on. Blank time is set to 1μs.

Charge-pump (CP1 and CP2)

Charge-pump circuit generates a higher power supply than VM to drive the source-side FET of H-bridge. In application, due to the need of charge and discharge, a 0.01μF capacitor needs to be connected between CP1 and CP2. A 0.1μF capacitor is also required between VCP and VMx to store charge.

Shutdown Function

When junction temperature is exceeded or VCP is too low, the output will be turned off. Undervoltage lockout (UVLO) can turn off the output at power-up.

Synchronous Rectification

When internal fixed off-time circuit is triggered and PWM-off works, the load current will return. In the process of current decaying, synchronous rectification circuit of the MS35656/MS35656N will turn on the corresponding DMOS FET and short out the body diode with RDS(on), which can effectively reduce the power dissipation. When zero current is detected, synchronous rectification is turned off to prevent the load current from reversing.

Sleep Mode

When all control input pins are grounded, i.e. AENBL=APHASE=BENBL=BPHASE=0, and the duration of low-level exceeds 2.8ms, the MS35656/MS35656N will enter the sleep mode with low power dissipation. At this time, all of modules in the chip shut down, including V3P3OUT pin output. When one of these input control pins goes high, the chip will be woken up again and start working.

Overcurrent Protection

The MS35656/MS35656N integrates overcurrent protection function. These conditions can be detected, such as short to power, ground or output. When short-circuit time exceeds 2.5μs, the chip will close the output stage. After about 20ms, the chip will try to restart automatically.

Decay Mode

During PWM chopping, coil current will be driven to reach the setting value after the H-bridge is enabled, as shown below.

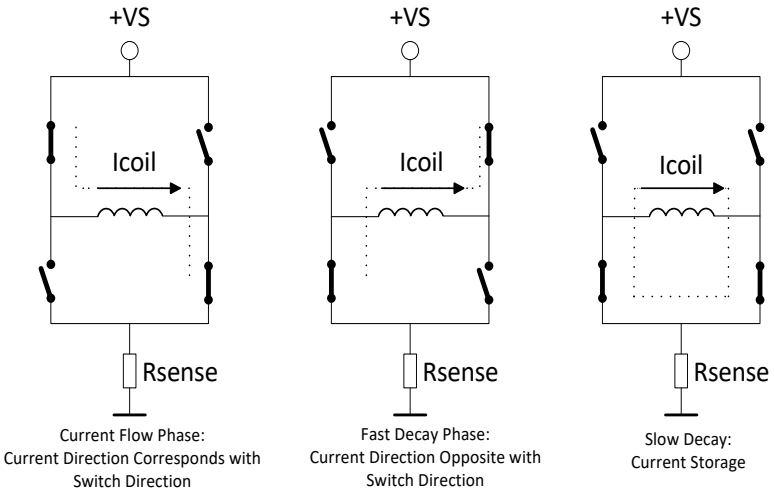


Figure 1. H-Bridge Operation Mode

When coil current reaches the setting threshold, H-bridge may operate in two modes, fast decay or slow decay.

In the fast decay mode, when coil current reaches the setting threshold, H-bridge will be turned on reversely to make the coil current drop rapidly. When the current in the coil approaches 0, H-bridge will be closed immediately to prevent reverse current.

In the slow decay mode, coil current is attenuated by starting the double low-side FETs.

The MS35656/MS35656N supports fast decay, slow decay and mixed decay modes. The selection of these modes is controlled by DECAY pin.

When DECAY pin is high(>2V), select fast decay mode. After I_{Trip} is triggered, two FETs are enabled with opposite operation directions and decay period is 18μs;

When DECAY pin is low(<1.3V), select slow decay mode. After I_{Trip} is triggered, dual low-side FETs are enabled and decay period is 18μs;

When DECAY pin is between 1.4V and 1.9V or floating, select mixed decay mode, and decay period is 18μs;

As shown in Figure 2 and Figure 3 below, after I_{Trip} is triggered, mixed decay mode starts from fast decay and continues for 75% of the whole decay cycle before entering slow decay. The decay period is 18μs.

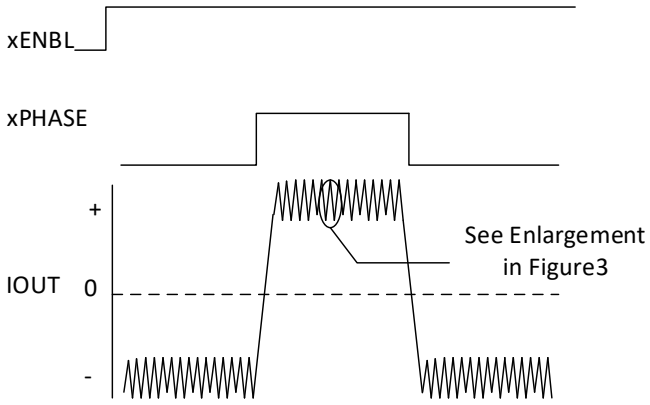


Figure 2. Mixed Decay Mode

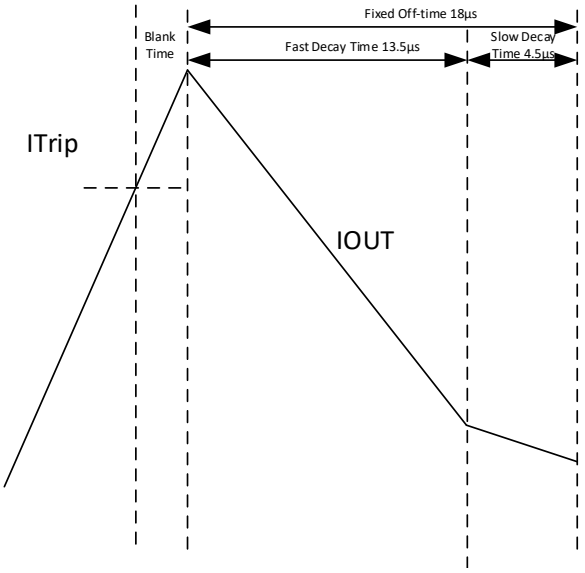


Figure 3. Enlargement View of Mixed Decay Mode

Step Sequencing Diagram

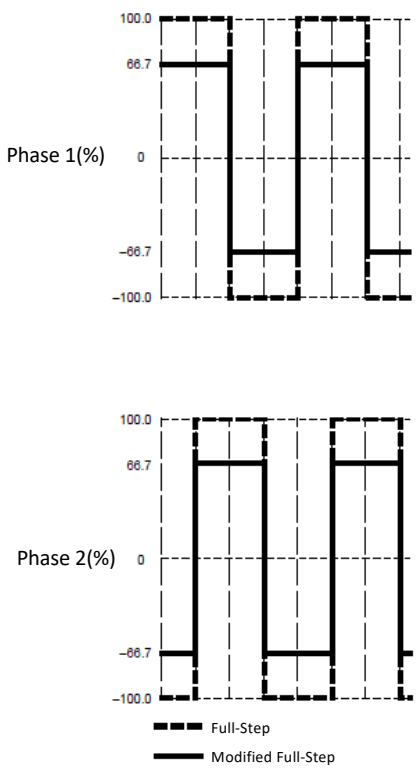


Figure 4. Step Sequencing for Full-Step

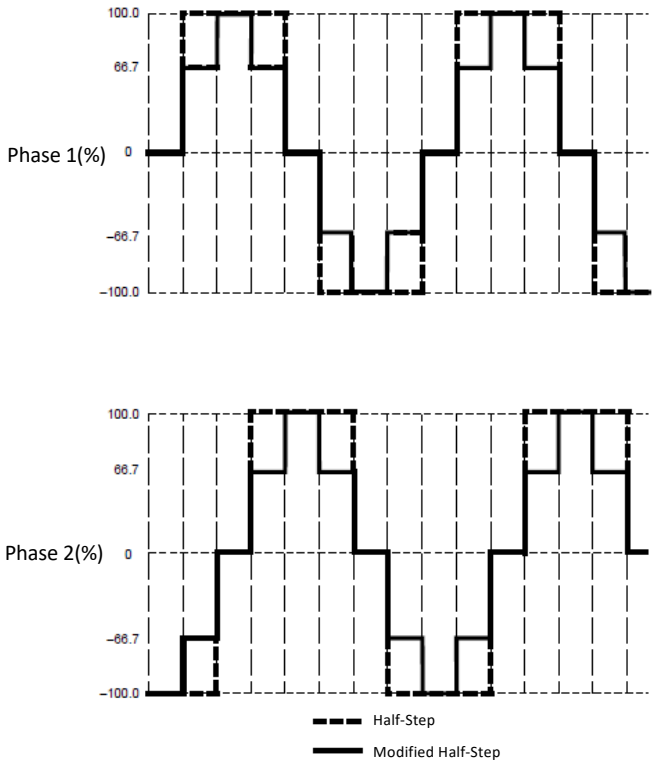


Figure 5. Step Sequencing for Half-Step

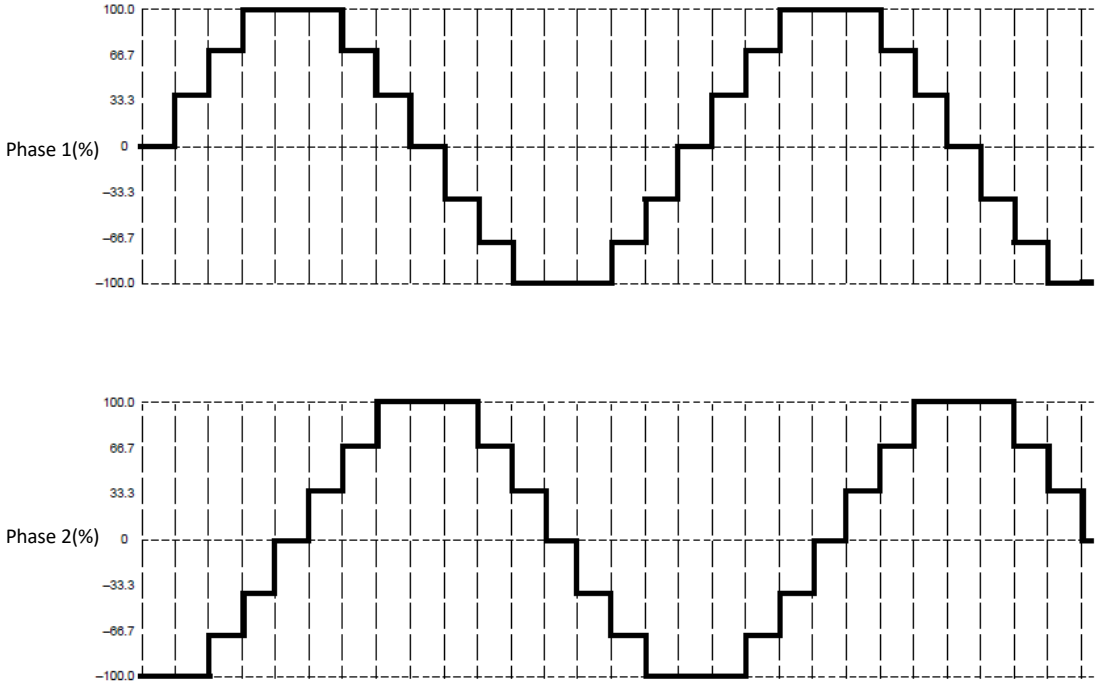


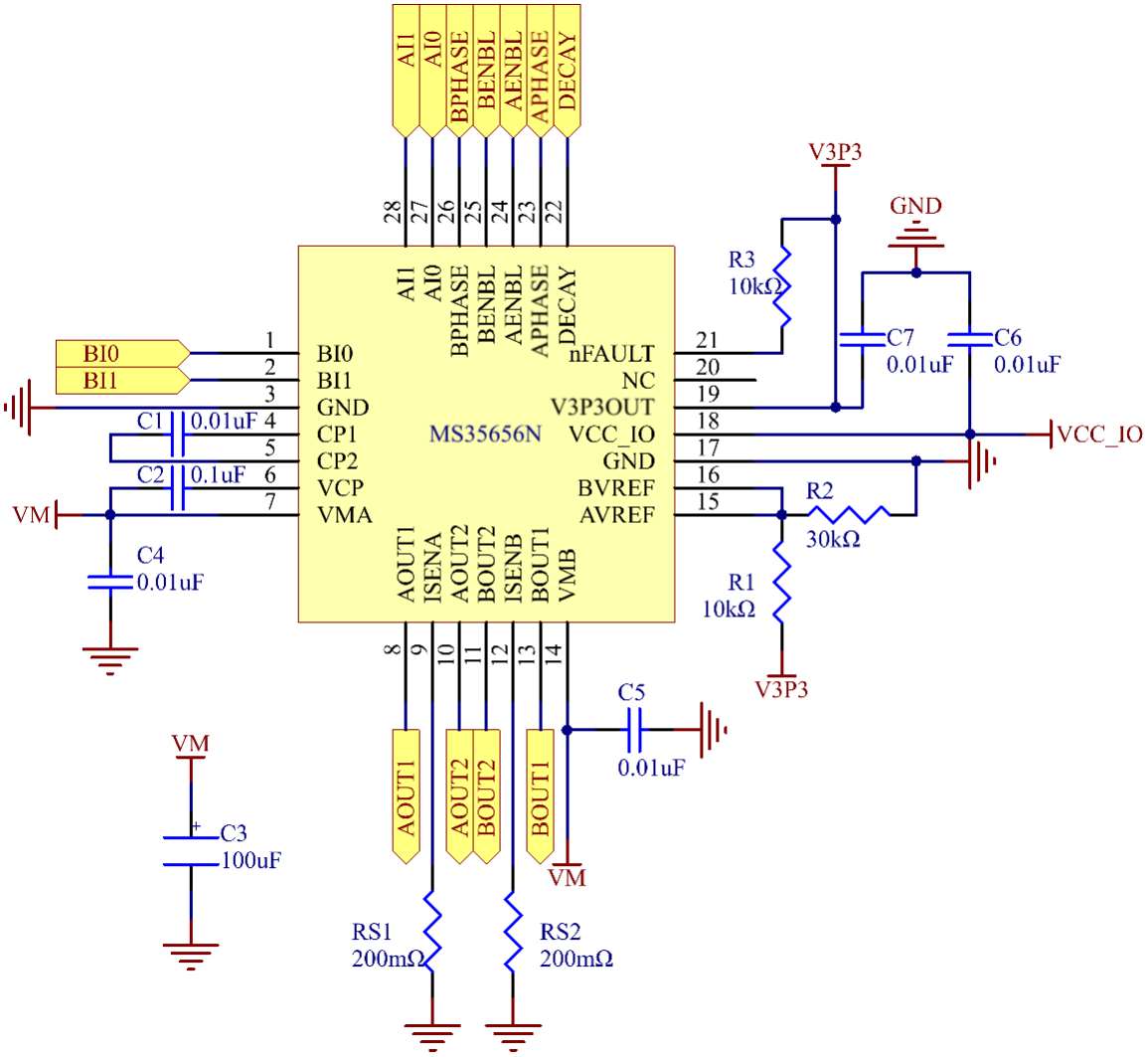
Figure 6. Step Sequencing for Quarter-Step

Step Sequencing Setting

Full	1/2	1/4	Phase 1 (% $I_{TripMax}$)	xI0	xI1	Phase	Phase 2 (% $I_{TripMax}$)	xI0	xI1	Phase
	1	1	0	H	H	X	100	L	L	0
		2	33	L	H	1	100	L	L	0
1	2	3	100/66*	L/H*	L	1	100/66*	L/H*	L	0
		4	100	L	L	1	33	L	H	0
	3	5	100	L	L	1	0	H	H	X
		6	100	L	L	1	33	L	H	1
2	4	7	100/66*	L/H*	L	1	100/66*	L/H*	L	1
		8	33	L	H	1	100	L	L	1
	5	9	0	H	H	X	100	L	L	1
		10	33	L	H	0	100	L	L	1
3	6	11	100/66*	L/H*	L	0	100/66*	L/H*	L	1
		12	100	L	L	0	33	L	H	1
	7	13	100	L	L	0	0	H	H	X
		14	100	L	L	0	33	L	H	0
4	8	15	100/66*	L/H*	L	0	100/66*	L/H*	L	0
		16	33	L	H	0	100	L	L	0

*Modified step mode

TYPICAL APPLICATION



IO Power Supply

The chip designs IO power pin VCC_IO, which is specially used to supply power to IO interface. The power supply needs to be connected with the single chip microcomputer power supply and supports 1.8V-5V power supply. It is recommended to connect a 0.01μF capacitor in application.

Power-on Sequence

The internal low-voltage input port of the MS35656 (AVREF, BVREF, AI0, AI1, BI0, BI1, APHASE, BPHASE, AENBL, BENBL, DECAY) have forward diodes to VCC_IO, the recommended power-on process is as follows:

VM and VCC_IO should be powered on firstly, there is no requirement for power-on. After powering on, APHASE or BPHASE pin is pulled high to wake up the chip, and other pins keep in low level. After about 1ms, control inputs can be made to the chip.

When controlling, be aware that APHASE, BPHASE, AENBL and BENBL keeping in low level can not exceed

2.8ms at the same time, or the chip will be in sleep mode with low power dissipation.

DC Motor Control

The chip integrates two H-bridge drives, each of which is equipped with an independent PWM current control circuit, so it can drive a DC motor. In application, the maximum current can be set through the VREF pin. I0, I1 and PHASE pin can be controlled by PWM signal to control the forward rotation, reverse rotation and standby of the motor.

Layout Making

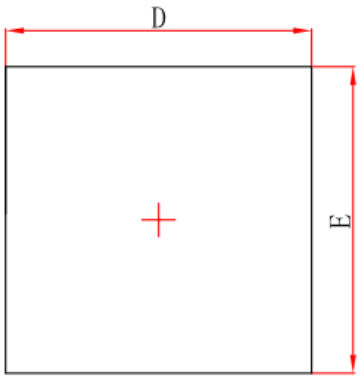
Heavy ground plane is required for printed circuit board. In order to achieve better performance and heat dissipation, the MS35656/MS35656N should be soldered directly to the board. On the back of MS35656/MS35656N is a metal exposed pad, which is directly soldered on the exposed PCB to radiate heat to other layers.

Sense Pin Setting

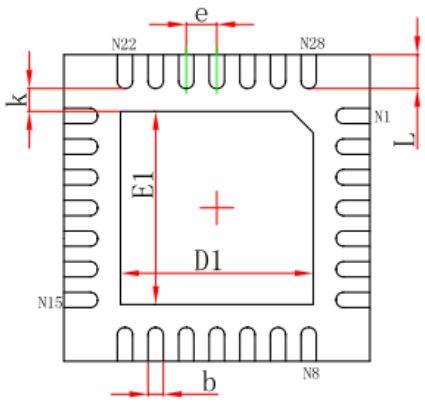
Sense pin resistance, RSx must have a low impedance path to the ground, because a large current will flow through RSx and generate an accurate feedback voltage to the Sense comparator. Long ground traces will produce additional resistance, generate uncertain voltage drop and reduce the accuracy of the Sense comparator. When selecting the Sense resistor, pay attention to ensure that the voltage on the Sense pin does not exceed ± 500mv during operation.

PACKAGE OUTLINE DIMENSIONS

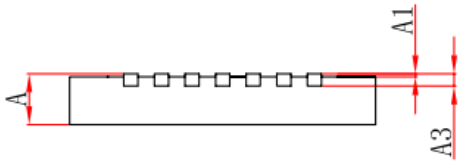
QFN28



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	4.900	5.100	0.193	0.201
E	4.900	5.100	0.193	0.201
D1	3.050	3.250	0.120	0.128
E1	3.050	3.250	0.120	0.128
k	0.200MIN		0.008MIN	
b	0.180	0.300	0.007	0.012
e	0.500TYP		0.020TYP	
L	0.450	0.650	0.018	0.026

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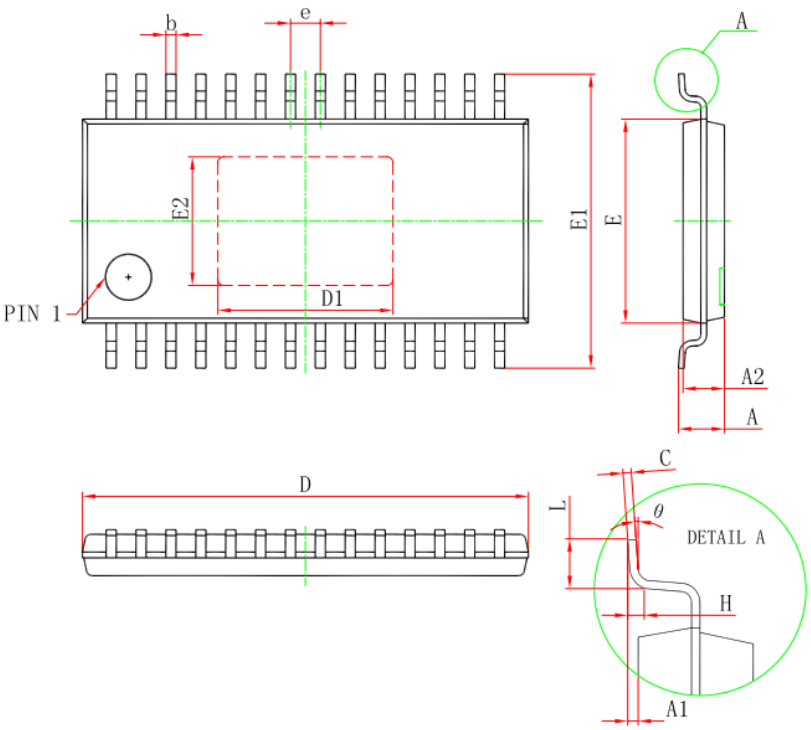

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	9.600	9.800	0.378	0.386
D1	3.710	3.910	0.146	0.154
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
E2	2.700	2.900	0.106	0.122
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description

Product Name: MS35656N, MS35656

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS35656N	QFN28	4000	1	4000	8	32000
MS35656	eTSSOP28	3000	1	3000	8	24000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.


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