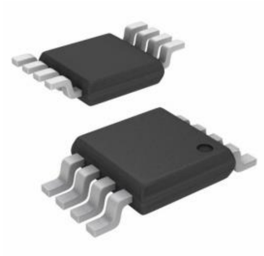
RF Detector/Controller

PRODUCT DESCRIPTION

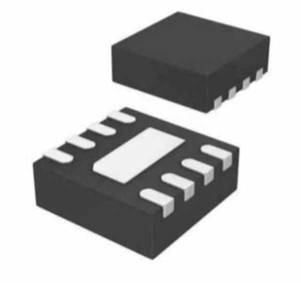
The MS2351M/MS2351D is a logarithmic amplifier chip, which is mainly used for receiving signal strength indication (RSSI) and controlling power amplifier. Its operating frequency ranges from 0.05GHz to 4.0GHz. Dynamic range can reach from 35dB to 45dB.

The MS2351M/MS2351D is a voltage response device. When it operates in the frequency range of 0.05GHz to 2.5GHz, the root mean square value of typical input signal ranges from 1.25mV to 224mV or from -45dBm~0dBm@50Ω.

The MS2351M/MS2351D uses AC coupling internally and provides two voltage outputs. One is from V_UP pin. The other one is from V_DN pin, which is the reverse phase of V_UP voltage and twice the gain. V_DN output drops from 2.20V to close to ground, which makes the chip operate in control mode.



MSOP8



DFN8

FEATURES

- Complete RF Detector/ Controller Function
- Dynamic Range in Typical Conditions:
  0.05GHz~2.5GHz: -45dBm~0dBm@50Ω
  2.6GHz~3.0GHz: -40dBm~0dBm@50Ω
  3.1GHz~4.0GHz: -35dBm~0dBm@50Ω
- 10dB Step Response Time: 83ns
- Good Temperature Stability
- Single Power Supply: 2.7V~5.5V

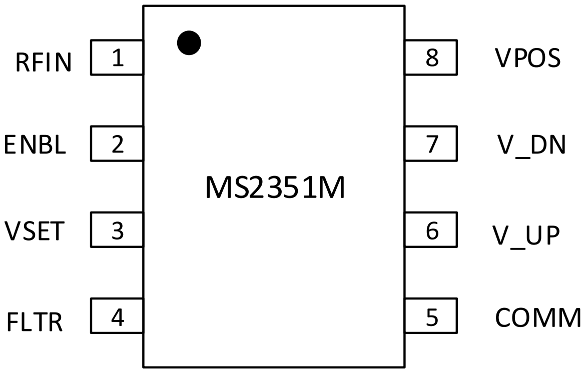
APPLICATIONS

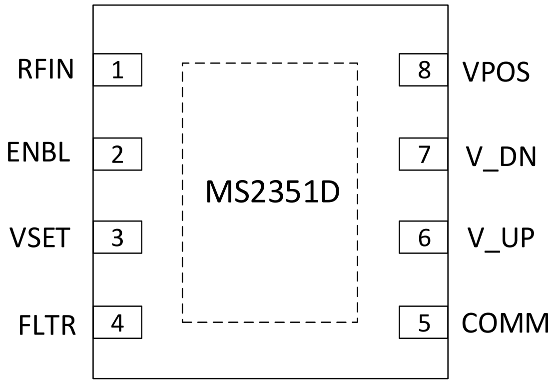
- Reception of Wireless Terminal and TSSI
- Transmitter Power Measurement and Control

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS2351M	MSOP8	MS2351M
MS2351D	DFN8	2351D

PIN CONFIGURATION

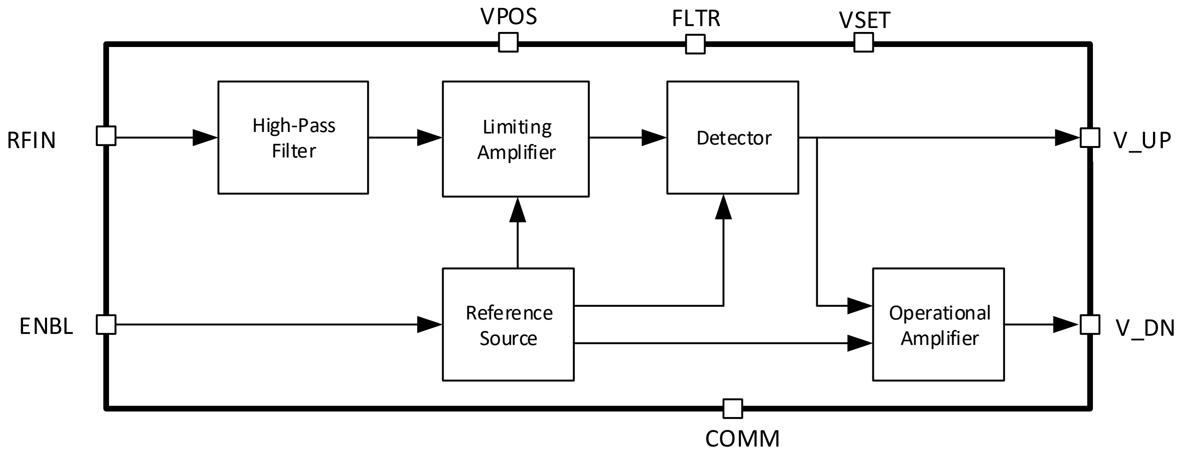




PIN DESCRIPTION

Pin	Name	Type	Description
1	RFIN	I	RF Input
2	ENBL	I	Connected to Power Supply: Normal Operation Mode. Connected to Ground: Shutdown.
3	VSET	I	Set the voltage for operating in control mode. VSET is connected to V_UP for operating in measurement mode.
4	FLTR	O	Connected with the external capacitor to extend output response time. The capacitor is connected between FLTR and V_UP
5	COMM	-	Reference Ground
6	V_UP	O	Logarithmic Output. Output is proportional to input signal amplitude
7	V_DN	O	Reverse Phase of V_UP. Relationship: V_DN=2.20-2×V_UP
8	VPOS	-	Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn’t represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	V_{POS}	5.5	V
V_UP, V_DN, VSET, ENBL		0 ~ V_{POS}	V
Input Voltage		1.6	V rms
Equivalent Power		+17	dBm
Maximum Allowable Power Dissipation	P_D	200	mW
Operating Temperature[1]	T_A	-40 ~ +85	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C
Soldering Temperature (10s)	T_{SOLDER}	260	°C

Note 1: Actual operating temperature range is relative to operating frequency.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{POS}=3.3V, T_A = 25°C .

Parameter	Condition	Min	Typ	Max	Unit
Overall Characteristics	45dB Dynamic Range	0.05		2.5	GHz
	40dB Dynamic Range	2.6		3.0	GHz
	35dB Dynamic Range	3.1		4.0	GHz
Input Voltage	AC-Coupled Internally	1.25		224	mV rms
Equivalent Power	51Ω External Termination, 0.05GHz~2.5GHz	-45		0	dBm
	51Ω External Termination, 2.6GHz~3.0GHz	-40		0	dBm
	51Ω External Termination, 3.1GHz~4.0GHz	-35		0	dBm
Logarithmic Slope	V_UP,100MHz		22.6		mV/dB
Logarithmic Intercept	V_UP,100MHz, 51Ω External Termination		-45		dBm
Input Interface, RFIN Pin					
DC Resistance to Ground			95		kΩ
In-Band Input Resistance	f=0.1GHz		3		kΩ
Input Capacitor	f=0.1GHz		2.3		pF
Main Output, V_UP Pin					
Voltage Range	Connect V_UP to VSET @1.9GHz	0.01		0.982	V
Minimum Output Voltage	No Signal Input on RFIN, R_L≥10k		0.01		V
Maximum Output Voltage	R_L≥10k @1.9GHz 0dBm		0.982		V
Absolute Operating Voltage Range	2.7V≤VPOS≤5.5V	V_{POS}-1.1	V_{POS}-1		V
Available Output Current	Current Source/ Current Sink	18.5/2.1	18.6/2.2	19.2/2.3	mA
Response Time	10%-90%, 10dB Step		83		ns
Residual RF Signal	f=0.1GHz, Worst Condition		30		μV
Inverted Output, V_DN Pin					
Gain Referred to V_UP	V_DN=2.20-2 × V_UP		-2		
Minimum Output Voltage	V_{POS}≥3.3V @1.9GHz 0dBm		0.286		V
Maximum Output Voltage	V_{POS}≥3.3V		2.20		V
Available Output Current	Current Source/ Current Sink	37.5/2.1	38/2.1	39/2.5	mA

Parameter	Condition	Min	Typ	Max	Unit
Output Reference Noise	RFIN=2GHz, -33dBV, f_{NOISE}=10kHz		0.16		$\mu V/\sqrt{Hz}$
Full-Scale Settling Time	-40dBm to 0dBm		142		ns
Input Settings, VSET Pin					
Voltage Range	Corresponding to Central 40dB	0.15		1.1	V
Input Resistor		10.5	11	11.6	kΩ
Logarithmic Slope	f=0.9GHz f=1.9GHz		22.6 22.4		mV/dB
Enable Interface, ENBL Pin					
Enabled On	High-Level Input, -40°C~85°C	1.9		V_{POS}	V
Input Current when Enabled	ENBL=2.7V, -40°C~85°C		20	300	μA
Enabled Off	Low-level Input, -40°C~85°C	-0.5		0.1	V
Power Supply, VPOS Pin					
Power Supply		2.7	3.3	5.5	V
Quiescent Current in the Temperature Range	-40°C~85°C	4.2	4.3	6.8	mA
Enable Shutdown Current in the Temperature Range	-40°C~85°C		0.44	6.8	mA

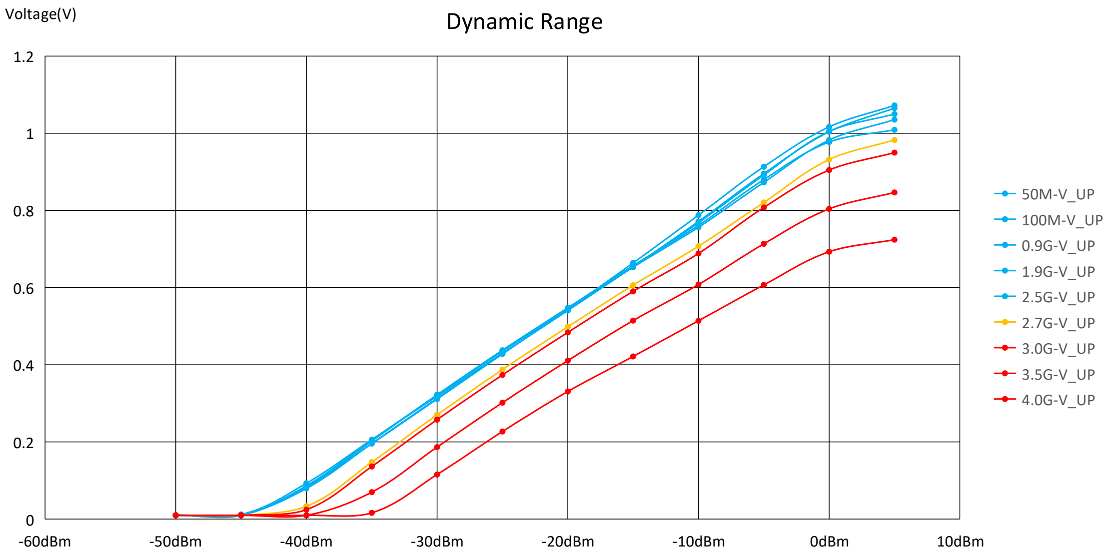
In typical operating conditions, the relationship between outputs V_UP, V_DN and input power as well as input frequency is as follows:

Input Frequency (Hz)	0.05G		0.1G		0.9G	
Input Power (dBm)	50M-V_UP	50M-V_DN	100M-V_UP	100M-V_DN	0.9G-V_UP	0.9G-V_DN
-50	0.0098	2.1908	0.0105	2.1861	0.0098	2.1908
-45	0.0112	2.1901	0.0121	2.1836	0.0113	2.1905
-40	0.0928	2.0283	0.08451	2.0461	0.0794	2.0536
-35	0.2059	1.8073	0.1956	1.8254	0.1958	1.8271
-30	0.3185	1.5864	0.3111	1.6011	0.3131	1.5972
-25	0.4298	1.3686	0.4279	1.3745	0.4284	1.3713
-20	0.5405	1.1512	0.5439	1.1452	0.5415	1.1497
-15	0.6542	0.9292	0.6639	0.9104	0.6536	0.9304
-10	0.7713	0.7001	0.7877	0.6679	0.7682	0.7067
-5	0.8953	0.4573	0.9132	0.4222	0.8918	0.4652
0	1.0039	0.2448	1.0165	0.2197	1.0048	0.2462
5	1.0652	0.1238	1.0722	0.1098	1.0498	0.1654

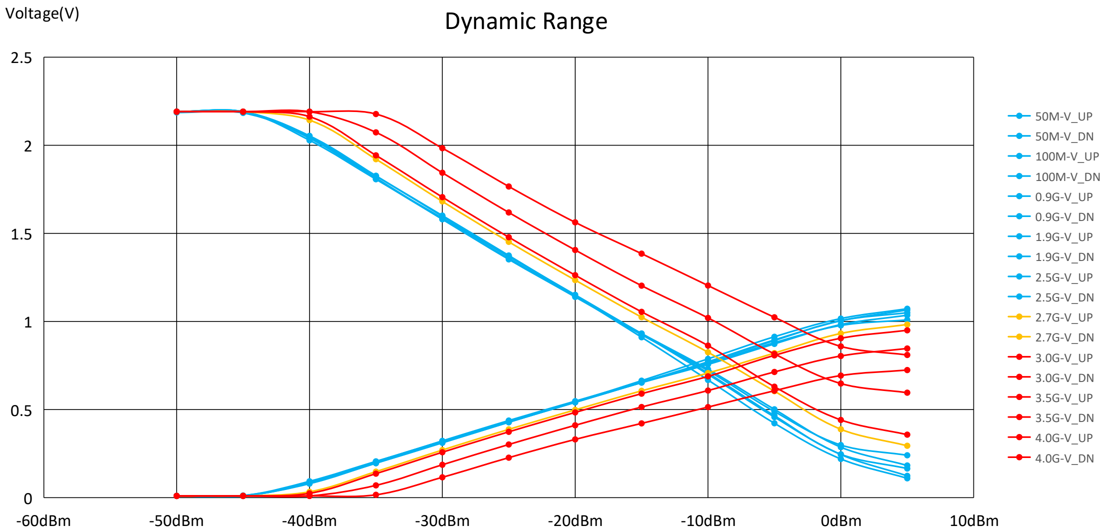
Input Frequency (Hz)	1.9G		2.5G		2.7G	
Input Power (dBm)	1.9G-V_UP	1.9G-V_DN	2.5G-V_UP	2.5G-V_DN	2.7G-V_UP	2.7G-V_DN
-50	0.0098	2.1908	0.0098	2.1908	0.0097	2.1905
-45	0.0094	2.1904	0.0099	2.1907	0.0098	2.1905
-40	0.0864	2.0403	0.0825	2.0496	0.0331	2.1429
-35	0.2047	1.8088	0.2022	1.8144	0.1476	1.9211
-30	0.3213	1.5805	0.3222	1.5801	0.2702	1.6814
-25	0.4351	1.3580	0.4377	1.3524	0.3875	1.4519
-20	0.5435	1.1452	0.5476	1.1393	0.4982	1.2348
-15	0.6528	0.9318	0.6568	0.9248	0.6063	1.0243
-10	0.7563	0.7289	0.7613	0.7205	0.7072	0.8252
-5	0.8726	0.5014	0.8797	0.4888	0.8205	0.6044
0	0.9824	0.2865	0.9773	0.2987	0.9319	0.3881
5	1.0353	0.1826	1.0089	0.2405	0.9827	0.2945

Input Frequency (Hz)	3.0G		3.5G		4.0G	
Input Power (dBm)	3.0G-V_UP	3.0G-V_DN	3.5G-V_UP	3.5G-V_DN	4.0G-V_UP	4.0G-V_DN
-50	0.0097	2.1908	0.0097	2.1908	0.0097	2.1908
-45	0.0098	2.1907	0.0098	2.1907	0.0097	2.1908
-40	0.0244	2.1625	0.0098	2.1906	0.0097	2.1908
-35	0.1362	1.9429	0.0697	2.0733	0.0161	2.1774
-30	0.2577	1.7057	0.1866	1.8441	0.1155	1.9835
-25	0.3736	1.4783	0.3017	1.6187	0.2269	1.7661
-20	0.4838	1.2627	0.4106	1.4056	0.3306	1.5627
-15	0.5902	1.0546	0.5144	1.2032	0.4215	1.3849
-10	0.6884	0.8630	0.6079	1.0202	0.5140	1.2040
-5	0.8076	0.6298	0.7134	0.8158	0.6068	1.0237
0	0.9047	0.4411	0.8040	0.6477	0.6929	0.8586
5	0.9499	0.3576	0.8466	0.5958	0.7242	0.8099

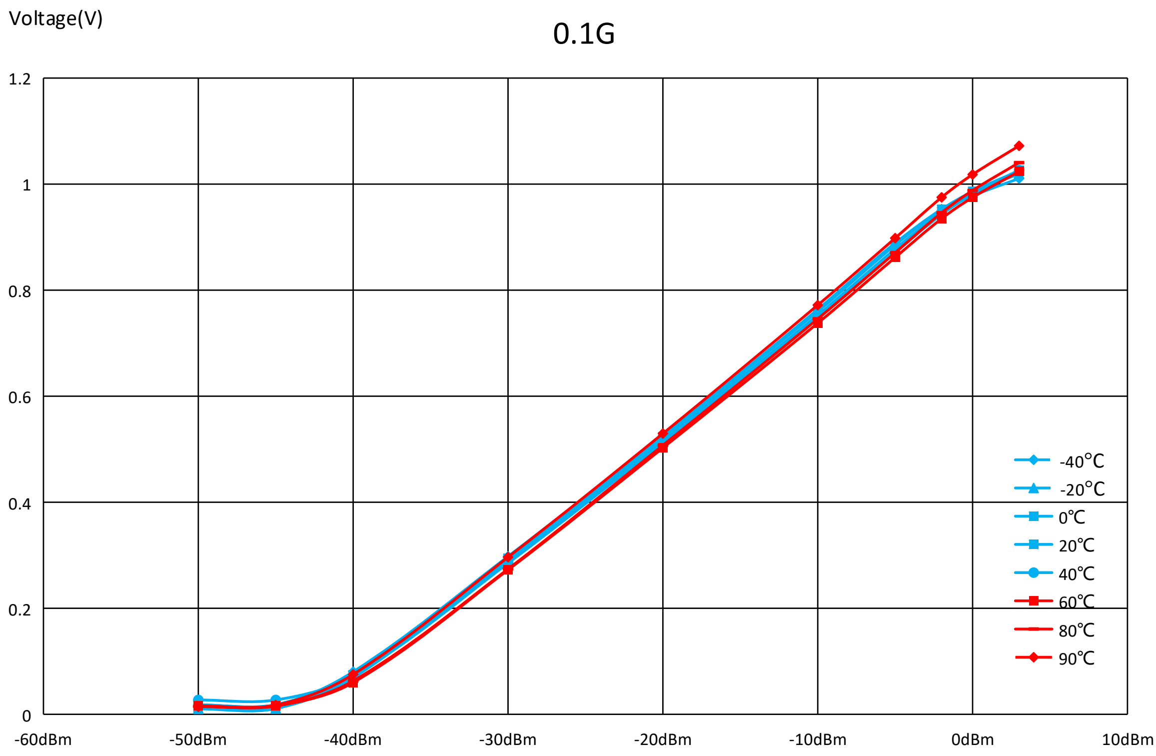
TYPICAL CHARACTERISTICS CURVE



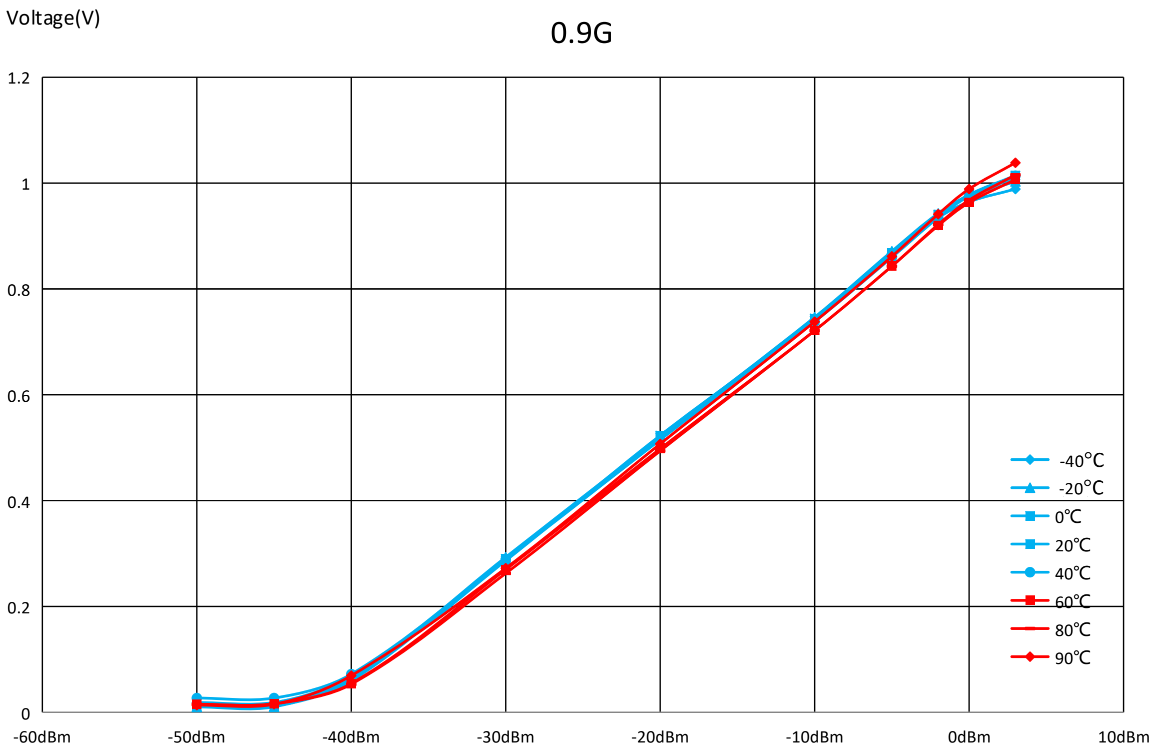
V_UP VS. Input Signal Power, Input Signal Frequency in Typical Conditions



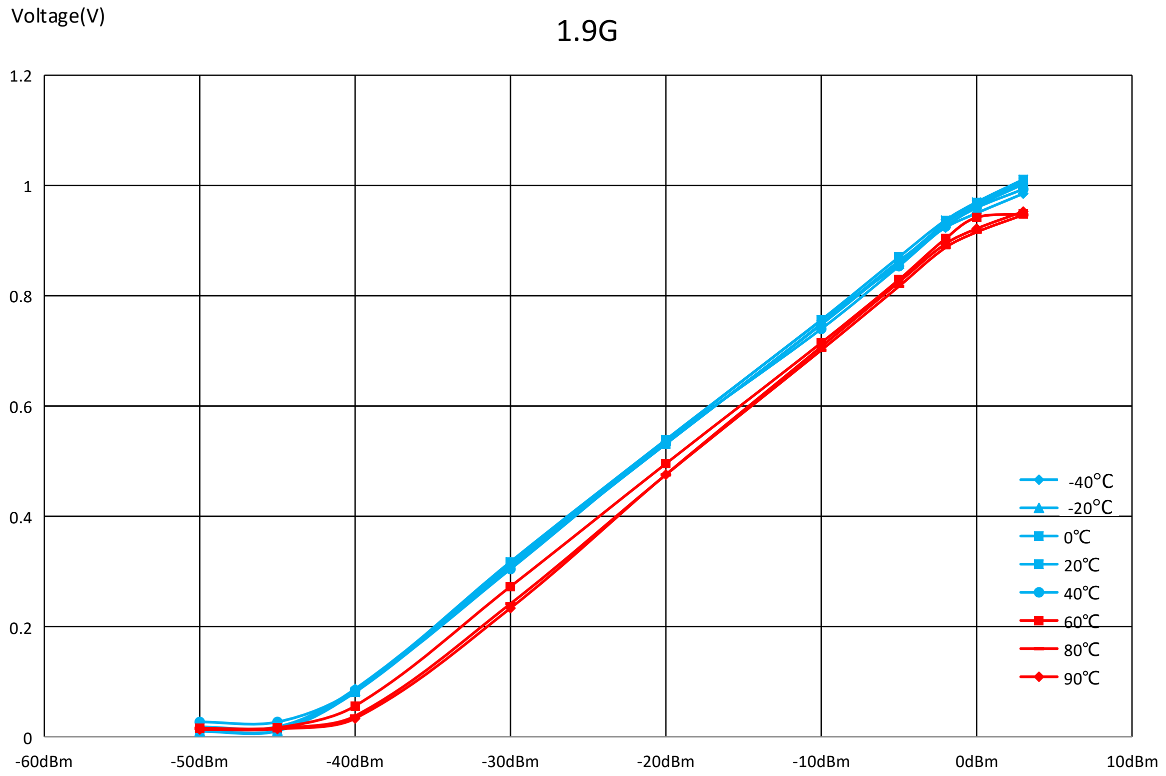
V_UP and V_DN VS. Input Signal Power, Input Signal Frequency in Typical Conditions



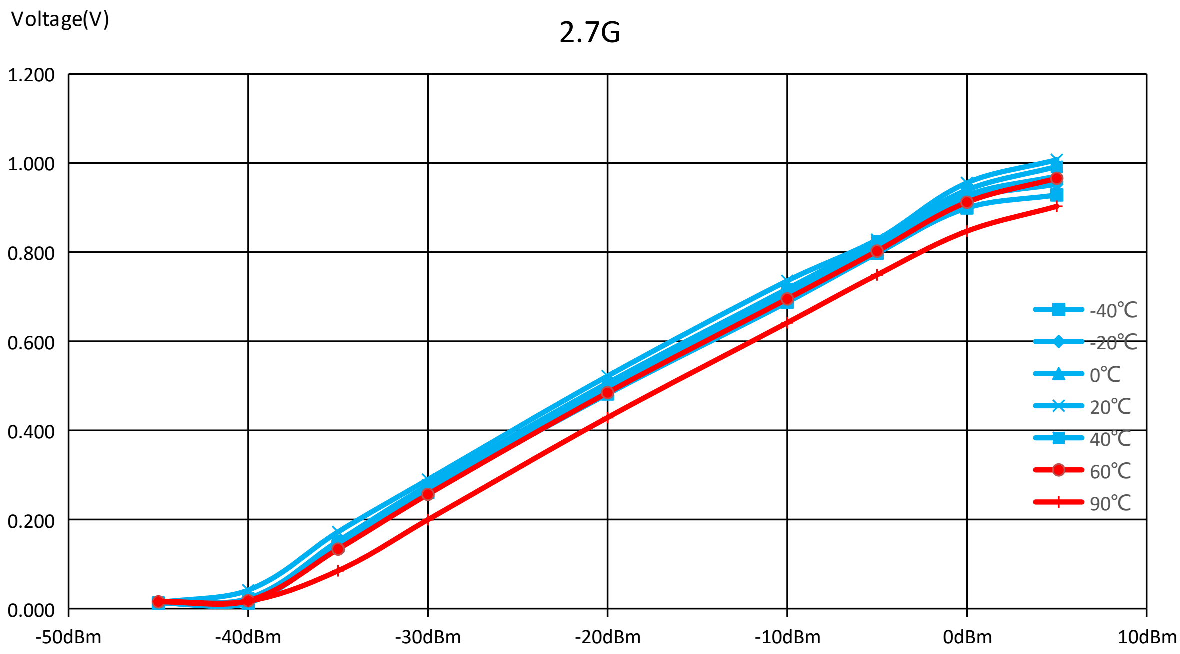
V_UP VS. Input Signal Power with Temperature at 3.3V, 0.1GHz



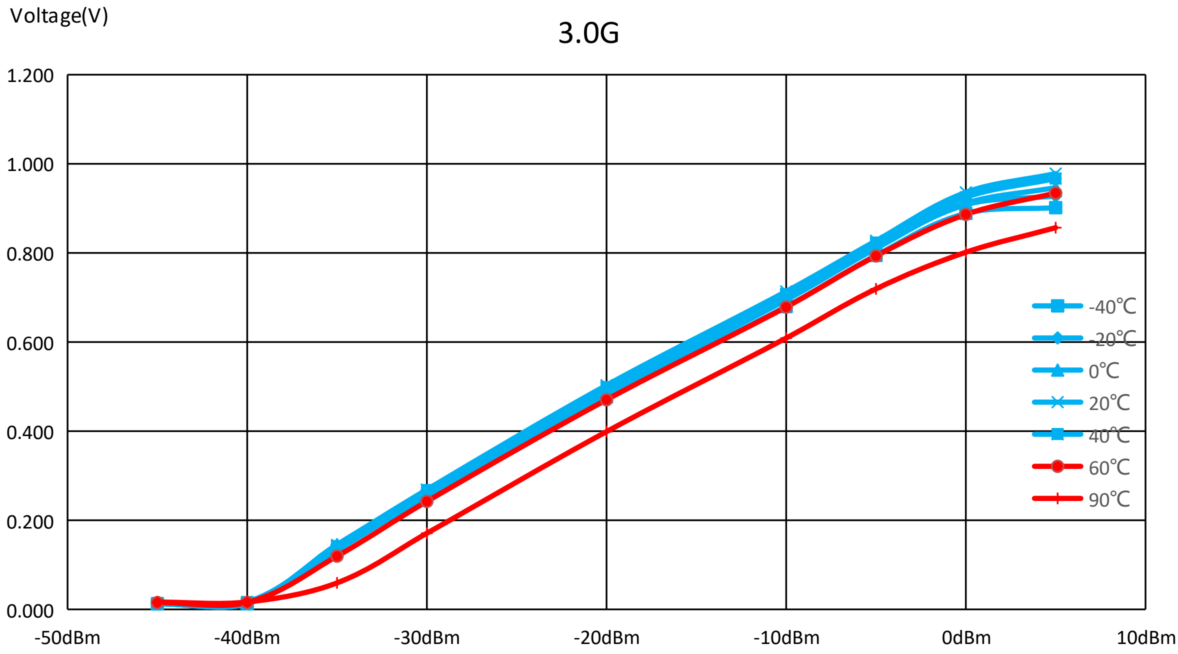
V_UP VS. Input Signal Power with Temperature at 3.3V, 0.9GHz



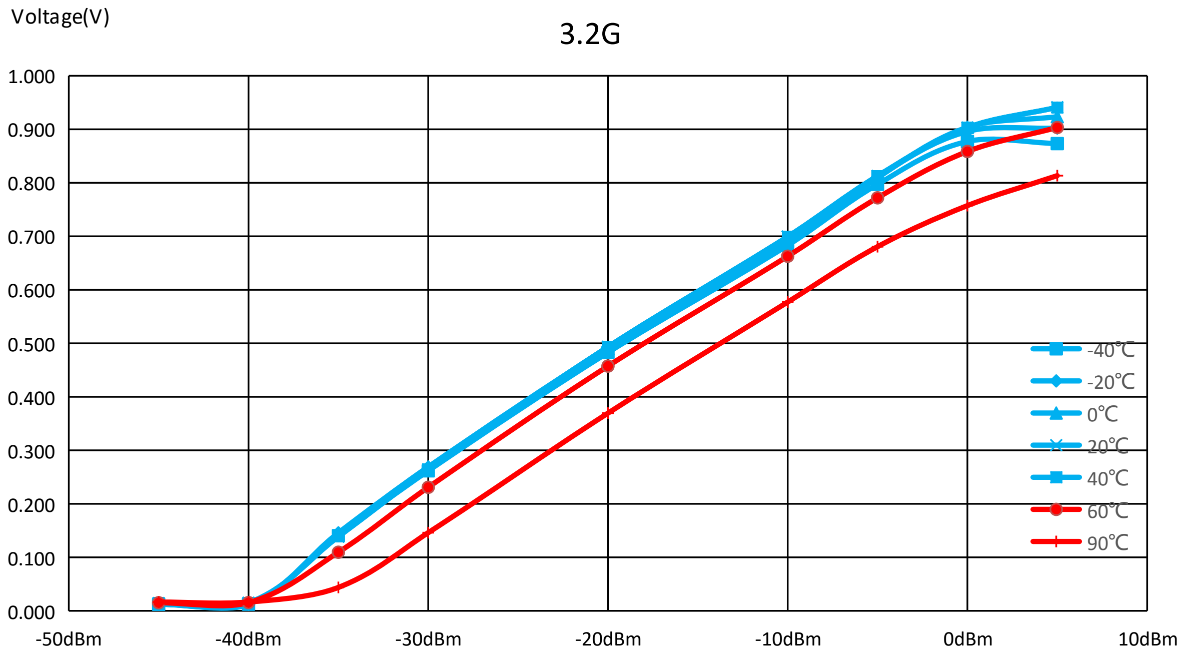
V_UP VS. Input Signal Power with Temperature at 3.3V, 1.9GHz



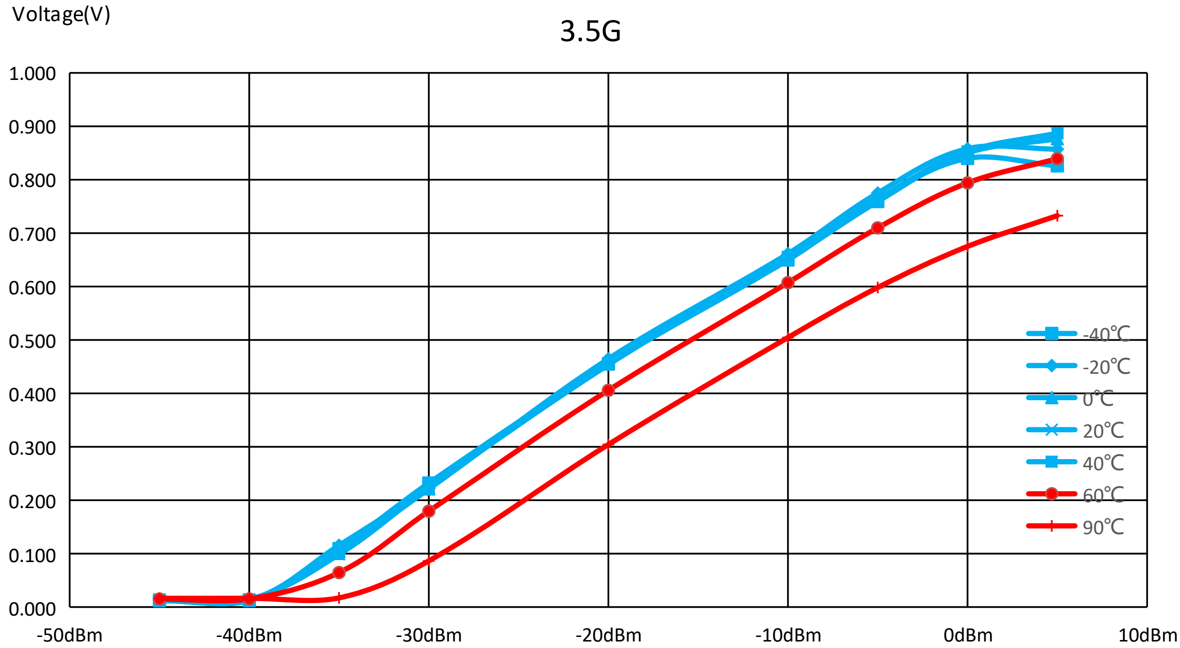
V_UP VS. Input Signal Power with Temperature at 3.3V, 2.7GHz



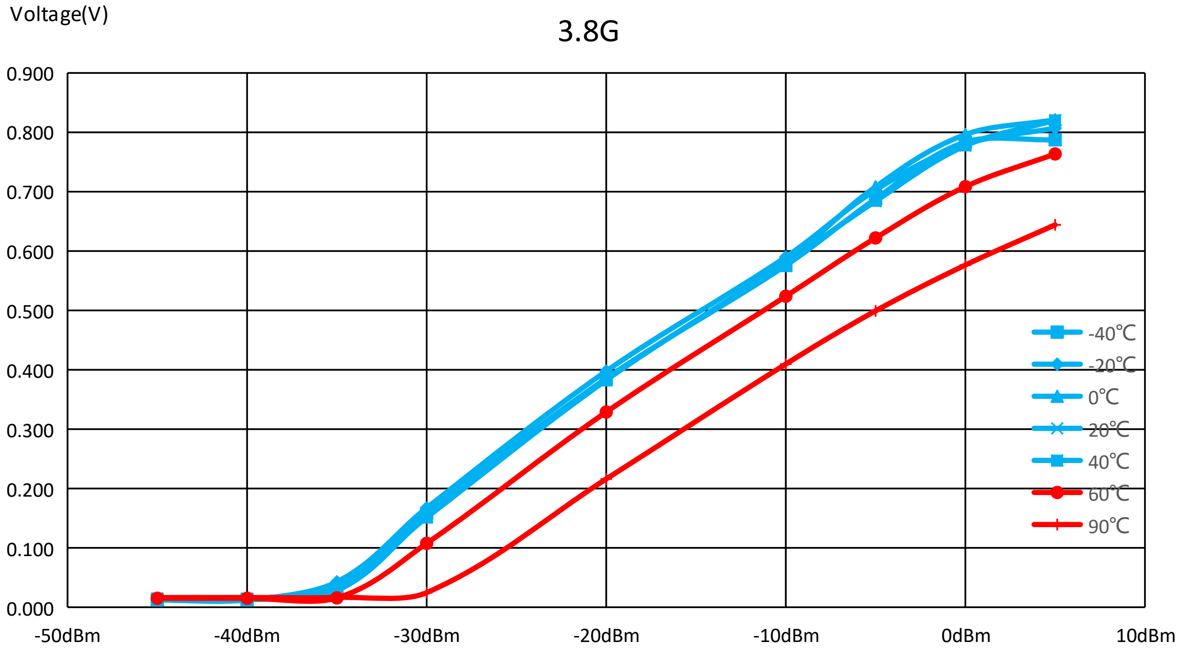
V_UP VS. Input Signal Power with Temperature at 3.3V, 3.0GHz



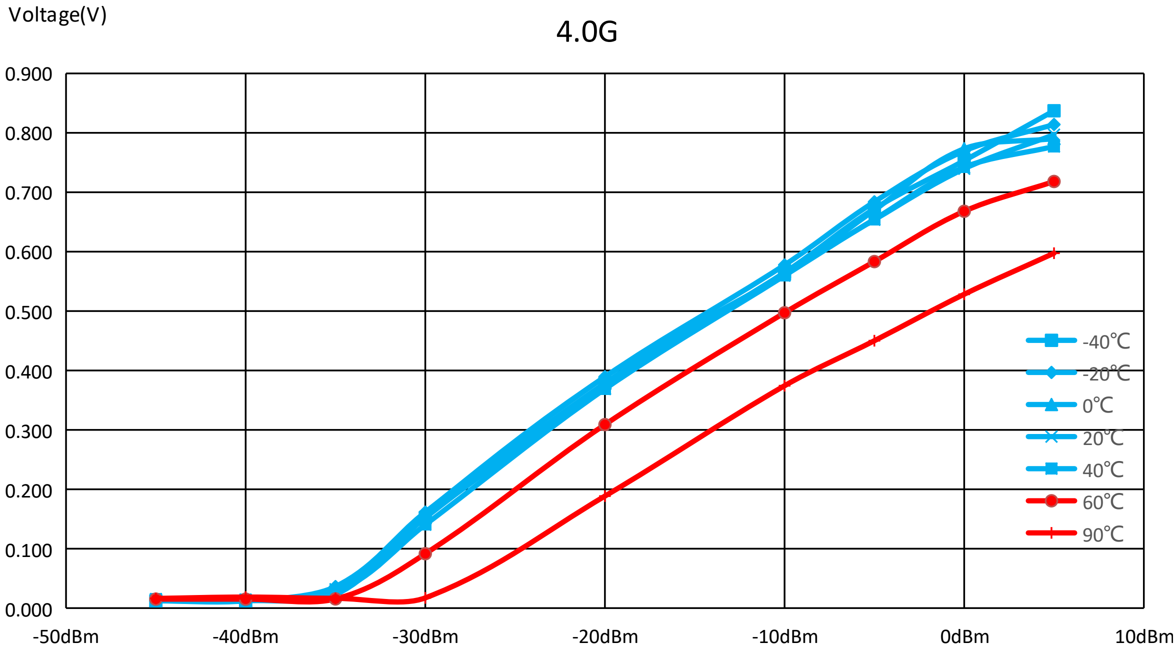
V_UP VS. Input Signal Power with Temperature at 3.3V, 3.2GHz



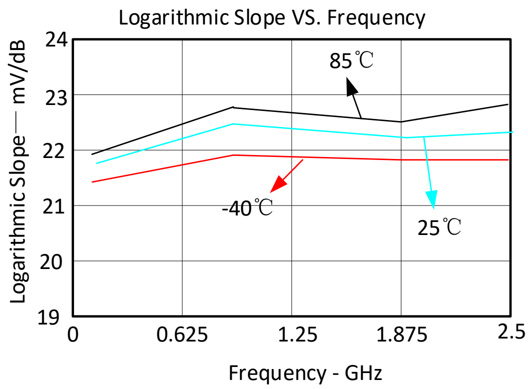
V_UP VS. Input Signal Power with Temperature at 3.3V, 3.5GHz

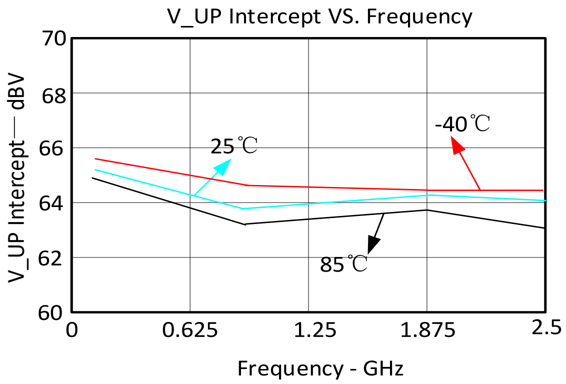


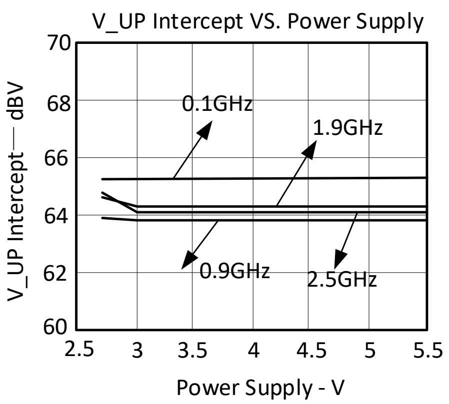
V_UP VS. Input Signal Power with Temperature at 3.3V, 3.8GHz

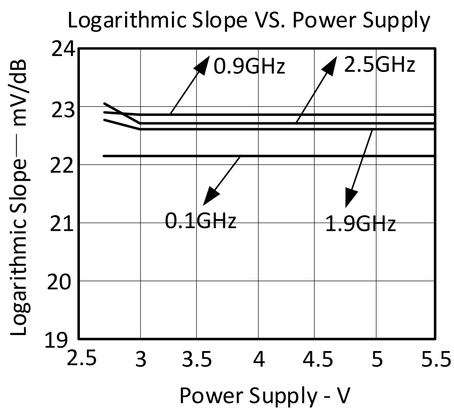


V_UP VS. Input Signal Power with Temperature at 3.3V, 4.0GHz

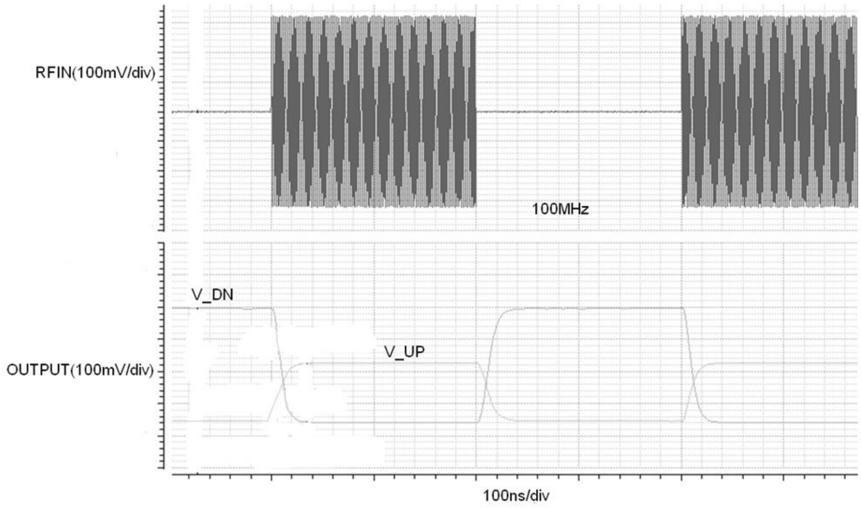








V_UP and V_DN Response Time: from -40dBm to 0dBm



FUNCTION DESCRIPTION

In order to easy to understand and calculate, logarithmic amplifier is often expressed as follows:

$$V\_UP = V_{Slope} \cdot log\left(\frac{V_{IN}}{V_X}\right)$$

V_{Slope} - Logarithmic Slope

V_X - Logarithmic Intercept

V_{IN} - Input Voltage

V_UP -Signal Strength Indication Output Voltage

Replacing input voltage with power, the equation can be further rewritten as:

$$V\_UP = V_{SLOPE} \cdot (P_{IN} - P_O)$$

This formula is also the bias for calculating theoretical output.

Where, V_{SLOPE} is the logarithmic slope, P_{IN} is the input power (@50Ω, dBm), P_O is the logarithmic intercept. V_{SLOPE} and P_O are constants, output voltage and input signal power(dBm) are linear relationship.

The factual error is defined as the difference between factual output and theoretical output.

$$Error(dB) = \frac{V\_UP - V_{slope} \times (P_{IN} - P_O)}{V_{slope}}$$

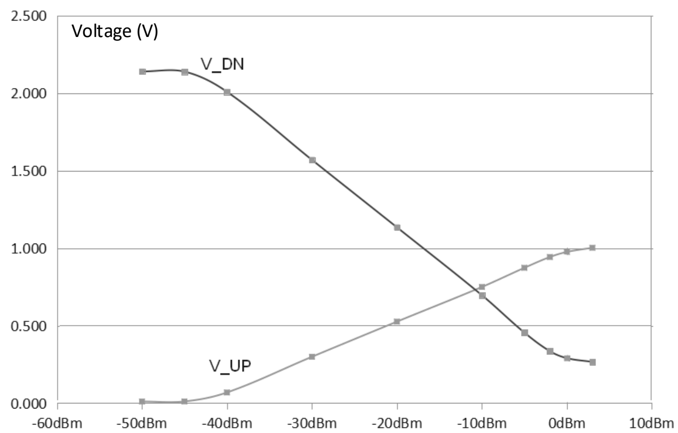
dBV can be used as a unit instead of dBm. Because dBV compression is fixed without depending on terminal impedance. But dBm depends on terminal load impedance. Take the root-mean-224mv sine wave as an example, it is expressed as fixed -13dBV, which corresponds to 0dBm@50Ω. In specified 50Ω system，0dBV=+13dBm.

The MS2351M/MS2351D also includes a reverse amplification output function, which can be used in control mode. Most power amplifiers need gain control bias circuit that must be able to change from a large positive value to ground when the power output requirement is reduced. V_DN pin of the MS2351M/MS2351D can generate this control voltage. The voltage not only has the opposite polarity to V_UP, but also must have certain DC offset to determine the maximum positive value when input signal power is minimum.

The initial value of V_DN is about 2.2V and decreases by twice the V_UP slope.

The relationship between V_DN and V_UP is as follows:

$$V\_DN = 2.20 - 2 \times V\_UP$$



The Relationship between V_DN and V_UP

APPLICATIONS

1. Measurement Mode

Figure 1 shows the connection relationship in measurement mode. A 0.1μF decoupling capacitor should be connected close to VPOS pin. If necessary, a small resistor or a inductor can be connected in series between external power supply and VPOS pin to further reduce power noise. When in normal operating mode, ENBL is connected to VPOS; when ENBL is connected to ground, the chip is shutdown.

When in measurement mode, VSET is connected to V_UP. This feedback path sets logarithmic slope to the usual value. At 1900MHz, the peak voltage ranges from -58dBV to -13dBV. Therefore, equivalent power ranges from -45dBm to 0dBm with using 50Ω termination.

V_DN is not usually used when in measurement mode.

Filter Capacitor

The video signal bandwidth of V_UP and V_DN is about 3.5MHz. In the sinusoidal signal application, when input signal frequency is much higher than 3.5MHz, there is no need to further filter the demodulation signal. When used in low-frequency carrier amplitude modulation application, the low-pass angle frequency needs to be reduced by increasing external capacitor C_F (Figure 1). The video signal bandwidth is calculated as follows:

$$BW = \frac{1}{2 \times \pi \times 4.4k\Omega \times (10pF + C_F)}$$

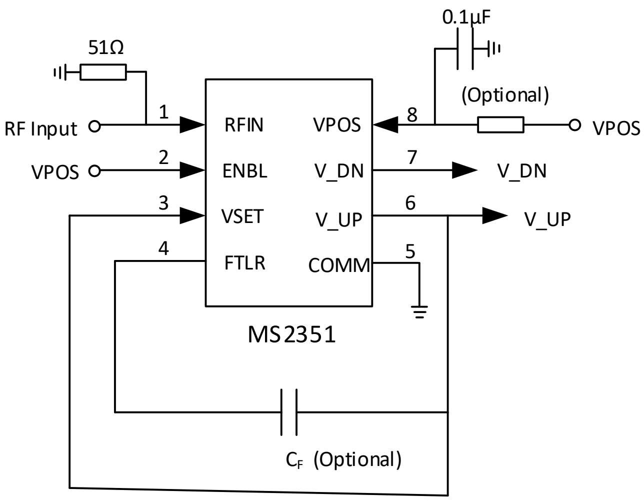


Figure 1. Basic Connections in Measurement Mode

2. Control Mode

Figure 2 shows the basic connections in control mode. Figure 3 shows typical application. The feedback from V_UP to VSET is broken, and the desired voltage is applied to VSET pin. When the signal power of RFIN is less than VSET voltage, V_DN would output high; when the signal power of RFIN is slightly higher than VSET voltage, V_DN would rapidly decrease to close to ground. However, in this closed loop, the reduction of V_DN causes the power amplifier to reduce its output. Finally, the actual signal power of input terminal of the MS2351M/MS2351D reaches a balance with the voltage required by VSET pin. The relationship between input signal and the voltage set by VSET pin follows the transfer function of the MS2351 (input signal amplitude VS. V_UP).

For example, when VSET=1, 0dBm input signal power on RFIN is required. Correspondingly, the output power of power amplifier should be more than 0dBm due to the attenuation of antenna coupler.

As shown in Figure 3, when the MS2351M/MS2351D is applied in the control loop of power amplifier, V_UP can set needed response time by optional C_F. The transient response is determined by filter capacitor C_F. When C_F is large, this loop is stable unconditionally, but the response is slower. The minimum capacitance C_F should be used so that the loop can be stabilized. And it is needed to control function attenuation for specific power amplifier. Because of the unavoidable nonlinearity, the choice of C_F must consider the worst case, which usually occurs at the minimum output of the power amplifier. Usually, resistor can be connected in series with C_F to increase a zero point to improve the dynamic characteristics of the loop.

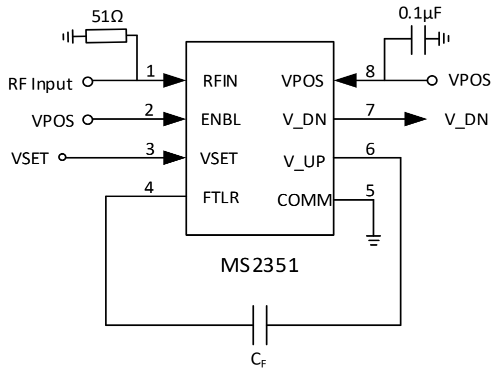


Figure 2. Control Mode

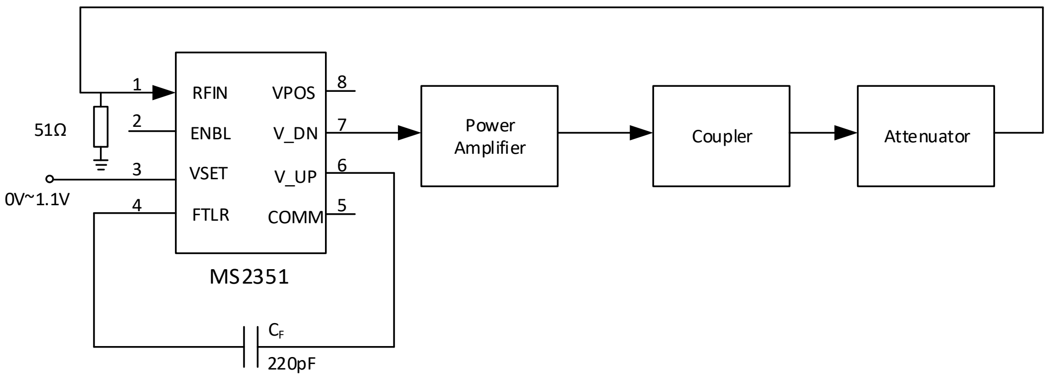


Figure 3. Typical Application in Control Mode

The voltage on VSET pin of the MS2351M/MS2351D ranges from 0V to 1.1V. Typically, it is driven by digital-to-analog converter (DAC). The voltage is compared with the input signal of the MS2351M/MS2351D. Any unbalance between VSET and RF input signal would be calibrated by V_DN (gain control pin of power amplifier is driven by V_DN).

Filter capacitor must be used to make the loop stable. The choice of C_F depends on gain control of power amplifier. But its frequency characteristic is very bad, so some tests and errors are unavoidable. In the example, 220pF capacitance gives enough speed for this loop so as to meet the slot time requirement while its response is still stable.

3. Input Coupling Options

The MS2351M/MS2351D has an internal input coupling capacitor without external AC coupling capacitor. Figure 4 shows match networks of narrowband, broadband and attenuator. Smith Chart can be used in actual need for match to ensure the best component value.

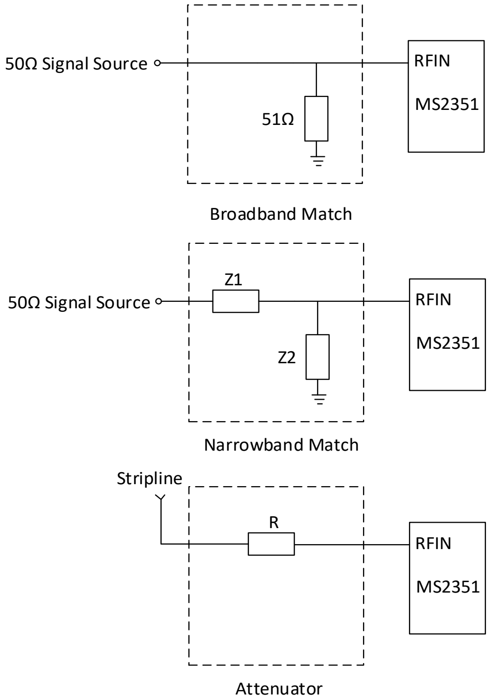


Figure 4 . Input Match and Connections

4. Increase Logarithmic Slope in Measurement Mode

The logarithmic slope can be increased by the connection method in Figure 5 to meet the maximum V_UP value, but available dynamic range will be reduced accordingly. In fact, the application environment should be considered.

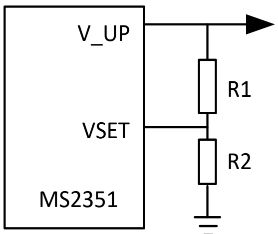


Figure 5. Increase Output Logarithmic Slope

The value of R1/R2 is determined by the following formula:

$$\frac{R1}{R2} = \frac{Slope_{new}}{Slope_{old}} - 1$$

If two equivalent resistors are used (both resistance values should be larger than 5kΩ), the logarithmic slope becomes twice times the origin value.

5. Evaluation Board

Figure 6 shows the evaluation board of the MS2351M/MS2351D. The circuit is powered by single 2.7V~5.5V power supply, which is decoupled by 0.1μF capacitance. For further decoupling, a resistor R5 or an inductor can be added.

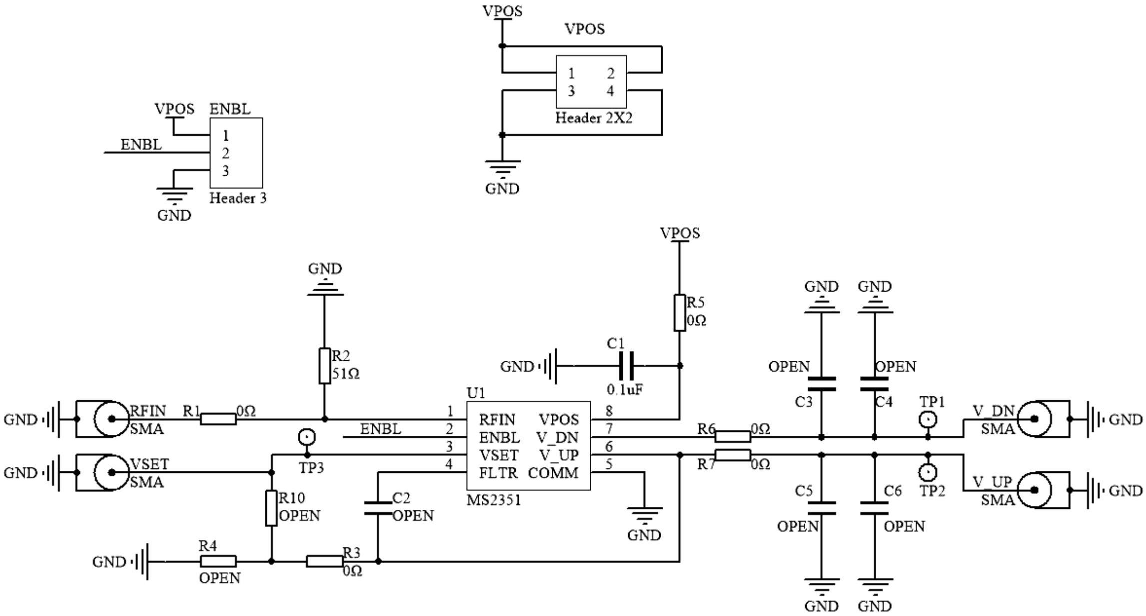
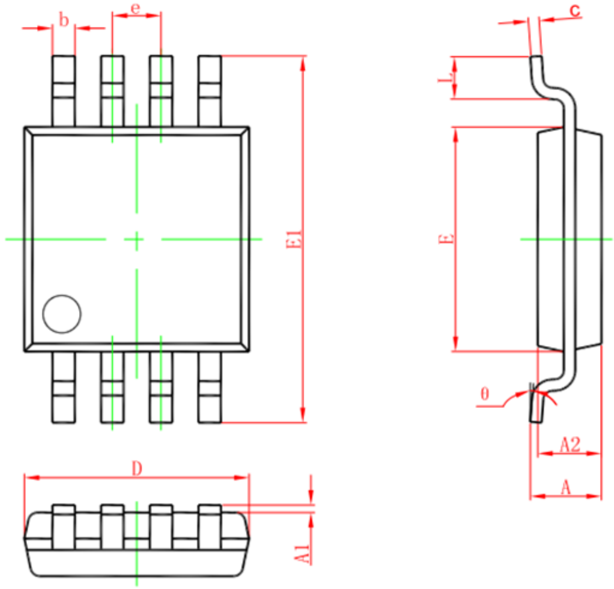


Figure 6. The MS2351M/MS2351D Evaluation Board

PACKAGE OUTLINE DIMENSIONS

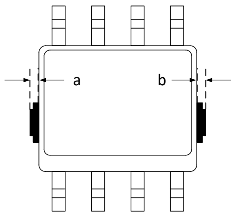
MSOP8



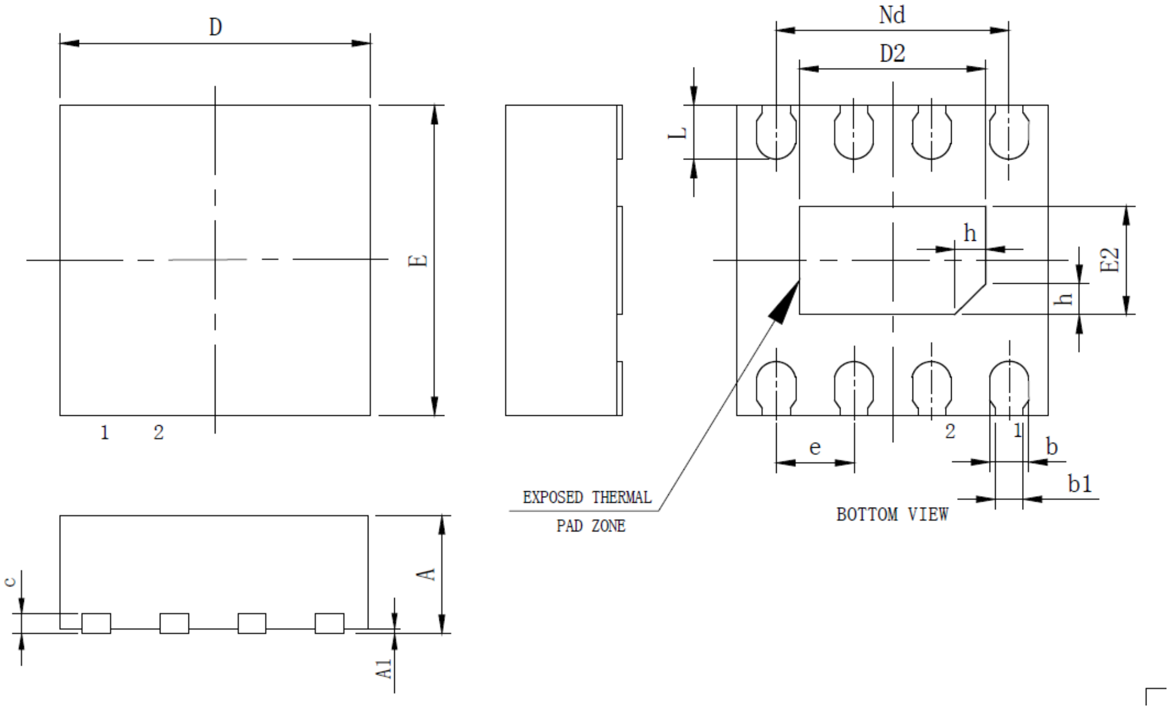
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650BSC		0.026BSC	
L	0.400	0.800	0.016	0.031
θ	0º	6º	0º	6º

Note: In addition to the package size, a and b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.



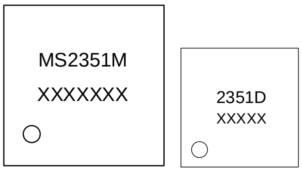
DFN8



Symbol	Dimensions in Millimeters		
	Min	Norm	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
b1	0.18 REF		
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D2	1.10	1.20	1.30
e	0.50 BSC		
Nd	1.50 BSC		
E	1.90	2.00	2.10
E2	0.60	0.70	0.80
L	0.30	0.35	0.40
h	0.15	0.20	0.25

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS2351M, 2351D

Product Code: XXXXXXX, XXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS2351M	MSOP8	3000	1	3000	8	24000
MS2351D	DFN8	3000	10	30000	4	120000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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