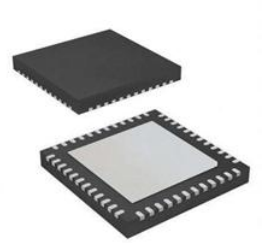
High-precision Time Measurement SOC

PRODUCT DESCRIPTION

The MS616F22 is a high-precision TDC SOC, built in high-speed TDC unit and 16-bit RISC MCU with low power dissipation. TDC unit integrates analog comparator, analog switch, Schmitt trigger, thus greatly simplifying peripheral circuit. In addition, internal first wave detection function improves anti-interference ability. The programmable range of internal comparator is ±35mV. 16-bit RISC MCU with low power dissipation provides several peripheral modules, such as 64K Flash, 2K RAM, ADC12, TimerA, TimerB, UART0, UART1 and so on. Unique processing architecture with low power dissipation makes the total system consume under 5uA.



FEATURES

MCU Part

Inner-core Circuit:

- 16-bit RISC Architecture, 125ns Instruction Cycle
- 62KB+128B Flash
- 2KB RAM
- Five Operating Modes Set by Software and Only Four Awaken

Clock Circuit:

- Built-in FLL Clock Module, Maximum Frequency Multiplication to 4M
- Provide MCLK/SMLK/ALK Clock Output
- 32.768kHz External Input Clock

External Module:

- Three ADC12 Input Terminals
- 15 GPIO, 11 Receiving Interrupt
- Two Timer Modules
- Two Independent UART Interfaces
- One online Programmable JTAG Interface
- One Offline Programmable BSL Interface

TDC Part

Measurement Range 1:

- 75ps Dual-channel Single Precision Mode
  37ps Single-channel Dual Precision Mode
- Measurement Range, 3.5ns(0ns) to 2.5μs
- 20ns Minimum Pulse Interval,
  Receive Four Pulses at most

Measurement Range 2：

- 37ps Dual Precision Mode,
  19ps Quadruple Precision Mode
- Measurement Range, 500ns to 4ms
  (on 4M high-speed clock)
- Measurable Three Pulses,
  Process Three Data Automatically

Analog Input Circuit:

- Stable Chopping, Low Drift Comparator, with Programmable Offset Voltage, ±35mV
- First Wave Detection,
  Measure Pulse Width
- External Circuit only with Two Resistors and Two Capacitors

Temperature Measurement Unit:

- Two or Four Temperature Sensors, PT500/PT1000or Higher
- Internal Schmitt Trigger

General:

- Pulse Generator, 127 Pulses at most
- Rising or Falling Edge Triggering Measurement
- High-precision STOP Shield Window

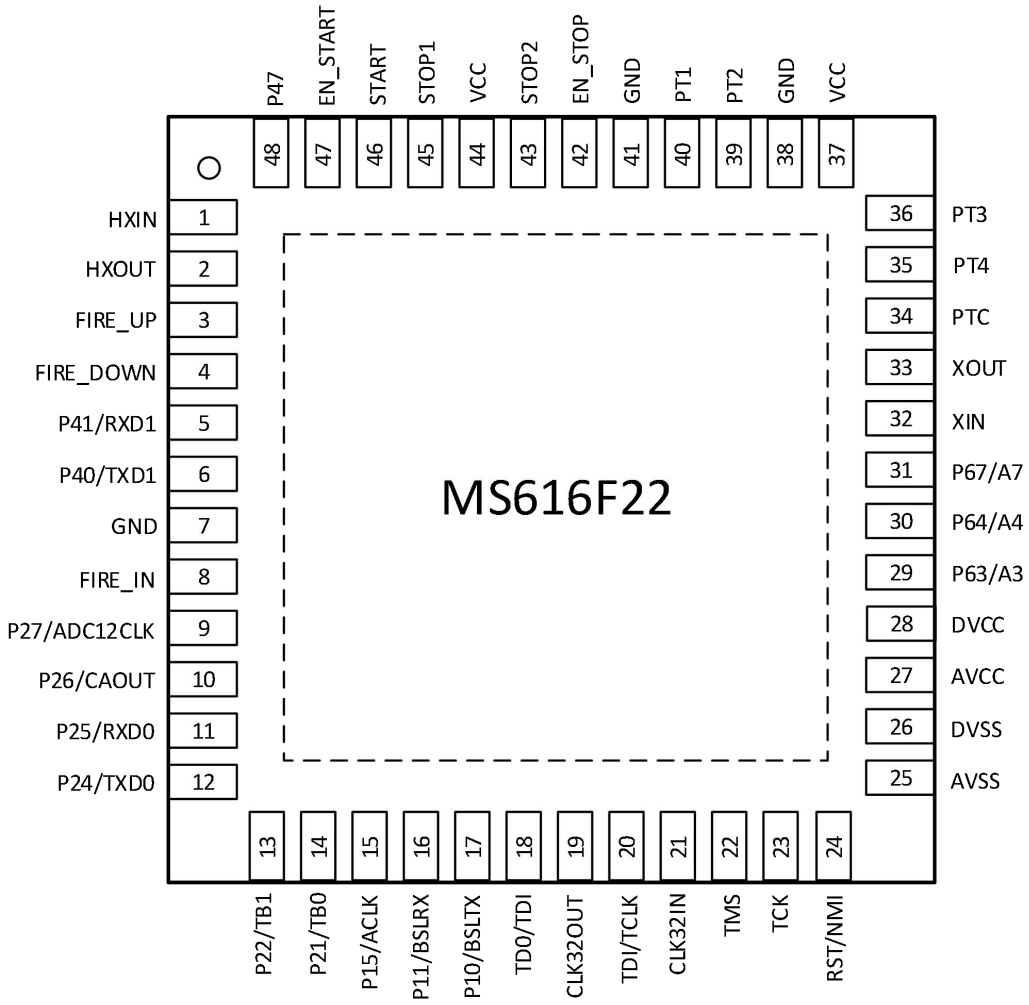
APPLICATIONS

- Ultrasonic Wave Measurement
- Laser Ranging

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS616F22	QFN48	MS616F22

PIN CONFIGURATION



PIN DESCRIPTION

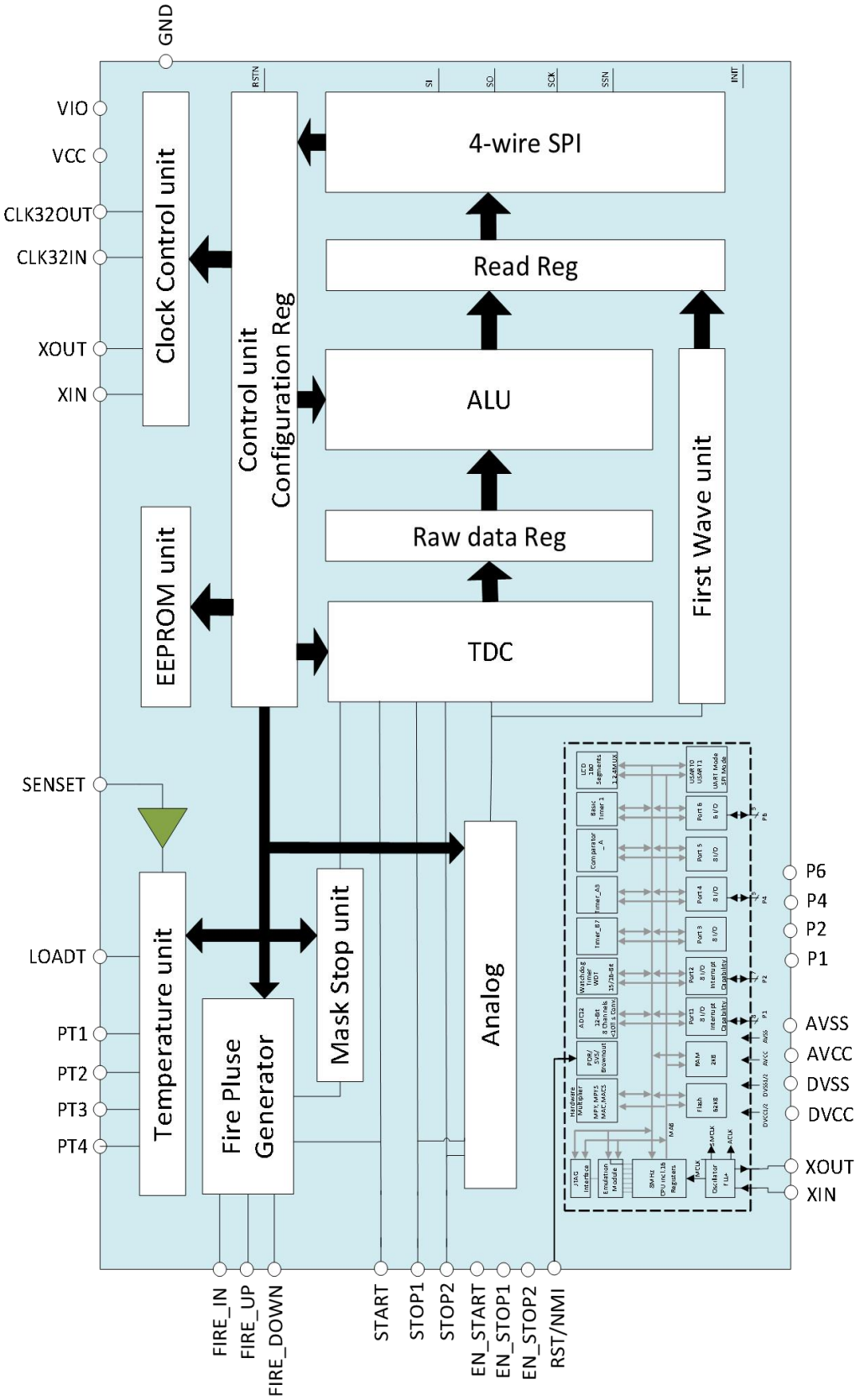
Pin	Name	Type	Description
1	HXIN	I	TDC High-speed Crystal Drive Input
2	HXOUT	O	TDC High-speed Crystal Drive Output
3	FIRE_UP	O	Pulse Generator Output 1
4	FIRE_DOWN	O	Pulse Generator Output 2
5	P41/RXD1	I/O	General Digital I/O Interface / In UART Mode, USART1 Receiving Data Input
6	P40/TXD1	O	General Digital I/O Interface / In UART Mode, USART1 Transmitting Data Output
7	GND	-	TDC Ground
8	FIRE_IN	I	“Sound Circulation Method” Signal Input Terminal
9	P27/ADC12CLK	I/O	General Digital I/O Interface / 12-bit ADC Conversion Clock
10	P26/CAOUT	I/O	General Digital I/O Interface / Comparator A Output
11	P25/RXD0	I/O	General Digital I/O Interface / In UART Mode, USART0 Receiving Data Input
12	P24/TXD0	I/O	General Digital I/O Interface / In UART Mode, USART0 Transmitting Data Output
13	P22/TB1	I/O	General Digital I/O Interface / Capture Input of Timer_B CCR1 : CCI1A/CCI1B
14	P21/TB0	I/O	General Digital I/O Interface / Capture Input of Timer_B CCR0 : CCI0A/CCI0B
15	P15/ACLK	I/O	General Digital I/O Interface / Auxiliary Clock ACLK Output
16	P11/BSLRX	I/O	General Digital I/O Interface / Capture Input of Timer_A: CCI0B / BSL Transmission
17	P10/BSLTX	I/O	General Digital I/O Interface / Capture Input of Timer_A: CCI0A / BSL Transmission
18	TDO/TDI	I/O	Test Data Output or Input Terminal of Programming Data
19	CLK32OUT	O	TDC 32 kHz Clock Output
20	TDI/TCLK	I	Test Data Input or Test Clock Input, Protection Fuse Connected to TDI / TCLK
21	CLK32IN	I	TDC 32 kHz Clock Input
22	TMS	I	Test Mode Selection. TMS is used as input terminal for program and test
23	TCK	I	Test Clock. TCK is clock input terminal for program and test

Pin	Name	Type	Description
24	RST/NMI	I	Reset Input or Unshielded Interrupt Input
25	AVSS	-	MCU Analog Ground
26	DVSS	-	MCU Digital Ground
27	AVCC	-	MCU Analog Power Supply
28	DVCC	-	MCU Digital Power Supply
29	P63/A3	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A3
30	P64/A4	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A4
31	P67/A7	I/O	General Digital I/O Interface / 12-bit ADC Analog Input A7
32	XIN	I	MCU Low-speed Crystal XT1, Input Terminal
33	XOUT	O	MCU Low-speed Crystal XT1, Output Terminal
34	PTC	O	Temperature Measurement Capacitance Connection Terminal
35	PT4	O	Temperature Measurement Terminal 4
36	PT3	O	Temperature Measurement Terminal 3
37	VCC	-	TDC Power Supply
38	GND	-	TDC Ground
39	PT2	O	Temperature Measurement Terminal 2
40	PT1	O	Temperature Measurement Terminal 1
41	GND	-	TDC Ground
42	EN_STOP	I	Stop Channel Enable Terminal, Active High
43	STOP2	I	Input Terminal for Stop Channel 2
44	VCC	-	TDC Power Supply
45	STOP1	I	Input Terminal for Stop Channel 1
46	START	I	Start Channel Input Terminal
47	EN_START	I	Start Channel Enable Terminal, Active High or Signal Output Terminal
48	P47	I/O	General Digital I/O Interface

Note: Interconnection between MCU and TDC

MCU	TDC	Description
P12	RSTN	MCU P12 Controlling TDC RSTN, MCU Set as Output Terminal
P13	SO	MCU P13 Receiving TDC SO Data, MCU Set as Input Terminal
P14	SI	MCU P14 Transmitting Data to TDC SI, MCU Set as Output Terminal
P16	SCK	MCU P16 Transmitting Clock to TDC SCK, MCU Set as Output Terminal
P17	SSN	MCU P17 Controlling TDC SSN, MCU Set as Output Terminal
P20	INIT	MCU P13 Receiving TDC INIT Signal, MCU Set as Input Terminal

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Range	Unit
Voltage Difference, Vcc to Vss	-0.3 ~ +4.1	V
Input Voltage	-0.3 ~ VCC+0.3	V
Device Diode Current	±2	mA
Operating Temperature (No Programming)	-55 ~ 150	°C
Storage Temperature (Programming)	-40 ~ 80	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
MCU Power Supply	AVCC DVCC	Program executing	1.8		3.6	V
		Program executing and SVS enabled, PORON=1	2.0		3.6	V
		Flash Programming	2.7		3.6	V
MCU Power Supply	V_{SS}		0		0	V
TDC Power Supply	VCC		2.5		3.6	V
Operating Temperature	T_A		-40		85	°C
LFXT1 Crystal Frequency	f_{LFXT1}	XTS_FLL=0, Quartz Oscillator		32.768		kHz
		XTS_FLL=1, Ceramic Oscillator	450		8000	kHz
		XTS_FLL=1, Crystal Oscillator	1000		8000	kHz
XT2 Crystal Frequency	f_{XT2}	Ceramic Oscillator	450		8000	kHz
		Crystal Oscillator	1000		8000	kHz
System Clock Frequency	f_{System}	Vcc=3.6V	DC		4	MHz

1. It's recommended to use the same power supply for AVCC and DVCC. The voltage difference between AVCC and DVCC can't exceed 0.3V.

2. When the power supply enough lows to trigger POR, the corresponding voltage is the minimum operating voltage. When the power supply increases to the value, which is equal to the minimum voltage value plus SVS hysteresis voltage, POR signal stops.

3. In LF mode, the LFXT1 oscillator needs to connect with one external quartz oscillator. When in XT1 mode, LFXT1 needs to connect with one ceramic or crystal oscillator.

ELECTRICAL CHARACTERISTICS

MCU Supply Current into AVCC + DVCC Except External Current

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Operation Mode (Note 1) $f_{MCLK}=f_{SMCLK}$=1MHz, f_{ACLK}=32768Hz XTS_FLL=0,SELM=(0,1)	I_{AM}	T_A=-40°C to 85°C	VCC=2.2V		280	350	μA
			VCC=3V		420	560	
Low Power Dissipation Mode (Note 1,4)	I_{LPM0}	T_A=-40°C to 85°C	VCC=2.2V		32	45	μA
			VCC=3V		55	70	
Low Power Dissipation Mode (Note 2,4) $f_{MCLK}=f_{SMCLK}$=0MHz f_{ACLK}=32768Hz, SCG=0	I_{LPM2}	T_A=-40°C to 85°C	VCC=2.2V		11	14	μA
			VCC=3V		17	22	
Low Power Dissipation Mode (Note 3,4) $f_{MCLK}=f_{SMCLK}$=0MHz f_{ACLK}=32768Hz, SCG=1	I_{LPM3}	T_A=-40°C	VCC=2.2V		1	1.5	μA
		T_A=25°C			1.1	1.5	
		T_A=60°C			2	3	
		T_A=85°C			3.5	6	
		T_A=-40°C	VCC=3V		1.8	2.2	μA
		T_A=25°C			1.6	1.9	
		T_A=60°C			2.5	3.5	
		T_A=85°C			4.2	7.5	
Low Power Dissipation Mode (Note 2,4) $f_{MCLK}=f_{SMCLK}$=0MHz f_{ACLK}=0Hz, SCG=1	I_{LPM4}	T_A=-40°C	VCC=2.2V		0.1	0.5	μA
		T_A=25°C			0.1	0.5	
		T_A=60°C			0.7	1.1	
		T_A=85°C			1.7	3	
		T_A=-40°C	VCC=3V		0.1	0.5	μA
		T_A=25°C			0.1	0.5	
		T_A=60°C			0.8	1.2	
		T_A=85°C			1.9	3.5	

Note:

1. Timer_B frequency is locked as $f_{DCOCLK}=f_{DCO}$=1MHz. All inputs are connected to 0V or VCC. All outputs have no source or reverse current.

2. All inputs are connected to 0V or VCC. All outputs have no source or reverse current.

3. All inputs are connected to 0V or VCC. All outputs have no source or reverse current. The current consumption of LPM3 is achieved by measuring the operating current of timer 1 and LCD (select ACLK). Comparator A and the current in SVS module would be described specially.

4. Including the current consumption in BROWNOUT module.

In operation mode, the relationship between consumption current and system frequency:

$$I_{AM} = I_{AM}\ [1\ MHz] \times f_{System}\ [MHz]$$

In operation mode, the relationship between consumption current and power supply:

$$I_{AM} = I_{AM\ [3\ V]} + 175\ \mu A/V \times (V_{CC} - 3\ V)$$

MCU Schmitt Trigger Input Terminal——P1,P2,P4,P6

Parameter	Symbol	Power Supply	Min	Typ	Max	Unit
Forward Input Threshold Voltage	V_{IT+}	2.2 V	1.1		1.5	V
		3 V	1.5		1.9	
Reverse Input Threshold Voltage	V_{IT-}	2.2 V	0.4		0.9	V
		3 V	0.9		1.3	
Input Hysteresis (V_{IT+} - V_{IT-})	V_{hys}	2.2 V	0.3		1.1	V
		3 V	0.5		1	

MCU Standard Input Terminal——RST/NMI,JTAG(TCK,TMS,TDI,TDO)

Parameter	Symbol	Power Supply	Min	Typ	Max	Unit
Low Level Input Voltage	V_{IL}	2.2V/3V	VSS		VSS+0.6	V
High Level Input Voltage	V_{IH}		0.8Vcc		VCC	V

MCU Input Terminal——Px.x,TAx,TBx

Parameter	Symbol	Condition	Power Supply	Min	Typ	Max	Unit
External Interrupt Timing	t(int)	Terminal P1,P2: P1.x to P2.x External triggering signal is interrupt flag (Note 1)	2.2V/3V	1.5			cycle
			2.2V	62			ns
			3V	50			
Timer_A, Timer_B Capture Time	t(cap)	TA0,TA1,TA2 TB0,TB1,TB2,TB3,TB4, TB5,TB6	2.2V	62			ns
			3V	62			
Clock Frequency applied to Timer_A/B	f(TAext)	TACLK, TBCLK, INCLK: t(H) = t(L)	2.2V			8	MHz
	f(TBext)		3V			10	
Clock Frequency of Timer_A/B	f(TAint)	Select SMCLK or ACLK	2.2V			8	MHz
	f(TBint)		3V			10	

Note 1: When external signal sets interrupt flag, the corresponding $t_{(int)}$ is even with trigger signal shorter than $t_{(int)}$. The clock cycle and time parameter must be simultaneously met to ensure interrupt flag setting. $t_{(int}$ is measured referred to MCLK cycle.

MCU Leakage Current (Note 1,2)

Parameter	Symbol	Condition	Power Supply	Min	Max	Unit
Leakage Current	I_{lkg}	Px Terminal： $V_{(Px.x)}$	2.2/3V		50	nA

Note :

1. Leakage current is measured when VSS or VCC is applied to relative pins, unless otherwise noted.
2. The terminal pin must be set as input , and couldn't have any pull-up or pull-down resistor.

MCU Output Terminal——P1,P2,P4,P6

Parameter	Symbol	Condition	Power Supply	Min	Typ	Max	Unit
High Level Output Voltage	V_{OH}	$I_{OH(max)}$ =-1.5 mA (Note 1)	2.2V	VCC-0.25		VCC	V
		$I_{OH(max)}$ =-6 mA (Note 2)	2.2V	VCC-0.6		VCC	
		$I_{OH(max)}$ =-1.5 mA (Note 1)	3V	VCC-0.25		VCC	
		$I_{OH(max)}$ =-6 mA (Note 2)	3V	VCC-0.6		VCC	
Low Level Output Voltage	V_{OL}	$I_{OL(max)}$=1.5 mA (Note 1)	2.2V	VSS		VSS+0.25	V
		$I_{OL(max)}$=6 mA (Note 2)	2.2V	VSS		VSS+0.6	
		$I_{OL(max)}$=1.5 mA (Note 1)	3V	VSS		VSS+0.25	
		$I_{OL(max)}$=6 mA (Note 2)	3V	VSS		VSS+0.6	

Note :

1. $I_{OH(max)}$ and $I_{OL(max)}$ are the maximum total current, the sum of all output currents. Only when it is less than 12mA, just meet maximum voltage without drop.
2. $I_{OH(max)}$ and $I_{OL(max)}$ are the maximum total current, the sum of all output currents. Only when it is less than 48mA, just meet maximum voltage without drop.

MCU Output Frequency

Parameter		Condition		Min	Typ	Max	Unit
$f_{(Px.y)}$(1≤x≤6,0≤y≤7)		C_L=20pF, I_L=1.5mA	V_{CC} = 2.2 V	DC		5	MHz
			V_{CC} = 3 V	DC		7.5	
$f_{(ACLK)}$		C_L = 20 pF				$f_{(System)}$	MHz
$f_{(MCLK)}$							
$f_{(SMCLK)}$							
Output Duty Cycle	$t_{(Xdc)}$	P1.5/TACLK/CLK, C_L=20pF, V_{CC}=2.2V/3V	$f_{(ACLK)}=f_{(LFXT1)}=f_{(XT1)}$	40%		60%	
			$f_{(ACLK)}=f_{(LFXT1)}=f_{(LF)}$	30%		70%	
			$f_{(ACLK)}=f_{(LFXT1)}$		50%		
		P1.1/TA0/MCLK, C_L=20pF, V_{CC}=2.2V/3V	$f_{(MCLK)}= f_{(XT1)}$	40%		60%	
			$f_{(MCLK)}=f_{(DCOCLK)}$	50%-15ns	50%	50%+15ns	
		P1.4/TBCLK/SMCLK,C_L=20pF, V_{CC}=2.2V/3V	$f_{(SMCLK)}=f_{(XT2)}$	40%		60%	
			$f_{(SMCLK)}= f_{(DCOCLK)}$	50%-15ns	50%	50%+15ns	

MCU Wake-up Mode LPM3

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Delay Time	$t_{d(LPM3)}$	f = 1 MHz	2.2V/3V			6	μs
		f = 2 MHz				6	
		f = 3 MHz				6	

RAM

Parameter	Condition	Min	Typ	Max	Unit
VRAMh	CPU Stop (Note 1)	1.6			V

Note 1: The parameter defines the minimum power supply when RAM changes. And all programme must stop when measuring the parameter.

LCD

Parameter		Condition		Min	Typ	Max	Unit
Analog Voltage	$V_{(33)}$	P5.7/R33 Voltage	VCC=3V	2.5		VCC+0.2	V
	$V_{(23)}$	P5.6/R23 Voltage			$[V_{(33)}-V_{(03)}] \times 2/3 + V_{(03)}$		V
	$V_{(13)}$	P5.5/R13 Voltage			$[V_{(33)}-V_{(03)}] \times 2/3 + V_{(03)}$		V
	$V_{(33)}$-$V_{(03)}$	R33 to R03 Voltage		2.2		VCC+0.2	V
Input Leakage Current	$I_{(R03)}$	R03=VSS	No loads on all control and common terminals, VCC=3V			20	nA
	$I_{(R13)}$	P5.5/R13=VCC/3				20	nA
	$I_{(R23)}$	P5.6/R23=2VCC/3				20	nA
Segment Address Voltage	$V_{(Sxx0)}$	I(Sxx) = -3μA， VCC=3V		$V_{(03)}$		$V_{(03)}$-0.1	V
	$V_{(Sxx1)}$			$V_{(13)}$		$V_{(13)}$-0.1	V
	$V_{(Sxx2)}$			$V_{(23)}$		$V_{(23)}$-0.1	V
	$V_{(Sxx3)}$			$V_{(33)}$		$V_{(33)}$-0.1	V

MCU Comparator A (Note 1)

Parameter	Condition	Power Supply	Min	Typ	Max	Unit
$I_{(CC)}$	CAON=1,CARSEL=0,CAREF=0	2.2V		25	40	μA
		3V		45	60	
$I_{(Refladder/RefDiode)}$	CAON=1, CARSEL=0, CAREF=1/2/3, No load at P1.6/CA0 and P1.7/CA1	2.2V		30	50	μA
		3V		45	71	
$V_{(Ref025)}$	PCA0=1, CARSEL=1, CAREF=1, No load at P1.6/CA0 and P1.7/CA1	2.2 V / 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	PCA0=1, CARSEL=1, CAREF=2, No load at P1.6/CA0 and P1.7/CA1	2.2V / 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	PCA0=1, CARSEL=1, CAREF=3, No load at P1.6/CA0 and P1.7/CA1; T_A = 85°C	2.2 V	390	480	540	mV
		3 V	400	490	550	
Common-mode Input Voltage (V_{IC})	CAON=1	2.2 V / 3 V	0		VCC-1	V
Offset Voltage (V_p–V_S)	Note 2	2.2 V / 3 V	-30		30	mV
V_{hys}	CAON = 1	2.2 V / 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$	T_A = 25 °C, Overdrive 10mV, without filter: CAF = 0	2.2 V	160	210	300	ns
		3 V	80	150	240	
	T_A = 25°C, Overdrive 10mV, with filter: CAF = 1	2.2 V	1.4	1.9	3.4	μs
		3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$	T_A = 25°C, Overdrive 10mV, without filter: CAF = 0	2.2 V	130	210	300	ns
		3 V	80	150	240	
	T_A = 25 °C, Overdrive 10mV, with filter: CAF = 1	2.2 V	1.4	1.9	3.4	μs
		3 V	0.9	1.5	2.6	

Note:

1. The leakage current of comparator A has been defined in Ilkg(Px.x).

2. By setting CAEX bit, make the comparator A input reverse. And measure twice continuously, the input offset voltage could be cancelled, then add the two measurements.

POR/Brownout Reset(BOR) (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
$t_{d(BOR)}$	Brownout (Note 2)				2000	us
$V_{CC(start)}$		$dV_{CC}/dt \leq 3$ V/s		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \leq 3$ V/s			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \leq 3$ V/s	70	130	180	mV
$t_{(reset)}$		Pulse width needed at RST/NMI pin to reset internally, V_{CC} = 2.2 V/3 V	2			us

Note:

1. The current consumed in Brownout module has been included in total currents Icc. The voltage range is : $V_{(B\_IT-)} + V_{hys(B\_IT-)} \leq 1.8V$.

2. After $V_{CC}=V_{(B\_IT-)}+V_{hys(B\_IT-)}$, CPU starts to execute program after one $t_{d(BOR)}$ cycle. Before $V_{CC} \geq V_{CC(min)}$, FFL+ setting can't change. $V_{CC(min)}$ is the minimum power supply at operating frequency.

MCU Supply Voltage Supervision

Parameter	Condition		Min	Typ	Max	Unit
$t_{(SVSR)}$	$dV_{CC}/dt \geq 30$ V/ms		5		150	us
	$dV_{CC}/dt \leq 30$ V/ms				2000	us
$t_{d(SVSon)}$	SVSon, switch from VLD=0 to VLD ≠ 0, V_{CC} = 3 V		20		150	us
t_{settle}	VLD ≠ 0 (Note 2)				12	us
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \leq 3$ V/s			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s	VLD = 1	70	120	155	mV
		VLD = 2 to 14	$V_{(SVS\_IT-)}$ x0.004		$V_{(SVS\_IT-)}$ x0.008	
	$V_{CC}/dt \leq 3$ V/s , external voltage applied to A7 terminal	VLD = 15	4.4		10.4	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61 (Note 1)	
		VLD = 13	3.24	3.5	3.76 (Note 1)	
		VLD = 14	3.43	3.7 (Note 1)	3.99 (Note 1)	
	$V_{CC}/dt \leq 3$ V/s , external voltage applied to A7 terminal	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (Note 3)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	uA

Note:

1. The maximum operating voltage is 3.6V.

2.tsettle is the settle time that comparator needs to stabilize level when VLD switches from not 0 to the value between 2 and 15. The overdrive voltage is assumed to be more than 50mV.

3. The consumption current of SVS module has been included in Icc.

DCO

Parameter	Condition		Min	Typ	Max	Unit
$f_{(DCOCLK)}$	N(DCO)=01Eh, FN_8=FN_4=FN_3=FN_2=0,D=2; DCOPLUS = 1, $f_{Crystal}$=32.768kHz	VCC = 2.2 V/3V		1		MHz
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1	VCC = 2.2 V	0.3	0.65	1.25	MHz
		VCC = 3 V	0.3	0.7	1.3	MHz
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=0， FN_2=1; DCOPLUS = 1	VCC = 2.2 V	0.7	1.3	2.3	MHz
		VCC = 3 V	0.8	1.5	2.5	MHz
$f_{(DCO=2)}$	FN_8=FN_4=0,FN_3=1,FN_2=x; DCOPLUS = 1	VCC = 2.2 V	1.2	2	3	MHz
		VCC = 3 V	1.3	2.2	3.5	MHz
S_n	$S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	N(DCO) =01Eh, FN_8=FN_4=FN_3=FN_2=0, D= 2; DCOPLUS = 0	VCC = 2.2 V	-0.2	-0.3	-0.4	%/°C
		VCC = 3 V	-0.2	-0.3	-0.4	%/°C
D_V	N(DCO) =01Eh, FN_8=FN_4=FN_3=FN_2=0, D= 2; DCOPLUS = 0	VCC = 2.2 V/3V	0	5	15	%/V

MCU Crystal Oscillator, LFXT1 Oscillator (Note 1, 2)

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Integrated Input Capacitance	C_{XIN}	OSCCAPx = 0h	2.2 V/3 V		0		pF
		OSCCAPx = 1h	2.2 V/3 V		10		
		OSCCAPx = 2h	2.2 V/3 V		14		
		OSCCAPx = 3h	2.2 V/3 V		18		
Integrated Output Capacitance	C_{XOUT}	OSCCAPx = 0h	2.2 V/3 V		0		pF
		OSCCAPx = 1h	2.2 V/3 V		10		
		OSCCAPx = 2h	2.2 V/3 V		14		
		OSCCAPx = 3h	2.2 V/3 V		18		
Input Logic on XIN	V_{IL}	Note 3	2.2 V/3 V	VSS		0.2VCC	V
	V_{IH}			0.8VCC		VCC	V

Note:

1. The parasitic capacitance generated from package and board is about 2pF. The crystal effective load capacitance is (C_{XIN} x C_{XOUT})/(C_{XIN} + C_{XOUT}), which has nothing with XTS_FLL.

2. There are some principles to be observed as follows, in order to improve the EMI characteristic of low dissipation LFXT1 oscillator, especially in LF mode(32kHz).

(1) The traces between the MS616F22 and crystal should be as short as possible.

(2) Optimal design of ground plane near oscillator pin.

(3) Avoid that other clock and data lines have crosstalk with XIN and XOUT pins.

(4) Avoid layout traces below or near XIN and XOUT pins.

(5) By using match materials and repeated practices to reduce parasitic load on XIN, XOUT pins.

(6) If use protection coating, pay attention not to cause capacitive and resistive leakage among oscillator pins.

3. Only valid when using external logic clock and must set XTS_FLL bit. While invalid when using crystal and resonator.

4. For accurate real time clock application, OSCCAPx=0h, apply recommended capacitance.

MCU Crystal Oscillator, XT2 Oscillator (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
Integrated Input Capacitance	C_{XT2IN}	V_{CC} = 2.2 V/3 V		2		pF
Integrated Output Capacitance	C_{XT2OUT}	V_{CC} = 2.2 V/3 V		2		pF
Input Logic on XT2IN	V_{IL}	V_{CC} = 2.2 V/3 V	VSS		0.2VCC	V
	V_{IH}	Note 2	0.8VCC		VCC	V

Note: 1. The two terminals of oscillator all need to connect with load capacitance. The accurate capacitance value is provided by crystal manufacturer.

2. Only valid when using external logic clock and must set XTS_FLL bit. While invalid when using crystal and resonator.

MCU USART0, USART1 (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
USART0/1: Deglitch Time	$t_{(\tau)}$	V_{CC} = 2.2 V, SYNC = 0, UART mode	200	430	800	ns
		V_{CC} = 3 V, SYNC = 0, UART mode	150	280	500	

Note 1: The signal applied to USART0/1 receive terminal should meet t(τ) timing requirement, thus ensure URXS trigger is set. URXS trigger is set by low level pulse, which satisfies t(τ) minimum timing requirement. The operating conditions set by flag bit must be independent of the timing constraint. The deglitch circuit only operate when URXD0/1 line transmit negatively.

12-bit ADC, Power Supply and Input Range (Note 1)

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Analog Power Supply	AVCC	AVCC and DVCC is connected together. AVSS and DVSS is connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
Analog Input Voltage (Note 2)	$V_{(P6.x/Ax)}$	Applicable to all P6.0/A0 to P6.7/A7 terminals. Analog input terminal is selected by ADC12MCTLx, and P6Sel.x=1,0 ≤ x ≤ 7; $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
Operating Current on AV_{CC} (Note 3)	I_{ADC12}	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	2.2V		0.65	1.3	mA
			3V		0.8	1.6	
Operating Current on AV_{CC} (Note 4)	I_{REF+}	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 1	3V		0.5	0.8	mA
		$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 1	2.2V		0.5	0.8	mA
			3V		0.5	0.8	
Input Capacitance	C_I	Choose only one terminal one time, P6.x/Ax	2.2V			40	pF
Input Multiplexer Resistance	R_I	$0V \le V_{Ax} \le V_{AVCC}$	3V			2000	Ω

Note :

1. Leakage current has been defined in P6.x/Ax terminal parameter sheet.
2. Analog input voltage range should be within reference voltage range, thus achieve valid conversion result.
3. Reference current is not included in I_{ADC12}.
4. Reference current is provided by AVCC. And the current is independent of ADC12ON until conversion starts. Before A/D conversion, set REFON bit to enable built-in reference voltage module.

12-bit ADC, External Reference

Parameter		Condition		Min	Typ	Max	Unit
Positive External Reference Voltage Input	V_{eREF+}	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (Note 2)		1.4		V_{AVCC}	V
Negative External Reference Voltage Input	V_{REF-}/V_{eREF-}	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (Note 3)		0		1.2	V
External Reference Differential Voltage Input	$(V_{eREF+} - V_{REF-}/V_{eREF-})$	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (Note 4)		1.4		V_{AVCC}	V
Static Input Current	I_{VeREF+}	$0V \le V_{eREF+} \le V_{AVCC}$	2.2V/3 V			±1	uA
Static Input Current	$I_{VREF-/VeREF-}$	$0V \le V_{eREF-} \le V_{AVCC}$	2.2V/3 V			±1	uA

Note :

1. External reference charges and discharge capacitance array during conversion.For external reference, input capacitance Ci is dynamic load during conversion period. The dynamic impedance of reference voltage should be matched with analog source impedance recommendation, achieving 12-bit setup accuracy on charging.
2. The accuracy constrains the minimum of positive external reference voltage. Decreasing accuracy demand could use lower reference voltage.
3. The accuracy constrains the maximum of negative external reference voltage. Decreasing accuracy demand could use higher reference voltage.
4. The accuracy constrains the difference of external reference voltage. Decreasing accuracy demand could use lower difference reference voltage.

12-bit ADC, Built-in Reference

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Positive Built-in Reference Voltage	V_{REF+}	REF2_5V = 1, $I_{VREF+} \le I_{VREF+}$max	3V	2.4	2.5	2.6	V
		REF2_5V = 0, $I_{VREF+} \le I_{VREF+}$max	2.2 V/3 V	1.44	1.5	1.56	
Minimum Power Supply of Positive Built-in Reference Voltage	$AVCC_{(min)}$	REF2_5V = 0, $I_{VREF+} \le$ 1mA		2.2			V
		REF2_5V = 1, $I_{VREF+} \le$ 0.5mA		V_{REF+}+0.15			
		REF2_5V = 1, $I_{VREF+} \le$ 1mA		V_{REF+}+0.15			
Load Current on V_{REF+}	I_{VREF+}		2.2 V	0.01		-0.5	mA
			3V			-1	
Load Modulation Current on V_{REF+}	$I_{L(VREF)+}$	I_{VREF+}= 500 uA +/− 100uA Analog input voltage~0.75V; REF2_5V = 0	2.2 V			±2	LSB
			3V			±2	LSB
		I_{VREF+} = 500 uA +/− 100uA Analog input voltage~1.25 V; REF2_5V = 1	3V			±2	LSB
Load Modulation Time on V_{REF+}	$I_{DL(VREF)+}$	I_{VREF+}=100 uA → 900uA, C_{VREF+} = 5 µF, Analog input voltage~ 0.5V_{REF+} Conversion result error≤ 1 LSB	3V			20	ns
External Capacitance on V_{REF+} (Note 1)	C_{VREF+}	REFON =1, 0 mA ≤ I_{VREF+} ≤ I_{VREF+}max	2.2 V/3 V	5	10		uF
Temperature Coefficient of Built-in Reference	T_{REF+}	I_{VREF+} is a constant, range: 0mA ≤ I_{VREF+} ≤ 1mA	2.2 V/3 V			±100	ppm /°C
Setup Time of Built-in Reference (Note 2)	t_{REFON}	I_{VREF+}= 0.5mA, C_{VREF+} = 10µF, V_{REF+} = 1.5 V	2.2 V			17	ms

Note :

1. Internal buffer magnifier and accuracy demand need one external capacitor. For all INL and DNL tests, connect two capacitors between V_{REF+} and A_{VSS}, V_{REF-}/V_{eREF-} and AV_{SS}, a 10uF tantalum capacitor and a 100nF ceramic capacitor.

2. Test condition: the conversion error is less than ±0.5 LSB after t_{REFON} opens. The setup time is up to external capacitance load.

12-bit ADC, Timing Parameter

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
$f_{ADC12CLK}$		Ensure accuracy of ADC linearity parameter	2.2V/3 V	0.45	5	6.3	MHz
Internal ADC12 Oscillator	$f_{ADC12OSC}$	ADC12DIV=0, $f_{ADC12CLK}=f_{ADC12OSC}$	2.2 V/ 3 V	3.7		6.3	MHz
Conversion Time	$t_{CONVERT}$	C_{VREF+} ≥ 5 uF, internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz - 6.3 MHz	2.2 V/ 3 V	2.06		3.51	us
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK: ADC12SSEL ≠ 0			13·ADC12DIV·1/$f_{ADC12CLK}$		us
ADC Enable Time	$t_{ADC12ON}$	Note 1				100	ns
Sampling Time	t_{Sample}	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, τ= [R_S + R_I] x C_I (Note 2)	3V	1220			ns
			2.2V	1400			

Note :

1. After ADC12ON is enabled, $t_{ADC12ON}$ is the time when the conversion error is less than ±0.5 LSB. And the reference voltage and input signal have be set.

2. After about 10τ, the conversion error is less than ±0.5 LSB, $t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800ns$ (n=ADC resolution=12, RS= input resistance).

12-bit ADC, Linearity Parameter

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Integral Nonlinearity Error	E_I	1.4 V ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ 1.6 V	2.2 V/ 3 V			±2	LSB
		1.6 V < (V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ [$V_{(AVCC)}$]				±1.7	
Differential Nonlinearity Error	E_D	(V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), C_{VREF+} = 10 uF (tantalum) and 100 nF (ceramic)	2.2 V/ 3 V			±1	LSB
Offset Error	E_O	(V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), Internal impedance of source R_S < 100Ω, C_{VREF+} = 10 uF (tantalum) and 100 nF (ceramic)	2.2 V/ 3 V		±2	±4	LSB
Gain Error	E_G	(V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), C_{VREF+} = 10 uF (tantalum) and 100 nF (ceramic)	2.2 V/ 3 V		±1.1	±2	LSB
Total Unadjusted Error	E_T	(V_{eREF+} – V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), C_{VREF+} = 10 uF (tantalum) and 100 nF (ceramic)	2.2 V/ 3 V		±2	±5	LSB

12-bit ADC, Temperature Sensor and Built-in Mid-voltage VMID

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Current on AV_{CC} (Note 1)	I_{SENSOR}	REFON = 0, INCH = 0Ah, ADC12ON=NA, T_A = 25	2.2 V		40	120	uA
			3 V		60	160	
V_{SENSOR}		ADC12ON =1, INCH = 0Ah, T_A =0°C	2.2 V		986	986±5%	mV
			3 V		986	986±5%	
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V		3.55	3.55±3%	mV/°C
			3 V		3.55	3.55±3%	
Sampling Time Required by Selecting Channel 10 (Note 2)	t_{SENSOR} (sample)	ADC12ON = 1, INCH = 0Ah, Conversion error ≤ 1 LSB	2.2 V	30			us
			3 V	30			
Current Divided on Channel 11	I_{VMID}	ADC12ON = 1, INCH = 0Bh, (Note 3)	2.2 V			NA	uA
			3 V			NA	
Voltage Divided on Channel 11	V_{MID}	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~ 0.5 x V_{AVCC}	2.2 V		1.1	1.1±0.04	V
			3 V		1.5	1.5±0.04	
Sampling Time Required by Selecting Channel 11	$t_{VMID(sample)}$	ADC12ON = 1, INCH = 0Bh, Conversion error ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

Note :

1. If (ADC12ON=1, REFON=1) or (ADC12ON=1, INCH=0Ah and sampling signal at high-level), sensor current I_{SENSOR} would be generated. The current includes the values through senor and reference.
2. Typical equivalent impedance of sensor is 51kΩ. The sampling time includes sensor enabled time $t_{SENSOR(on)}$.
3. V_{MID} is only used during sampling process, without generating extra current.
4. The sampling time, $t_{VMID(sample)}$ has included enabled time $t_{VMID(on)}$, without extra time.

Flash

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Operating Voltage at Programming, Erasing	$V_{CC(PGM/ERASE)}$			2.7		3.6	V
The Frequency for Flash Programming	f_{FTGP}			257		476	kHz
The Frequency for Flash Erasing	f_{FTGE}			15		100	kHz
Current on DV_{CC} at Programming	I_{PGM}		2.7 V/ 3.6 V		3	5	mA
Current on DV_{CC} at Erasing	I_{ERASE}		2.7 V/ 3.6 V		3	7	mA
Accumulated Programming Time	t_{CPT}	Note 1	2.7 V/ 3.6 V			10	ms
Accumulated Large-scale Erasing Time	$t_{CMErase}$	Note 2	2.7 V/ 3.6 V	200			ms
Programming/ Erasing Duration				10^4	10^5		cycles

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
Data Save Cycle	$t_{Retention}$	T_J = 25°C		100			years
Word or Byte Programming Time	t_{Word}	Note 3			35		t_{FTG}
Block Programming Time of the First Word or Byte	$t_{Block, 0}$				30		
Block Programming Time of Each Additional Word or Byte	$t_{Block, 1-63}$				21		
Waiting Time for Block Programming Finishing Sequencing	$t_{Block, End}$				6		
Large-scale Erasing Time	$t_{Mass Erase}$				5297		
Segment Erasing Time	$t_{Seg Erase}$				4819		

Note：

1. When a 64-bit Flash module is written, it couldn't exceed accumulated programming time.The parameter is applicable to all Flash programming methods.
2. The large-scale erasing time is up to Flash timing.
   At least 11.1ms (= 5297x1/f_{FTG}, maximum = 5297x1/476kHz).
3. These values have been fixed into the state machine of Flash controller.
4. The erasing frequency on chip is less than 100K.
5. Program on chip by word format, rather than byte format.
6. Information storage only has A segment (128 bytes), without B segment.
7. 2048 bytes rather than 512 bytes in each segment of master storage.

JTAG, Interface

Parameter		Condition	Power Supply	Min	Typ	Max	Unit
TCK Input Frequency	f_{TCK}	Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
Internal Pull-up Resistors on TMS, TCK, TDI/TCLK	$R_{Internal}$	Note 2	2.2 V/ 3 V	25	60	90	kΩ

Note :

1. f_{TCK} may be constrained by the timing requirement of selected module.
2. TMS, TDI/TCLK and TCK pull-up resistors have been integrated.

JTAG, Fuse (Note 1)

Parameter		Condition	Min	Typ	Max	Unit
Power Supply Needed by Fuse-blow	$V_{CC(FB)}$	T_A = 25°C	2.5			V
TDI/TCLK Voltage Needed by Fuse-blow	V_{FB}		6		7	V
TDI/TCLK Current Needed by Fuse-blow	I_{FB}				100	mA
Time for Fuse-blow	t_{FB}				1	ms

Note 1: Once the fuse is blown, the JTAG/Test of the MS616F22 can't be connected, and the simulation characteristic would be lost. JTAG mode is switched to bypass mode.

TDC DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
32kHz Crystal Current	I_{32}	$I_{CC}+I_{IO}$, only 32kHz crystal operating		1		uA
4MHz Crystal Current	I_{hs}	$V_{cc}=V_{io}$= 3.6V		200		uA
		$V_{cc}=V_{io}$=3.0V		130		uA
		Off		<1		uA
Time Measuring Unit Current	I_{tmu}	Only time measurement enabled		4		mA
Quiescent Current	I_{ddq}	All clocks off,@85°C		<0.1		uA
Operating Current	I_o	TOF-UP/DOWN, 1/s normal temperature, PT1000,1/30s		1.1 0.15		uA
Temperature Measuring Current	I_T	Once every 30 seconds		0.085		uA
Current of Analog Part	I_{ana}	Enable analog part		0.8		mA
Total Current	I_{total}	Twice time measurements per second Once temperature measurement every 30 seconds		2.3		uA
High Level Output Voltage	V_{oh}	I_{oh}= tbd mA V_{io}=Min.	$0.8V_{io}$			V
Low Level Output Voltage	V_{ol}	I_{ol}=tbd mA, V_{io}=Min			$0.2V_{io}$	V
High Level Input Voltage	V_{ih}	LVTTL, V_{io} = Max.	$0.7V_{io}$			V
Low Level Input Voltage	V_{il}	LVTTL, V_{io} = Min.			$0.3V_{io}$	V
High Level Schmitt Trigger Voltage	V_{th}		$0.7V_{io}$			V
Low Level Schmitt Trigger Voltage	V_{tl}				$0.3V_{io}$	V
Schmitt Trigger Threshold	V_h			0.28		V

TDC Analog Frontend

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Comparator Input Drift Voltage (Chopper Stable)				<1	2	mV
On-Resistance of Analog Switches at STOP1/STOP2 Inputs	$R_{dson(AS)}$			200		Ω
On-Resistance of FIRE_UP,FIRE_DOWN Output Buffers	$R_{dson(FIRE)}$	Symmetrical outputs, R_{dson} (HIGH)= R_{dson} (LOW)		4		Ω
Output Current of FIRE_UP,FIRE_DOWN Output Buffers	I_{FIRE}			96		mA

TDC Time Measurement Unit

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Measurement Accuracy	LSB	Measurement Range 1&2		75		ps
		DOUBLE_RES = 0 DOUBLE_RES = 1		37		
		Measurement Mode 2: QUAD_RES = 1		19		
Standard Deviation	σ	Measurement Range 1&2 DOUBLE_RES = 0 DOUBLE_RES = 1		t.b.d		ps
		Measurement Mode 2: QUAD_RES = 1		t.b.d		
Measurement Range	t_m	Measurement Range 1	3.5ns		2.4µs	
		Measurement Range 2 (4M High-speed Clock)	500ns		4ms	
Integral Non-linearity	INL			<0.1		LSB
Differential Non-linearity	DNL			<0.1		LSB

TDC Temperature Measurement Unit (Note 1)

Parameter		Condition				Unit
		Built-in Schmitt Trigger		External Schmitt Trigger[2]		
		PT500	PT1000	PT500	PT1000	
Resolution RMS		17.5	17.5	16.0	16.0	Bit
SNR		105	105	96	96	dB
Absolute Gain [3]		0.9912	0.9931	0.9960	0.9979	
Absolute Gain vs.V_{io} [3]	3.6V	0.9923	0.9940	0.9962	0.9980	
	3.0V	0.9912	0.9931	0.9960	0.9979	
	2.5V	0.9895	0.9915	0.9956	0.9979	
Gain Drift vs.V_{io}		0.25	0.23	0.06	0.04	%/V
Maximum Gain Error@ d ϴ =100 K		0.05%	0.05%	0.02%	<0.01%	
Gain Drift vs. Temperature		0.022	0.017	0.012	0.0082	%/10K
Gain Drift vs. V_{io}				0.08		%/V
Initial Zero Drift		<20	<10	<20	<10	mK
Zero Drift vs. Temperature		<0.05	<0.03	<0.012	<0.082	mK/°C
PSRR			>100			dB

Note:

1. All measurements are at 3.0V. C_{load} = 100nF for PT1000, 200 nF for PT500 (C0G- type).

2. Apply external 74AHC14 Schmitt trigger.

3.Compare with the situation where the ideal gain is 1.

TDC Clock Oscillator

Parameter	Symbol	Min	Typ	Max	Unit
32kHz Reference Crystal Clock	Clk_{32}		32.768		kHz
32kHz Crystal Start-up Time after Power-up	t_{32st}		3		s
High-speed Crystal Reference Clock	Clk_{HS}	2	4	8	MHz
Start-up Time for Ceramic Crystal	t_{oszst}		100		µs
Start-up Time for Quartz Crystal	t_{oszst}		1		ms

TDC Serial Interface

Parameter	Symbol	Max		Unit
		VCC=2.5V	VCC=3.3V	
Serial Clock Frequency	f_{clk}	15	20	MHz
Serial Clock, Pulse High	t_{pwh}	30	25	ns
Serial Clock, Pulse Low	t_{pwl}	30	25	ns
SSN Enabled to Clock Edge Valid	t_{sussn}	40	10	ns
SSN Pulse Width between Write Cycles	t_{pwssn}	50	40	ns
SSN Hold Time after SCK Falling Edge	t_{hssn}	40	25	ns
Data Valid to SCK Falling Edge	t_{sud}	5	5	ns
Data Hold Time after SCK Falling Edge	t_{hd}	5	5	ns
SCK Rising Edge to Data Valid	t_{vd}	20	16	ns

Serial Interface (SPI compatible, Clock Phase Bit =1, Clock Polarity Bit =0):

The serial interface is compatible with 4-wire SPI. It requires a SerialSelectNot (SSN) signal, so it can't work in 3-wire SPI interface.

The first rising edge of SCK will reset INTN pin (interrupt pin) state.

The transmission starts from the most significant bit (MSB) and ends with the least significant bit (LSB). Data transmission is done in bytes format. Data transmission can stop after each byte by sending a LOW-HIGH-LOW level to SSN.

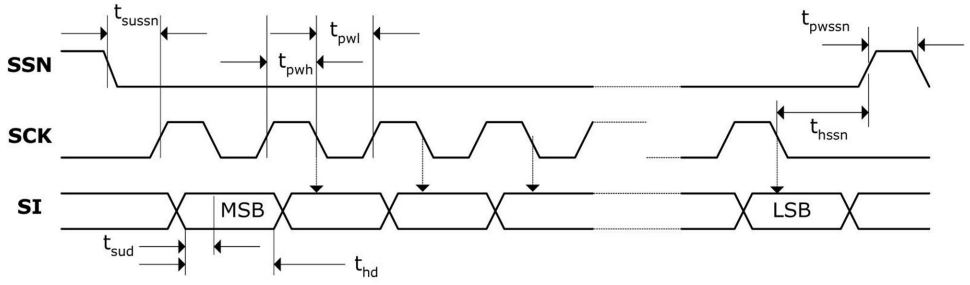


Figure 1. SPI Write Timing

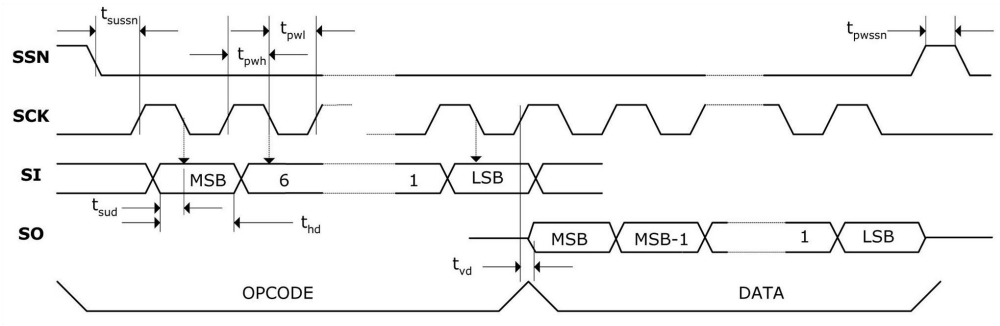


Figure 2. SPI Read Timing

Timing for Closing STOP Channel

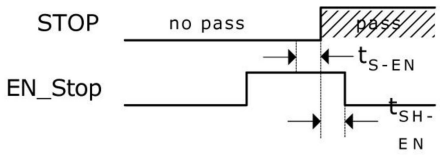


Figure 3. Timing for Closing STOP Channel

Parameter	Symbol	Min	Max	Unit
Enable Setup Time	t_{S-EN}	t.b.d.	-	ns
Enable Hold Time	t_{SH-EN}	t.b.d.	-	ns

System Reset Timing

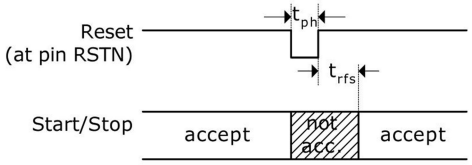
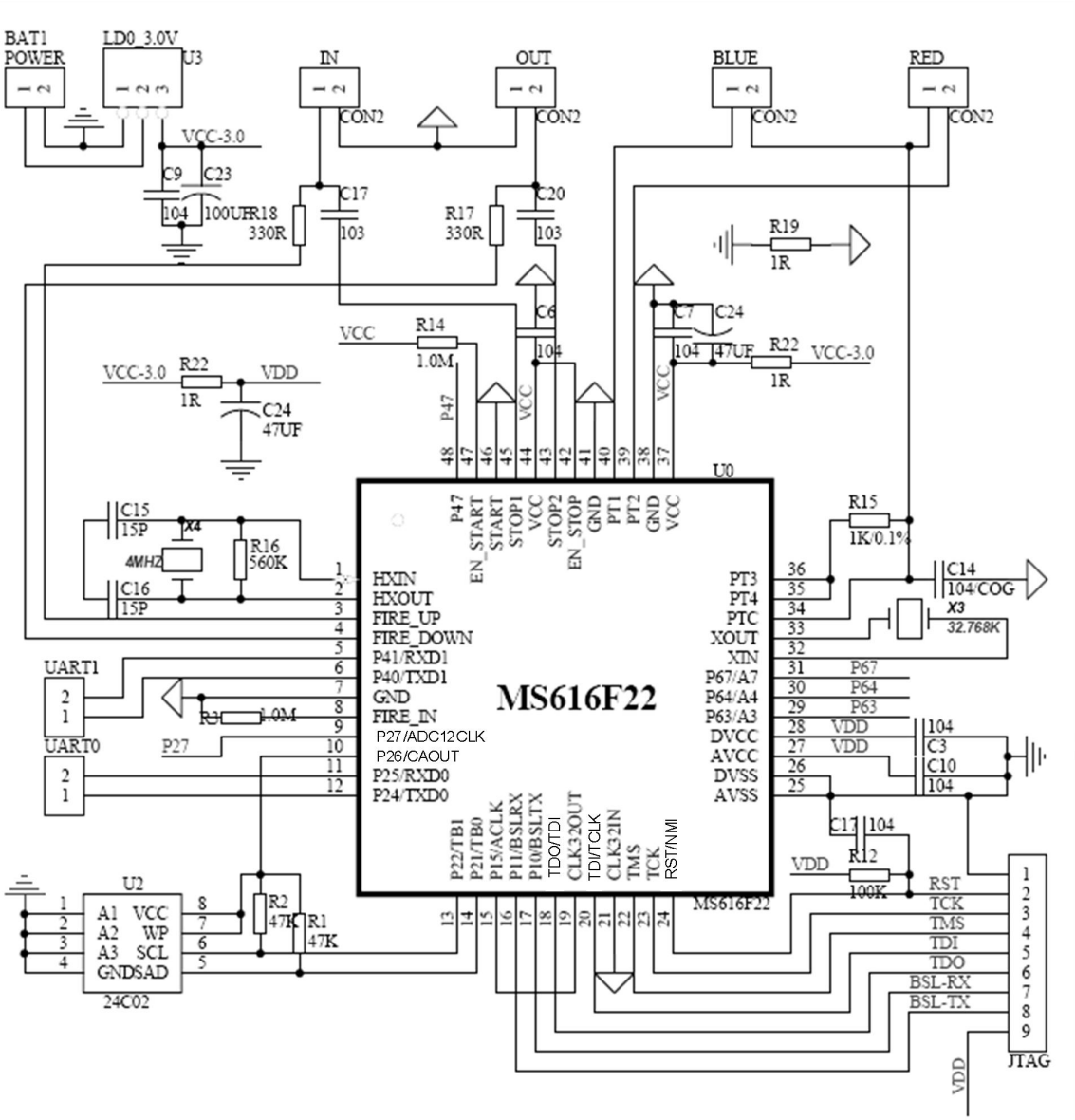


Figure 4. System Reset Timing

Parameter	Symbol	Min	Max	Unit
Reset Pulse Width	t_{ph}	t.b.d.	-	ns
Time Internal between rising edge of reset pulse and pulse received	t_{rfs}	t.b.d.	-	ns

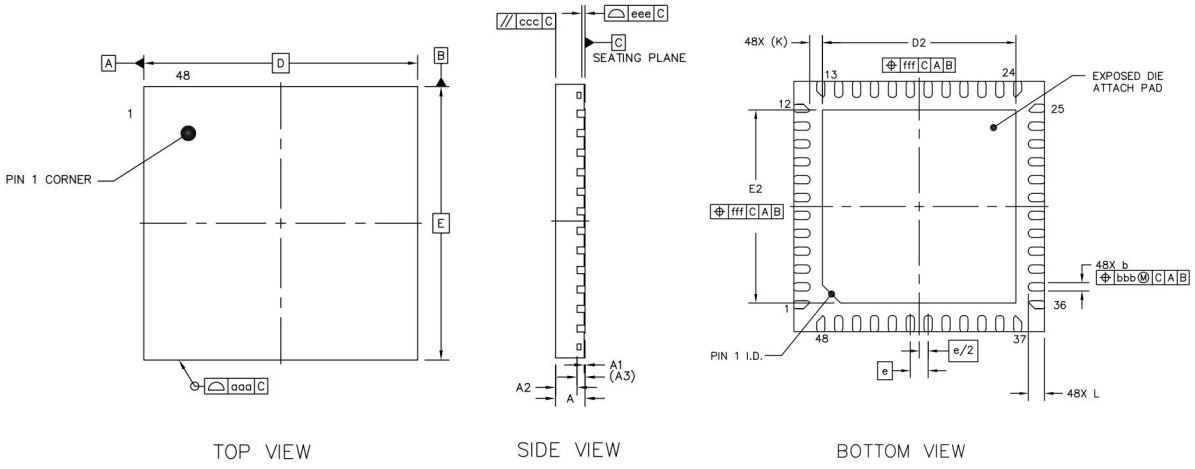
Note: After power-on reset, it is necessary to wait 500us at least to initiate the analog part.

TYPICAL APPLICATION DIAGRAM



PACKAGE OUTLINE DIMENSIONS

QFN48 (07X07) (Back Thermal Pad)

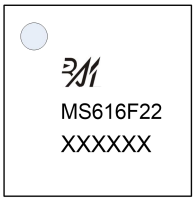


TOP VIEW SIDE VIEW BOTTOM VIEW

		Symbol	Dimensions In Millimeters		
			Min	Typ	Max
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2		0.55	
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.18	0.23	0.28
BODY SIZE	X	D	7 BSC		
	Y	E	7 BSC		
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D2	5.3	5.4	5.5
	Y	E2	5.3	5.4	5.5
LEAD LENGTH		L	0.35	0.45	0.55
LEAD TIP TO EXPOSED PAD EDGE		K	0.35 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.1		
EXPOSED PAD OFFSET		fff	0.1		

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name : MS616F22

Product Code : XXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS616F22	QFN48	2000	1	2000	8	16000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

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- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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