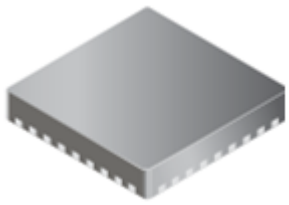
Quad DMOS Full Bridge Driver

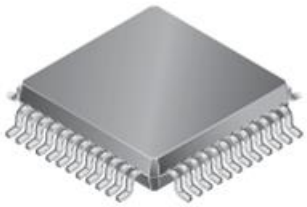
PRODUCT DESCRIPTION

The MS35631N/MS35631 is a quad DMOS full bridge driver, which can drive two stepper motors or four DC motors.The driving current of each full bridge can be up to 1.2A. The MS35631N/MS35631 integrates a fixed off-time PWM current regulator and a 2bit nonlinear DAC, and could operate in full, half, quarter steps and forward, reverse, standby modes. PWM current regulator uses mixed decay mode, which can reduce audio motor noise and power dissipation and improve step accuracy. The MS35631N/MS35631 also integrates internal synchronous rectification control circuit to reduce PWM operating power dissipation.

The MS35631N/MS35631 integrates protection circuits, such as undervoltage protection (UVLO), overcurrent protection, overturning current protection and thermal shutdown, thus not to require specified power start sequence.



QFN36



TQFP48

FEATURES

- Quad Full Bridge
- Dual Stepper Motor Driving
- Large Current Output
- 3.3V and 5V Logics
- Synchronous Rectification
- Built-in UVLO
- Overcurrent Protection
- Overturn Protection
- Thermal Shutdown

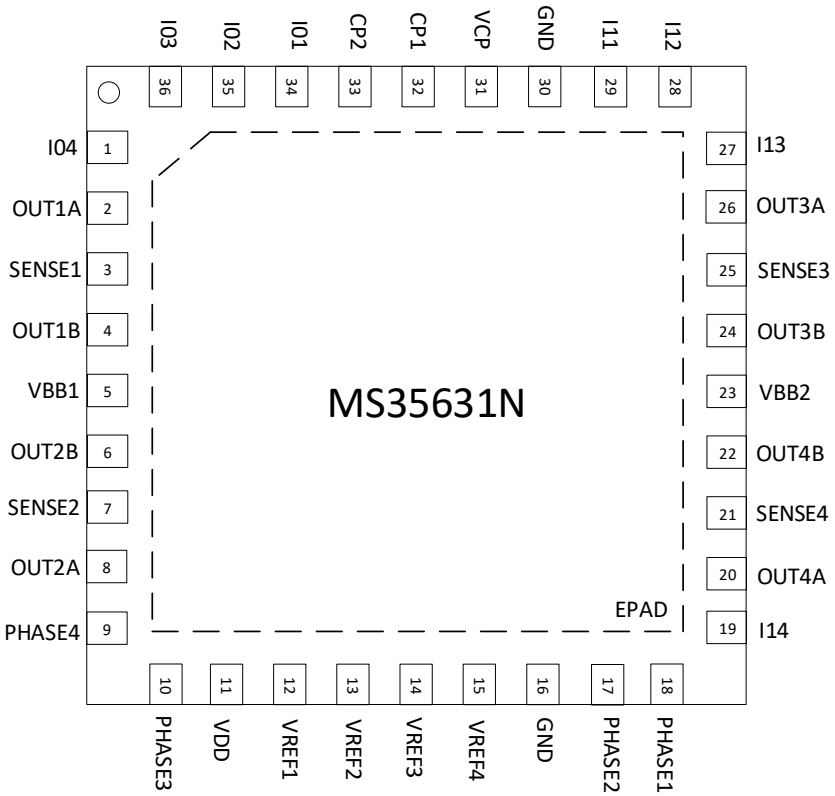
APPLICATIONS

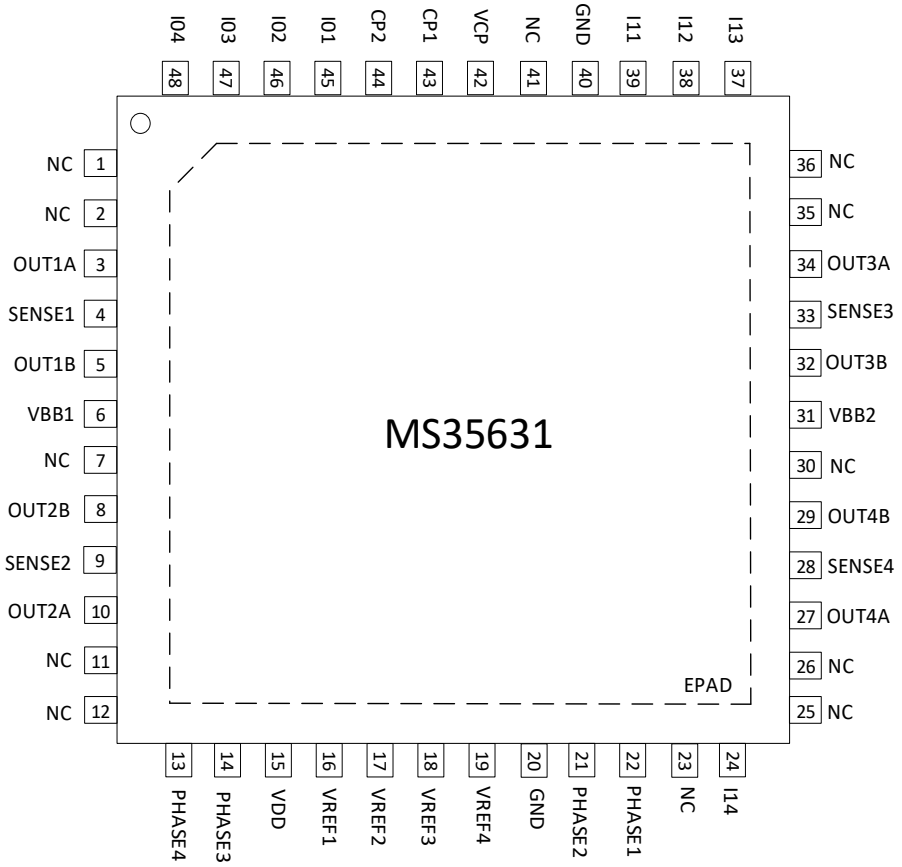
- Security Monitoring
- Stage Lights
- Toys
- Robotic Technology
- Medical Equipment

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS35631N	QFN36	MS35631N
MS35631	TQFP48	MS35631

PIN CONFIGURATION



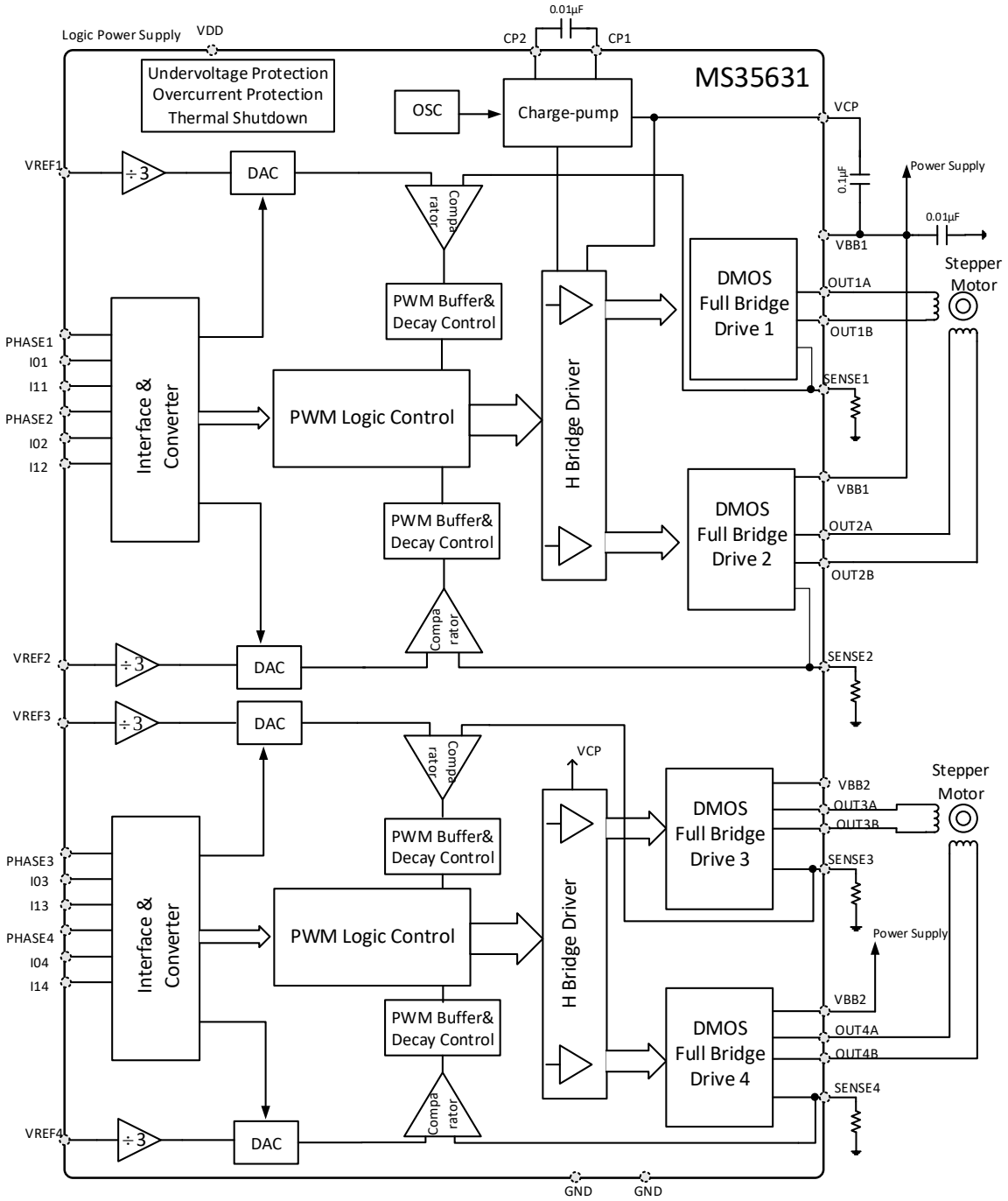


PIN DESCRIPTION

Pin		Name	Description
MS35631N	MS35631		
2	3	OUT1A	DMOS H-Bridge Channel 1 Output A
3	4	SENSE1	Channel 1, SENSE Resistor Pin
4	5	OUT1B	DMOS H-Bridge Channel 1 Output B
5	6	VBB1	Power Supply
6	8	OUT2B	DMOS H-Bridge Channel 2 Output B
7	9	SENSE2	Channel 2, SENSE Resistor Pin
8	10	OUT2A	DMOS H-Bridge Channel 2 Output A
9	13	PHASE4	Channel 4, Control Input Pin
10	14	PHASE3	Channel 3, Control Input Pin
11	15	VDD	Logic Power Supply
12	16	VREF1	Channel 1, Analog Input Pin
13	17	VREF2	Channel 2, Analog Input Pin
14	18	VREF3	Channel 3, Analog Input Pin
15	19	VREF4	Channel 4, Analog Input Pin
16	20	GND	Ground
17	21	PHASE2	Channel 2, Control Input Pin
18	22	PHASE1	Channel 1, Control Input Pin
19	24	I14	Channel 4, Control Input Pin
20	27	OUT4A	DMOS H-Bridge Channel 4 Output A
21	28	SENSE4	Channel 4, SENSE Resistor Pin
22	29	OUT4B	DMOS H-Bridge Channel 4 Output B
23	31	VBB2	Power Supply
24	32	OUT3B	DMOS H-Bridge Channel 3 Output B
25	33	SENSE3	Channel 3, SENSE Resistor Pin
26	34	OUT3A	DMOS H-Bridge Channel 3 Output A
27	37	I13	Channel 3, Control Input Pin
28	38	I12	Channel 2, Control Input Pin
29	39	I11	Channel 1, Control Input Pin
30	40	GND	Ground
31	42	VCP	Reservoir Charge Capacitor Pin

Pin		Name	Description
MS35631N	MS35631		
32	43	CP1	Charge-pump Capacitor Pin
33	44	CP2	Charge-pump Capacitor Pin
34	45	I01	Channel 1, Control Input Pin
35	46	I02	Channel 2, Control Input Pin
36	47	I03	Channel 3, Control Input Pin
1	48	I04	Channel 4, Control Input Pin
-	1,2,7,11,12,23, 25,26,30,35, 36,41	NC	Not Connection
-	-	EPAD	Exposed Thermal Pad, soldered to PCB directly and connected to ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	V_{BB}	-0.5 ~ 38	V
Logic Supply	V_{DD}	-0.4 ~ 6	V
Output Current	I_{OUT}	1.2	A
Logic Input Voltage	V_{IN}	-0.3 ~ 6	V
SENSEx Pin Voltage	V_{SENSEx}	0.5	V
VREFx Pin Voltage	V_{REFX}	2.5	V
Operating Temperature	T_A	-40 ~ 105	°C
Junction Temperature	T_{JMAX}	150	°C
Storage Temperature	T_{STG}	-65~ 150	°C
ESD(HBM)	V_{ESD}	>±3k	V

Thermal Resistance

Parameter	Symbol	MS35631N	MS35631	Unit
		QFN36	TQFP48	
Junction to Ambient	$R_{\theta JA}$	19.02	17.50	°C/W

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A= 25°C ±2°C, V_{BB}=24V, V_{DD}=3.3V.

Power

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply	V_{BB}		8		36	V
Logic Supply	V_{DD}		3		5.5	V
Power Supply Current	I_{BB}			2.4	10	mA
Logic Supply Current	I_{DD}			1.84		mA

Output Power FET

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-side FET Output On-Resistance	R_{DSONH}	I_{OUT}=500mA,T_J=25°C		0.5	0.7	Ω
Low-side FET Output On-Resistance	R_{DSONL}	I_{OUT}=500mA,T_J=25°C		0.5	0.8	Ω

Logic and Low Voltage Input

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Voltage	$V_{IN(H)}$		0.7×V_{DD}		V_{DD}+0.3	V
Low-level Input Voltage	$V_{IN(L)}$		-0.3		0.3×V_{DD}	V
VREFx Input Voltage	V_{REFX}		0		2.5	V
VREFx Input Current	I_{REF}	V_{REF}=1.5V			±1	μA

Timing

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Propagation Delay	t_{D1}	PWM Conversion, HS FET Open	350	550	1000	ns
	t_{D2}	PWM Conversion, HS FET Closed	35		300	ns
	t_{D3}	PWM Conversion, LS FET Open	350	550	1000	ns
	t_{D4}	PWM Conversion, LS FET Closed	35		250	ns
Overturn Delay	t_{COD}		300	425	1000	ns
Blank Time	t_{BLANK}		0.7	1	1.3	μs

Output Current Accuracy

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Current Error[1]	V_{ERR}	V_{REF} =1.5V, Phase Current 100%	-5		5	%
		V_{REF} =1.5V, Phase Current 67%	-5		5	%
		V_{REF} =1.5V, Phase Current 33%	-15		15	%

Note 1: $V_{ERR} = (V_{REF}/3 - V_{SENSE})/(V_{REF}/3)$.

Protection Circuit

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VBB Undervoltage Protection	$V_{UV(VBB)}$	V_{BB} Rise	6.5	6.8	7.1	V
VBB Undervoltage Hysteresis	$V_{UV(VBB)HYS}$		0.3	0.4	0.5	V
VDD Undervoltage Protection	$V_{UV(VDD)}$	V_{DD} Rise	2.6	2.7	2.8	V
VDD Undervoltage Hysteresis	$V_{UV(VDD)HYS}$		75	105	125	mV
Thermal Shutdown	T_{JSD}	Temperature Rise	155	165	175	°C
Thermal Shutdown Hysteresis	T_{JSD_HYS}			15		°C
Overcurrent Protection Trip Point	I_{OCP}			3		A
Overcurrent Protection Detection Time	t_{OCP}			1		μs
Overcurrent Protection Self-start Output Close Time	t_{PRO}	Trigger Overcurrent Protection		10		ms

FUNCTION DESCRIPTION

Device Characteristics

The MS35631N/MS35631 could drive two stepper motors or four DC motors, and also one stepper motor plus two DC motors. The output H full bridges are four N-channel DMOS FETs, controlled by PWM. The output peak current of each full bridge is decided by R_{SENSEx} and V_{REFx} together. Input pins include PHASEX, I0x, I1x.

Internal PWM Current Control Principle

Each full bridge has PWM current control circuit with fixed decay time, which makes load current not more than setting value, ITRIP. One H-bridge diagonal pair of source and drain FETs are enabled, and current flows into motor and R_{SENSE} resistor. When the voltage on R_{SENSE} is equal to one third of VREF voltage, current detection comparator would reset PWM controller and disable source DMOS FET. The maximum current limit is determined by the resistance of R_{SENSE} and the voltage on VREF terminal. The maximum current is calculated:

$$ITripMax=VREF/(3\times R_{SENSE})$$

Each stepping current limit, ITrip , is the percentage of ITripMax, maximum current limit. ITrip calculated formula is as follows:

$$ITrip = (\%\ ITripMax/100)\times ITripMax$$

% ITripMax see step sequence setting below. Note that the maximum voltage on R_{SENSE} doesn't exceed ±500mV in application.

Fixed Off-time

Internal PWM control circuit integrates one fixed-time pulse to disable FETs. The off-time, toff, is set as 10μs internally.

Blank Time

When output is changed caused by internal circuit, the output of current detection comparator would be ignored within blank time to avoid output false detection, such as reverse recovery current of clamp diode or the overcurrrent due to on/off for load capacitor. The blank time is set as 1μs.

Control Logic

The communication between device and controller is transmitted via industry standard I1, I0, PHASE interface. Full, half, quarter step modes can be realized by control logic. Each H bridge sets dependant VREF pin and higher precision step modes can be achieved by dynamically control VREF pin.

Charge-pump (CP1, CP2)

The charge-pump circuit generates a higher power supply than VBB to drive the source FET of the H-bridge. In application, due to the need for charge and discharge, a 0.1uF ceramic capacitor is needed to be connected between CP1 and CP2. A 0.1uF ceramic capacitor is also required between VCP and VBBx to store charge.

Protection Function

The MS35631N/MS35631integrates perfect protection functions, including thermal shutdown, undervoltage protection and overcurrent protection.

The overcurrent protection function could detect many shorted conditions, such as output to power, ground and output-to-output. When short-circuit time is detected over 1μs, the output is disabled. After 10ms, the MS35631N/MS35631 would attempt to restart automatically.

Synchronous Rectification

When the internal fixed decay time circuit is triggered and the PWM-off works, the load current will return. During current decay, the synchronous rectification function will turn on the corresponding DMOS FET and short out the parasitic diode with Rdson resistance, which can effectively reduce power dissipation. When zero current is detected, synchronous rectification is turned off to prevent the load current from reversing.

Mixed Decay Mode

H bridge operates in mixed decay mode as shown in following figures. When current reaches current limit, fast decay mode is entered and the duration time (t_{FD}) occupies 33% of total decay period. Then system enter into slow decay mode. During the conversion from fast to slow decay modes, driver would be disabled for 300ns (dead time). The setting could avoid bridge throughout.

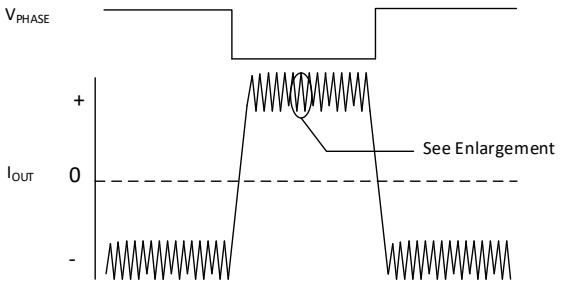


Figure 1. Mixed Decay Mode

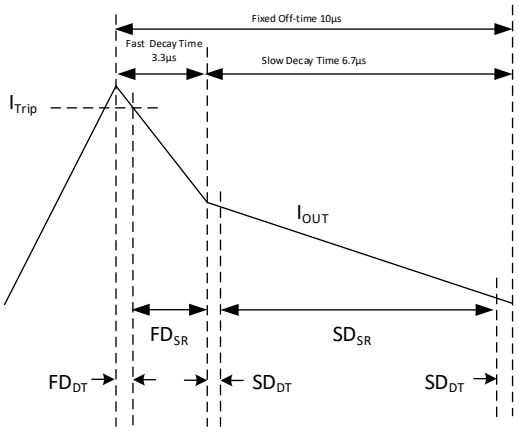
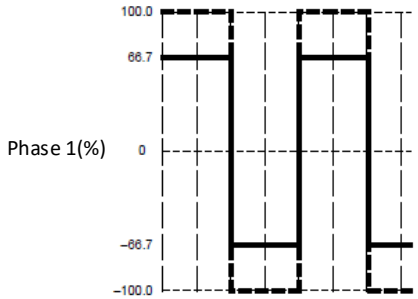


Figure 2. Enlarged View of Mixed Decay Mode

Step Sequencing Diagram



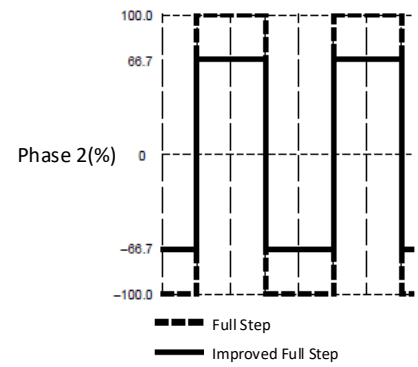
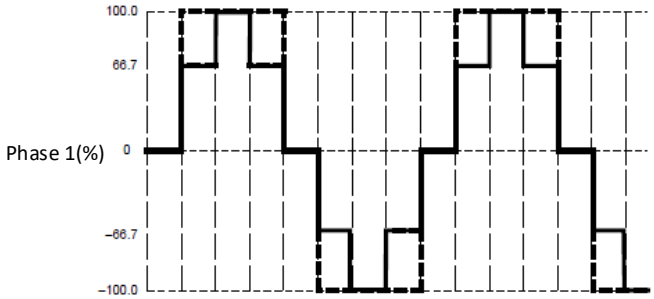


Figure 3. Step Sequencing for Full Step



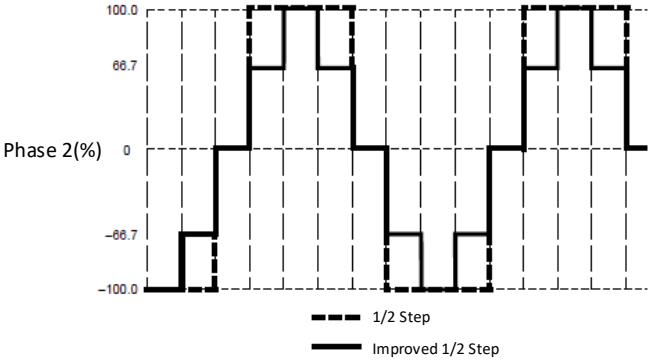
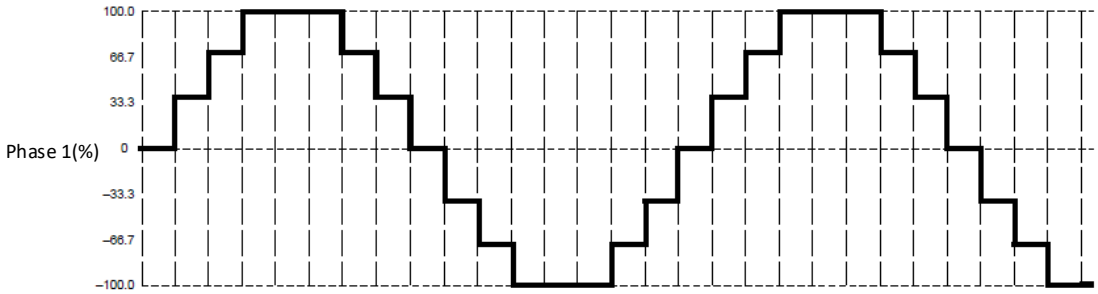


Figure 4. Step Sequencing for 1/2 Step



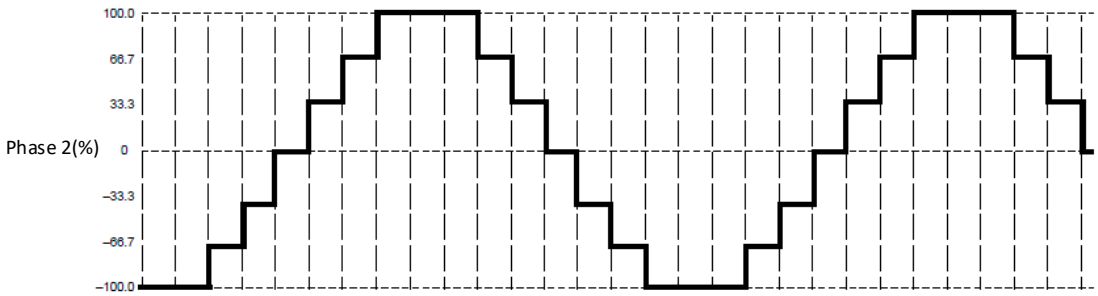


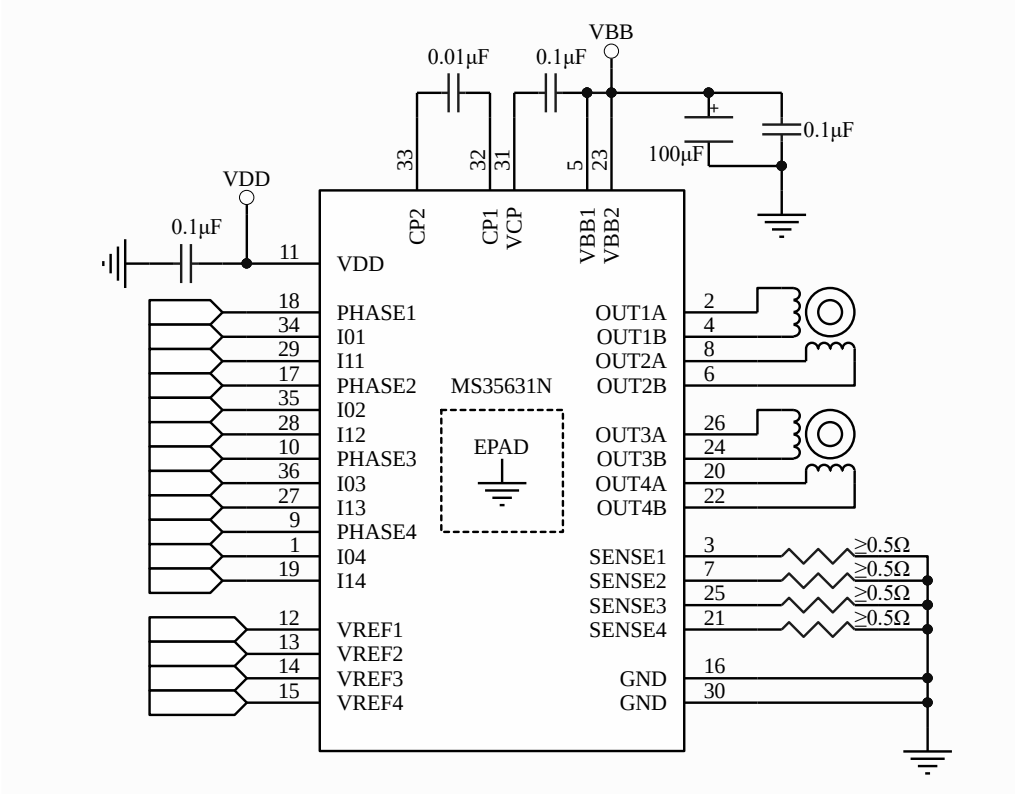
Figure 5. Step Sequencing for 1/4 Step

Step Sequencing Setting

Full	1/2	1/4	Phase 1 (% $I_{TripMax}$)	xI0	xI1	Phase	Phase 2 (% $I_{TripMax}$)	xI0	xI1	Phase
	1	1	0	H	H	X	100	L	L	0
		2	33	L	H	1	100	L	L	0
1	2	3	100/66*	L/H*	L	1	100/66*	L/H*	L	0
		4	100	L	L	1	33	L	H	0
	3	5	100	L	L	1	0	H	H	X
		6	100	L	L	1	33	L	H	1
2	4	7	100/66*	L/H*	L	1	100/66*	L/H*	L	1
		8	33	L	H	1	100	L	L	1
	5	9	0	H	H	X	100	L	L	1
		10	33	L	H	0	100	L	L	1
3	6	11	100/66*	L/H*	L	0	100/66*	L/H*	L	1
		12	100	L	L	0	33	L	H	1
	7	13	100	L	L	0	0	H	H	X
		14	100	L	L	0	33	L	H	0
4	8	15	100/66*	L/H*	L	0	100/66*	L/H*	L	0
		16	33	L	H	0	100	L	L	0

*Improved Step Mode

TYPICAL APPLICATION



DC Motor Control

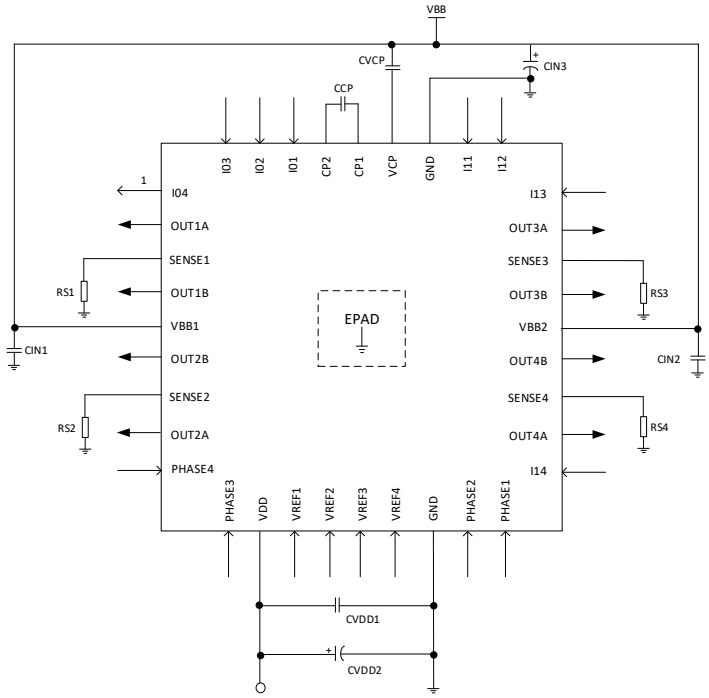
TheMS35631N/MS35631 integrates four H-bridge drives, each of which is equipped with an independent PWM current control circuit, so it can drive four DC motors. In application, the maximum current can be set by the VREF pin, and the I0x, I1x and PHASEx pins can be controlled by PWM signal to control forward rotation, reverse rotation and standby of the motor.

Layout Making

Heavy ground plane is required for printed circuit board. In order to achieve better performance and heat dissipation, the MS35631N/MS35631 should be directly soldered to the board. On the back of the MS35631N/MS35631 is a metal heat sink, which is directly soldered on the exposed PCB board to radiate heat to other layers.

Layout Ground Trace

In order to reduce ground drift, it is necessary to set one special ground trace with single point and low impedance near the chip in PCB. Generally, the position, where the grounding plane is just below the the thermal pad, is the ideal special ground trace. Special ground trace with low impedance could effectively avoid ground drift and ensure the stability of power supply.

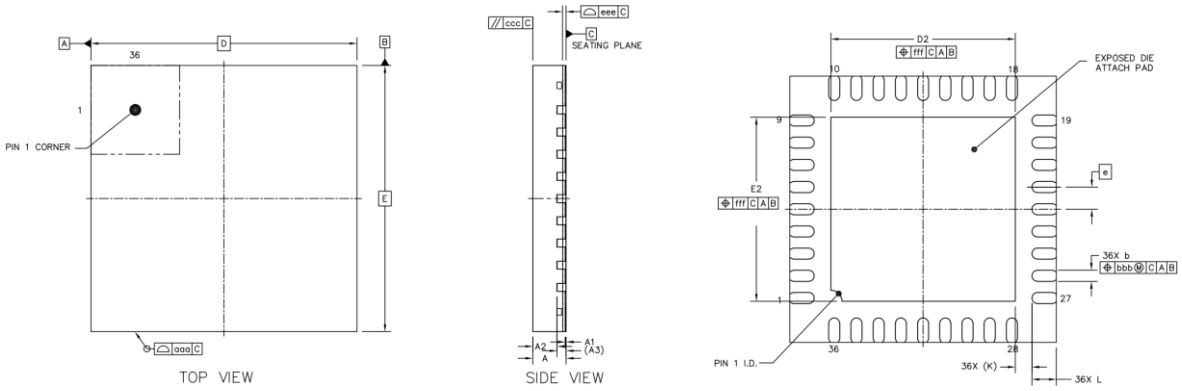


SENSE Pin Setting

R_{SENSEx} resistor on SENSE pin must be connected with one low impedance path to ground. Because R_{SENSEx} would flow through large current and generate accurate feedback voltage to SENSE comparator. Long ground trace would generate extra resistance, thus causing uncertain voltage drop and reduce the accuracy of SENSE comparator. When select SENSE resistor, note that the voltage on SENSE pin should not exceed ±500mV in operation.

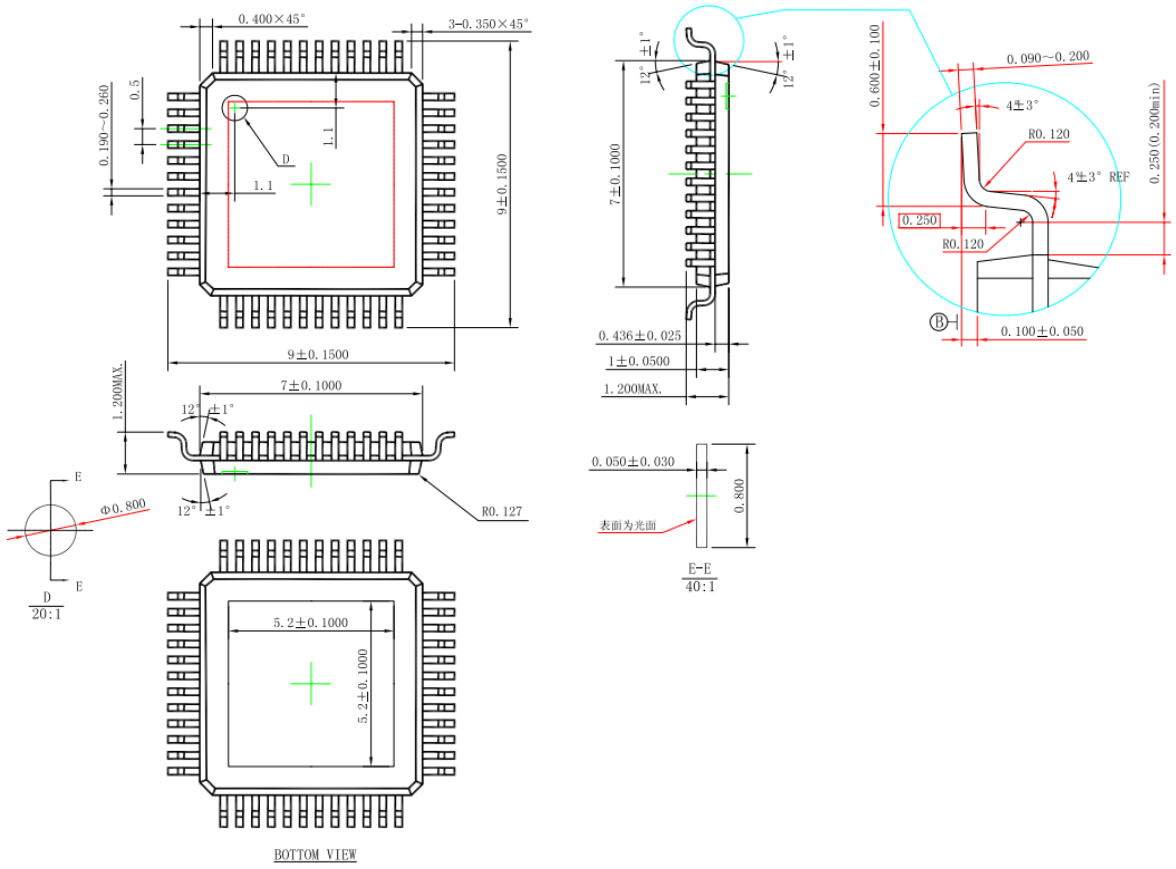
PACKAGE OUTLINE DIMENSIONS

QFN36(06X06) (Back Thermal Pad)



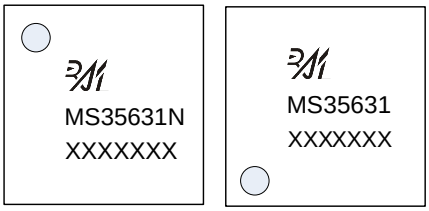
Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203REF		
b	0.2	0.25	0.3
D	6BSC		
E	6BSC		
e	0.5BSC		
D2	4.05	4.15	4.25
E2	4.05	4.15	4.25
L	0.45	0.55	0.65
K	0.375REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		

TQFP48(07X07) (Back Thermal Pad)



MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name : MS35631N, MS35631

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS35631N	QFN36	2000	1	2000	8	16000

Device	Package	Piece/Tray	Tray/Box	Piece/Box	Box/Carton	Piece/Carton
MS35631	TQFP48	250	10	2500	4	10000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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