16 Microstepping Motor Driver

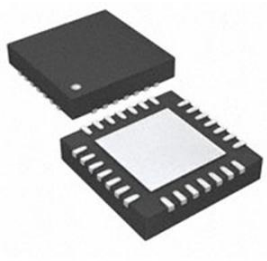
PRODUCT DESCRIPTION

The MS4988B is a bipolar microstepping motor driver with built-in 4bit DAC, which can achieve five step modes: full, 1/2, 1/4, 1/8, 1/16 step. And the MS4988B has the maximum driving capacity of 35V, ±1.5A.

The MS4988B is pulse control mode, that every time the step pin is applied to one pulse, the motor would move one microstep without phase sequence table, high-frequency control line and complex program control interface.

In addition, the MS4988B has the regulator of fixed current decay period, automatically selecting current decay mode, slow and mixed decay. The mixed decay is fast decay in previous time and slow decay in remaining time. This decay mode contributes to improve step accuracy , reduce motor noise and power dissipation.

The internal synchronous rectification circuit could reduce power dissipation. The MS4988B has protection functions, including thermal shutdown(TSD), overcurrent protection(OCP), undervoltage lockout(UVLO) and short-circuit protection and it requires no special power-on process.



QFN28

FEATURES

- Low Output On-resistance
- Automatic Current Decay Mode Selection and Detection
- Synchronous Rectification
- Mixed and Slow Decay Mode
- Compatible with Logic Input for 5V and 3.3V
- Full, 1/2, 1/4, 1/8, 1/16 Step Mode
- Thermal Shutdown , Undervoltage Lockout
- Low Current Sleep Mode(<50uA)

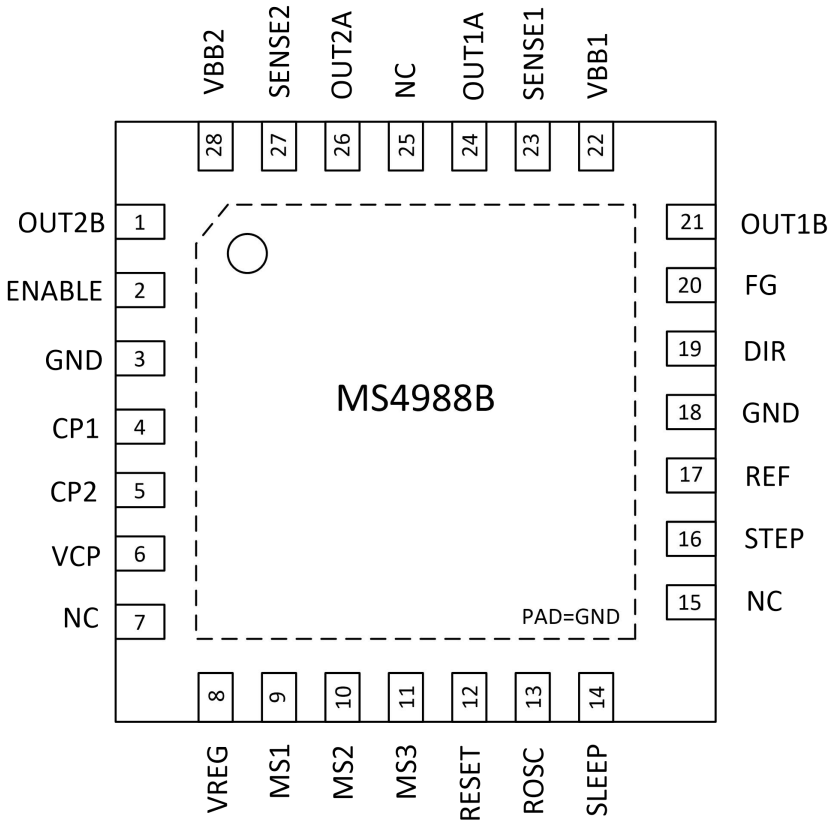
APPLICATIONS

- Security and Protection Video Monitoring
- 3D Print
- Robot Technology
- Industry Application

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS4988B	QFN28	MS4988B

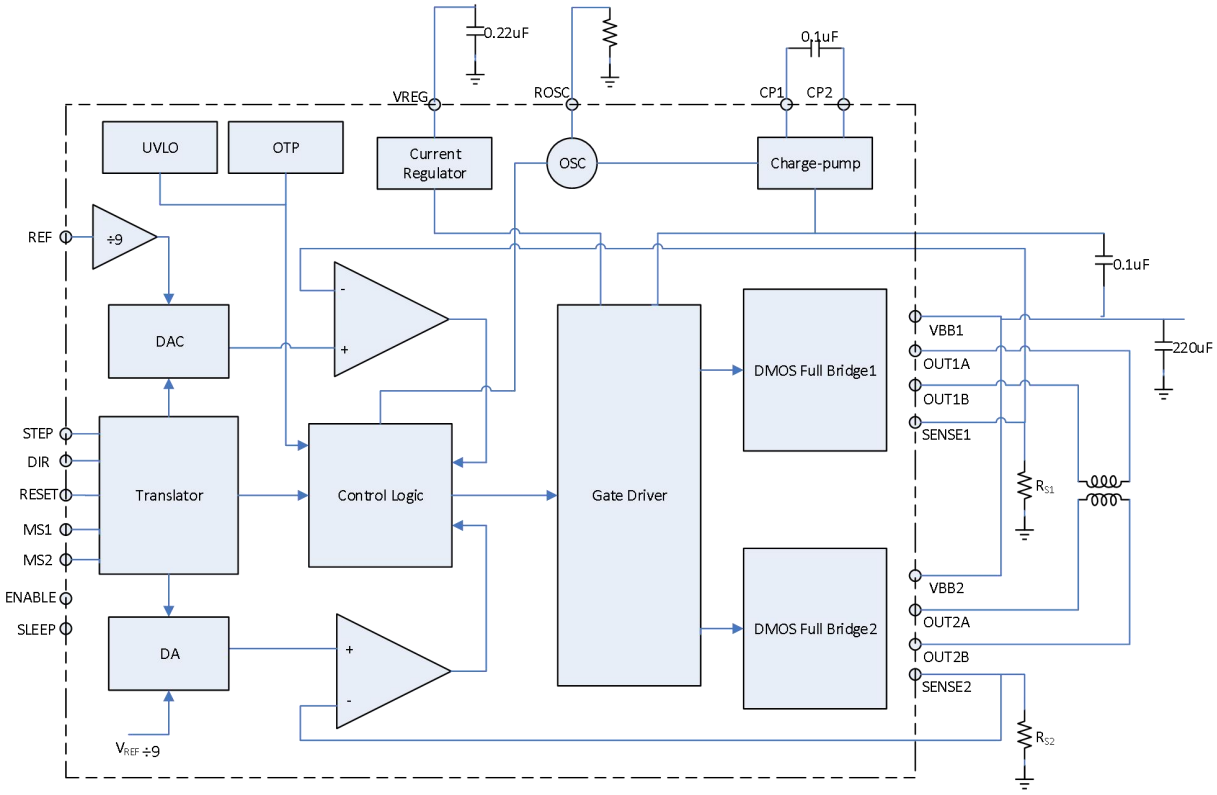
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	OUT2B	O	Output Channel Two, Terminal B
2	ENABLE	I	Output Enable
3,18	GND	I/O	Ground
4	CP1	I/O	Charge-pump Capacitor Terminal
5	CP2	I/O	Charge-pump Capacitor Terminal
6	VCP	O	Charge-pump Output
7,25	NC	-	Not Connection
8	VREG	O	Low-voltage Power Supply Output
9	MS1	I	Step Mode Control
10	MS2	I	Step Mode Control
11	MS3	I	Step Mode Control
12	RESET	I	Reset
13	ROSC	I/O	Current Decay Control
14	SLEEP	I	Sleep Mode
15	NC	-	Not Connection
16	STEP	I	Step Clock
17	REF	I	DAC Power Supply
19	DIR	I	Forward/Reverse Mode
20	FG	O	Fault Detection Output
21	OUT1B	O	Output Channel One, Terminal B
22	VBB1	I/O	High-voltage Load Power 1
23	SENSE1	I/O	Output Current Detection 1
24	OUT1A	O	Output Channel One, Terminal A
26	OUT2A	O	Output Channel Two, Terminal A
27	SENSE2	I/O	Output Current Detection 2
28	VBB2	I/O	High-voltage Load Power 2
-	PAD	-	Thermal Pad, must be connected to ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Maximum Operating Voltage	V_{BB}	35	V
Output Current	I_{OUT}	±1.5	A
Logic Input Voltage	V_{IN}	-0.3 ~ 5.5	V
Motor Output Voltage		-2 ~ 37	V
SENSE Voltage	V_{SENSE}	-0.5 ~ 0.5	V
Reference Voltage	V_{REF}	5.5	V
Operating Temperature	T_A	-20 ~ 85	°C
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{str}	-55 ~ 150	°C

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Load Power Supply	V_{BB}	Operation Mode	5.5		35	V
		Sleep Mode				
On-resistance (HS)	$R_{ON(H1)}$	I_O=-1.5A		400		mΩ
On-resistance (LS)	$R_{ON(L1)}$	I_O=-1.5A		330		mΩ
Diode Forward Voltage (HS)	$V_{D(H1)}$	I_D=1.5A			1.2	V
Diode Forward Voltage (LS)	$V_{D(L1)}$	I_D=1.5A			1.2	V
Load Power Supply Current	I_{BB}	F_{PWM}<50kHz		5		mA
		Normal Operation, Output Disabled		1.8		mA
		Sleep Mode		46		uA
High Input Voltage	$V_{in(1)}$		0.6×VREG			V
Low Input Voltage	$V_{in(0)}$				0.4×VREG	
Logic Input Delay	$V_{HYS(IN)}$	a % of VREG	5	11	19	%
Step Mode	R_{MS1}	MS1 pin		400		kΩ
	R_{MS2}	MS2 pin		400		
	R_{MS3}	MS3 pin		400		
Blank Time	t_{Blank}			1.6		us
Fixed Decay Period	t_{Off}	ROSC=VREG or GND	20	30	40	us
		ROSC=25kΩ	23	30	37	us
REF Input Voltage	V_{REF}		0		5	V
REF Input Current	I_{REF}			<1		nA
Dead Time	t_{DT}			500		ns
Thermal Shutdown	T_{TSD}			167		°C
Thermal Shutdown Hysteresis	Y_{TSDHYS}			15		°C
Logic Power Undervoltage Protection	VREGuvlo	VREG Rise		2.6		V
Logic Power Protection Hysteresis	HYSVREG			0.1		V
Load Power Undervoltage Protection	VBBuvlo	VBB Rise		5.2		V
Load Power Protection Hysteresis	HYSVBB			0.2		V
Built-in LDO : VREG						
VREG Output Voltage	V_{vreg}		4.8	5.1	5.4	V
VREG Output Impedance	R_{vreg}			10		Ω
VREG Output Load Capacity	$I_{outlimit}$	VREG Dropping to 4.5V		50		mA
VREG Power Supply Rejection Ratio	$R_{VREGvsVBB}$	VBB Input 5Hz		60		dB

FUNCTION DESCRIPTION

Chip Operation

The MS4988B can achieve five microstep modes, selecting full, 1/2, 1/4, 1/8, 1/16 step mode according to MSx pin. The current in two full-bridges made up of NDMOS are regulated synchronously through PWM control circuit with fixed decay period. Each step output current depends on V_{REF} , external SENSE resistance and DAC output voltage.

When power-on and reset, DAC output and phase current polarity are set as initial HOME state (HOME state is the 0.707 position of DAC maximum output voltage), and current rectification is the mixed decay mode at each phase. When STEP command occurs, DAC output and current polarity start normal operation. The step resolution is controlled by MSx, as shown in table 1.

When stepping falls, the decay mode is mixed decay. While when stepping rises, the decay mode is slow decay. This operation mode is called automatic decay mode, which improves motor operating performance and reduces current waveform distortion caused by motor back-EMF.

Microstepping Control (MS1, MS2and MS3)

The microstep resolution is controlled by MS1, MS2and MS3, as shown in table 1. There is a 400kΩ pull-up resistor in MSx. Only after detect the rising edge of STEP signal, step mode switch is performed.

If need to change step mode, the translator is reset. Otherwise must switch on the common step position of the two step modes, in order not to lose step. When chip is power down reset due to thermal shutdown and overcurrent protection, the translator would be set as HOME state to correct all step modes.

Motor step mode truth table (IN=''High"represents $IN^+ > IN^-$).

Table 1. Step Mode Control Truth Table

MS3	MS2	MS1	Step Mode
L	L	L	Full
L	L	H	1/2
L	H	L	1/4
L	H	H	1/8
H	L	L	1/16

Reset Terminal (RESET)

When reset is valid, the translator is set as HOME state, and all output FETs are disabled. Until RESET is placed as high level, STEP signal is valid again.

STEP Input (STEP)

One step rising edge makes motor operate one microstep. Translator controls DAC output value and the current direction of each winding. The step resolution depends on MSx.

Direction Control (DIR)

DIR pin control motor rotation direction and starts detection when each STEP rising edge occurs.

Internal PWM Current Control

Each full bridge is controlled by PWM circuit with fixed decay period. The circuit limits the expectation value of load current (I_{TRIP}). At first, the diagonal high and low side FETs are enabled, then current flows through motor winding and SENSE resistor R_{Sx}. When the voltage on SENSE resistor is equal to DAC voltage, comparator clears PWM latch. The PWM latch chooses to disable appropriate FET and enter fixed-period decay mode.

The maximum limiting current is determined by R_{Sx} and $V_{REF.}$ The transconductance formula is as followed.

$$I_{TREPMAX}=V_{REF} / (9.0\times R_S)$$

Fixed Off-Time

Internal PWM current control circuit uses one-shot circuit to control the duration of time that the DMOS FETs shutdown. The off-time, t_{off} depends on ROSC terminal:

ROSC connected to VREG : Current decay period is 30us, and decay mode is mixed decay for all step modes (rising slow decay, falling mixed decay);

ROSC connected to GND : Current decay period is 30us, and when current increases and decrease, decay mode is mixed decay for all step modes;

ROSC connected to GND through resistor : Decay mode is mixed decay for all step modes (rising slow decay, falling mixed decay).

Decay decay period is dependant on following formula: $T_{off}=R_{OSC}/825$.

Blank Time

The reverse current, generated by parasitic diode, would cause false overcurrent detection. In order to avoid this phenomenon , setting 1us blank time makes the detection signal ineffective during the period.

Load Shorted Protection and Ground Protection

When motor loads are shorted together or directly connected to ground, the chip would detect overcurrent and disable shorted FET, avoiding damage to internal devices. After shorted protection operates, it is necessary to make SLEEP high or VBB low to recover normal operation.

When two outputs are shorted, current flows through SENSE resistor. After 1us, the voltage on SENSE resistor meets fault condition, which makes driver enter fixed decay period. After the decay period, the driver turns on again and the process repeats. Under this condition, the driver is immune to overcurrent completely. But short circuit would last the period of time equaling to fixed decay period.

Charge- pump (CP1 and CP2)

Charge-pump is used to generate the voltage more than VBB to drive high-side FET. The voltage is gradually increased through CP between CP1 and CP2, then is gradually accumulated through CG between VG and VCC.

The relationship between CP and CG is as followed.

CP charge and discharge frequency is 60kHz. When CP capacitance is very large, VG would be increased. While if the capacitance is too large, charge and discharge would become inefficient and VG charge time would be very long. CP and CG are set as: CP=0.22uF, CG=0.22uF.

Output Control Power Supply VREG

The internal generated power supply is used to drive output low-side FET. It is usually set as 5.1V and 0.22uF ceramic capacitor is connected to VREG pin. If fault occurs (low voltage), the internal structure of detecting VREG would disable all outputs.

ENABLE

ENABLE can enable and disable all FETs. When ENABLE is logic 1, all FETs are disabled; When ENABLE is logic 0, circuit operates normally. However, the translator input pins are constrained against ENABLE pin, such as STEP, DIR, MS1, MS2, MS3.

Shutdown

When thermal shutdown or undervoltage lockout performs, all FETs are disabled until fault is solved. When power on, undervoltage lockout also disables outputs and sets translator as HOME state.

SLEEP Mode

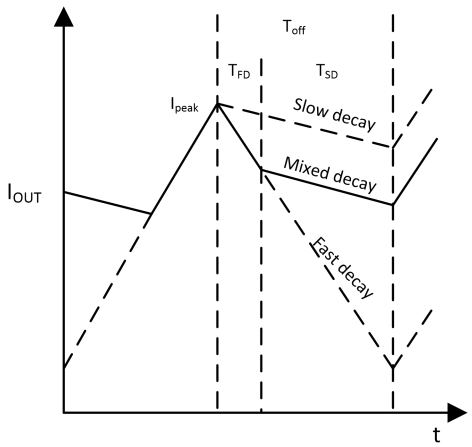
In order to reduce standby power dissipation, SLEEP would turn off most functions, including FETs, current regulator and charge-pump. SLEEP active low and when it becomes high, chip operates normally. When motor recoveries from sleep mode, there is usually about 1ms delay time to make charge-pump stable.

Mixed Decay Mode

In mixed decay mode, when current value reaches the trip value, the chip would first enter fast decay mode, occupying about 31.25% of total decay period, then turn to slow decay.

In general, mixed decay is only needed to apply to current decreasing state. For most loads, adopting automatic mixed decay mode (current increasing slow decay, current decreasing fast decay) could reduce ripples caused by increasing current and avoid step loss caused by decreasing current. For some slow-speed microstepping applications, because back-EMF is very small, the load current rapidly increases, causing step loss. ROSC is tied to ground, which realizes 100% mixed decay when current increases and decreases, avoiding step loss.

If without the problem, for the sake of reducing ripples, it is suggested to adopt automatic mixed decay mode.



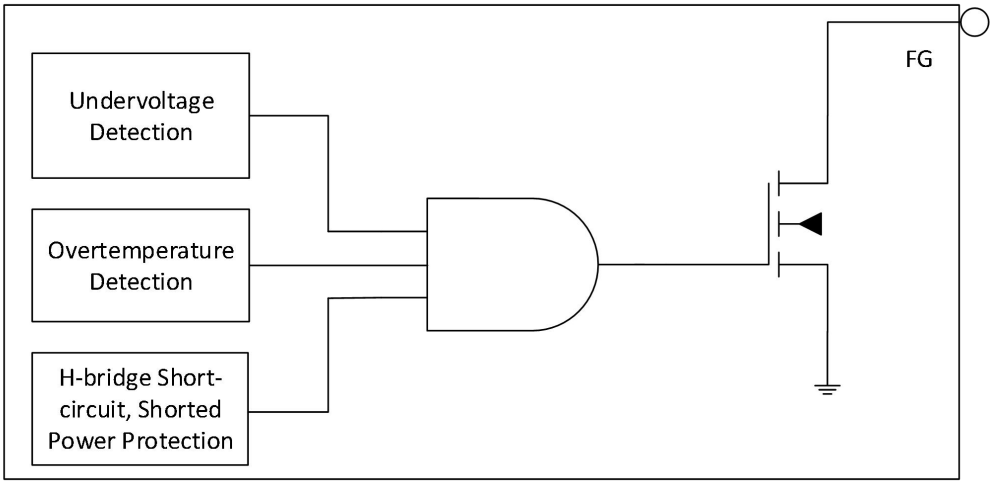
I_{peak} Maximum Output Current , T_{off} Fixed Off-time , T_{SD} Slow Decay Time , T_{FD} Fast Decay Time.

Synchronous Rectification

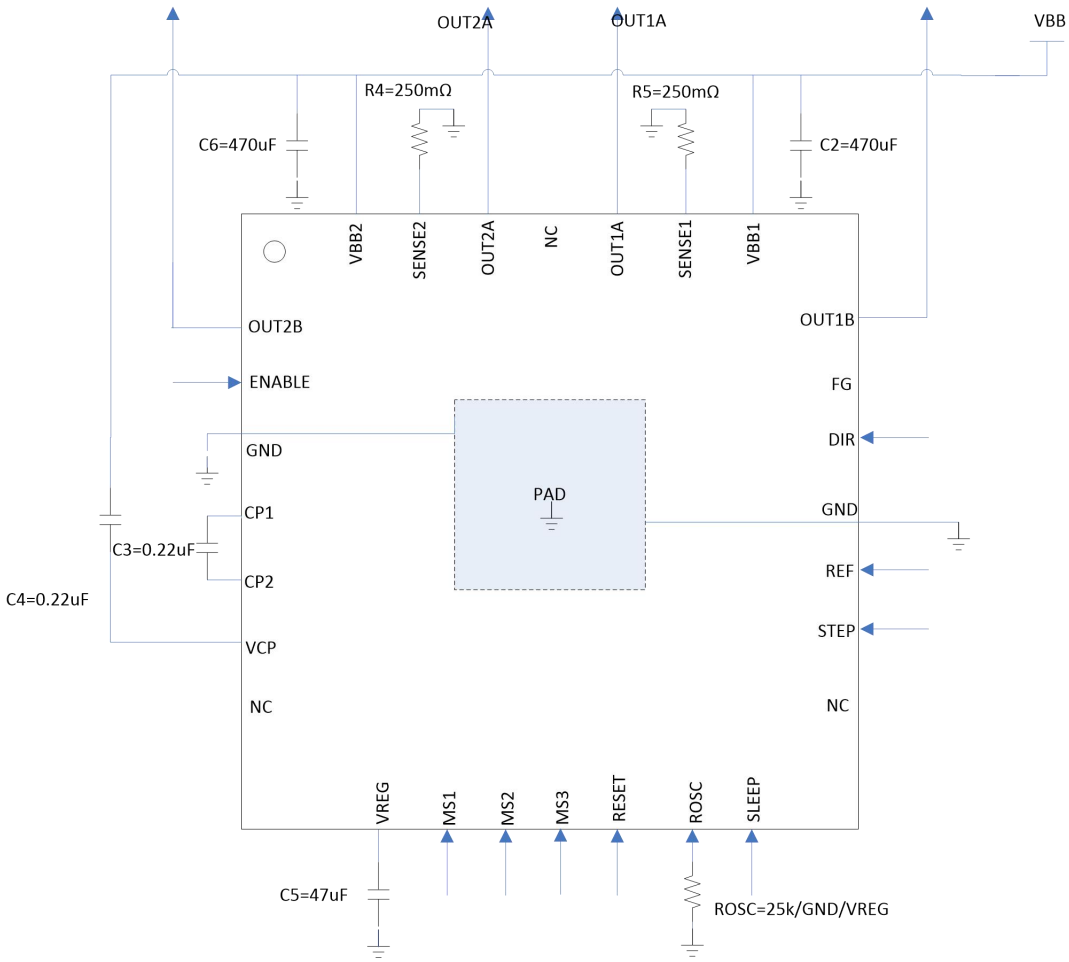
When chip enters decay period, load currents would continue flowing according to selected decay mode. The feature is that turn on appropriate FET when current decays. Low FET on-resistance shorts out the regeneration diode, which reduces power dissipation effectively and saves uses of Schottky diodes in other applications. When load current approaches 0, synchronous rectification is off to prevent reverse load current.

FG Output

When detection module detects abnormal situation, FG outputs low level with open drain, and maximum pull-down current is 15mA.



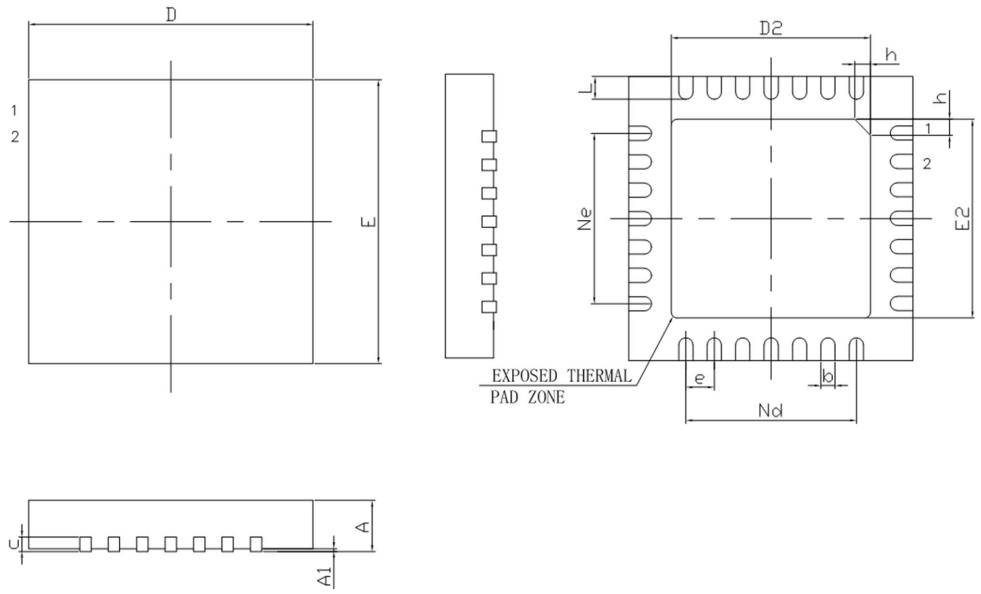
TYPICAL APPLICATION DIAGRAM



PACKAGE OUTLINE DIMENSIONS

QFN28

QFNWB5×5-28L(P0.50T0.75/0.85)



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.700	0.750	0.800
A1	-	0.02	0.050
b	0.180	0.250	0.300
c	0.180	0.200	0.250
e	0.500TYP		
D	4.900	5.00	5.100
D2	3.400	3.500	3.600
Ne	3.00BSC		
Nd	3.00BSC		
E	4.900	5.000	5.100
E2	3.400	3.500	3.600
L	0.350	0.400	0.450
h	0.300	0.350	0.400
L/F Carrier (mil)	150×150		

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name : MS4988B

Product Code : XXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS4988B	QFN28	1000	10	10000	4	40000

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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