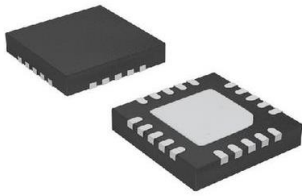
Spurious-free, 2.1GHz, Dual-loop Fractional-N Frequency Synthesizer

PRODUCT DESCRIPTION

The MS72300 is a dual-loop, fractional-N frequency synthesizer, which includes main-loop and auxiliary-loop phase-locked loop. And it is featured with extremely high frequency resolution, fast switching speed of output frequency and low phase-noise. The maximum operating frequency of the main loop is 2.1GHz, which is suitable for wireless communication system. And the auxiliary loop is suitable for frequency applications below 500MHz. The MS72300 adopts three-wire high-speed serial interface, combined with large loop bandwidth and high frequency resolution, which allows frequency modulation of the main-loop external VCO. Its characteristics is suitable for any modulation schemes with continuous phase and constant envelope, such as Frequency Modulation (FM), Frequency Shift Keying (FSK), Minimum Shift Keying (MSK) and Gaussian Minimum Shift Keying (GMSK).



QFN24

FEATURES

- Spurious-free Operation
- Maximum Operation Frequency: Main Loop: 2.1GHz, Auxiliary Loop: 0.5GHz
- High Frequency Resolution: below 100Hz
- High Internal Reference Frequency, Support Large Loop Bandwidth
- Fast Output Frequency Switching: below 100μs
- Phase Noise inside the Main-loop Bandwidth -91dBc/Hz@1800MHz
- Software Programmable Power-down Modes
- High-speed Serial Interface: 100Mbps
- Three-wire SPI Interface
- Programmable Division Ratios on Reference Frequency
- Phase detectors with programmable gain, Support Programmable Loop Bandwidth.
- Fast Lock function further shortens acquisition time.
- On-chip Crystal Oscillator Circuit
- Frequency Calibration for Temperature Compensation
- 3V Core Power Supply
- 3V ~ 5V Charge Pump Power Supply

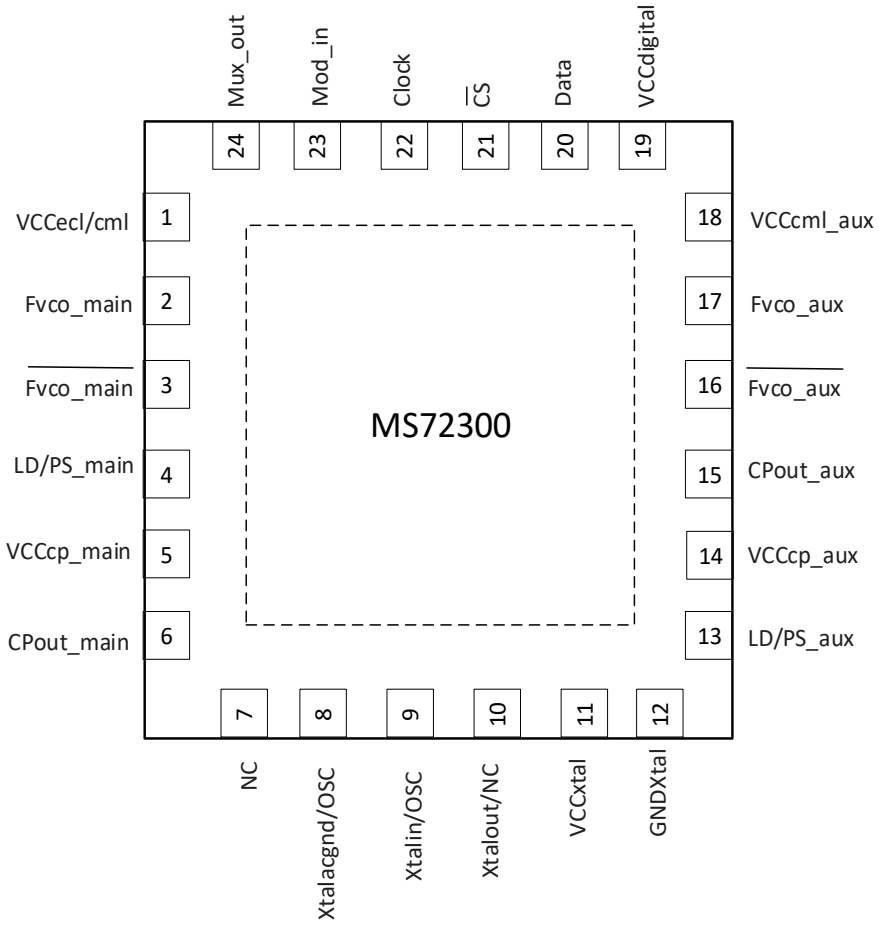
APPLICATIONS

- General RF Systems
- 2.5G/3G Wireless Infrastructure
- Broadband Wireless Access
- Wireless Telemetry with Low Bit Rate
- Instrumentation
- L-band Receivers
- Satellite Communications

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS72300	QFN24	MS72300

PIN CONFIGURATION

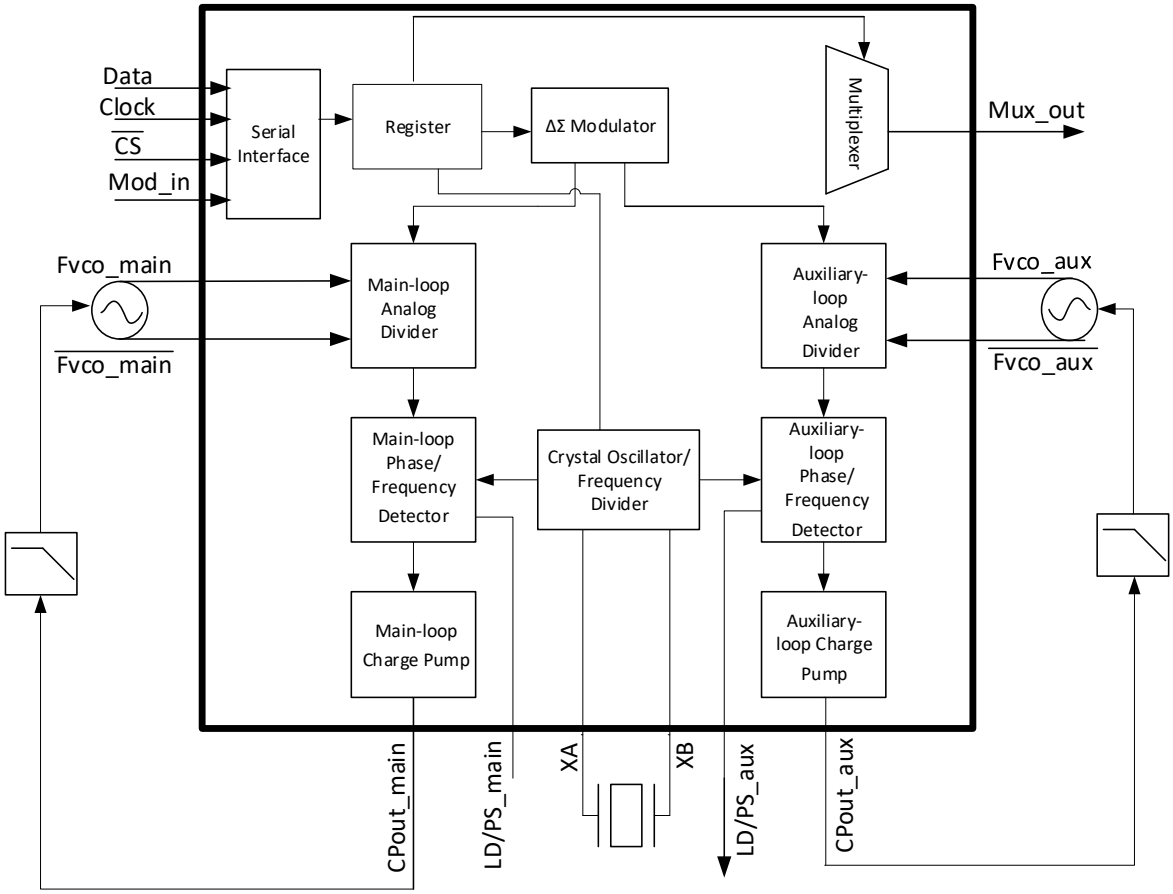


PIN DESCRIPTION

Pin	Name	Type	Description
1	VCCecl/cml	-	Main ECL/CML Power Supply
2	Fvco_main	I	Main VCO Differential Positive Input.
3	$\overline{\text{Fvco\_main}}$	I	Main VCO Differential Negative Input.
4	LD/PS_main	O	Main-loop Programmable Output Pin： lock detection or fast lock enabling. The pin is configured by using the phase detector /charge pump control register. When the corresponding bit of this register is 0, this pin serves as lock detection, and the collector is in open-circuit output state. When in low level, it indicates loss of lock. When in high level, it indicates lock; When the corresponding bit of this register is 1, this pin serves as fast lock enabling.
5	VCCcp_main	-	Main Charge Pump Power Supply
6	CPout_main	O	Main Charge Pump Output. The gain of charge pump/phase detector is configured by phase detector/charge pump control register.
7	NC	-	No Connection
8	Xtalacgnd/OSC	-/I	Reference Crystal AC Ground or External Crystal Oscillator Differential Input
9	Xtalin/OSC	I	Reference Crystal Input or External Crystal Oscillator Differential Input
10	Xtalout/NC	O/-	Reference Crystal Output or No Connection
11	VCCxtal	-	Crystal Power Supply
12	GNDxtal	-	Crystal Ground
13	LD/PS_aux	O	Auxiliary-loop Programmable Output Pin: lock detection or fast lock enabling. The pin is configured by using the phase detector /charge pump control register. When the corresponding bit of this register is 0, this pin serves as lock detection, and the collector is in open-circuit output state. When in low level, it indicates loss of lock. When in high level, it indicates lock; When the corresponding bit of this register is 1, this pin serves as fast lock enabling.

Pin	Name	Type	Description
14	VCCcp_aux	-	Auxiliary Charge Pump Power Supply
15	CPout_aux	O	Auxiliary Charge Pump Output. The gain of charge pump/phase detector is configured by phase detector/charge pump control register.
16	$\overline{\text{Fvco\_aux}}$	I	Auxiliary VCO Differential Negative Input
17	Fvco_aux	I	Auxiliary VCO Differential Positive Input
18	VCCcml_aux	-	Auxiliary ECL/CML Power Supply
19	VCCdigital	-	Digital Power Supply
20	Data	I	Serial Address and Data Input Pin. Address bits are followed by data bits.
21	$\overline{\text{CS}}$	I	Low Active Enable Pin. Address and data are loaded to Data pin on the rising edge of Clock pin. When $\overline{\text{CS}}$ is high, data is transferred to the register specified by the address, subsequent clock edges are ignored.
22	Clock	I	Clock Pin. When $\overline{\text{CS}}$ is low, register address and data are transferred to register on the rising edge of Clock (Address bits are shifted firstly)
23	Mod_in	I	Selectable Serial Modulation Data Input Pin. Address bits are followed by data bits.
24	Mux_out	O	Internal Multiplexer Output Pin. Selectable output oscillator clock, reference frequency batch clock, divided VCO clock, serial data or test signals. This pin can control tri-state output by synthesizer register.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Range	Unit
Maximum Analog RF Supply Voltage	3.6	V
Maximum Digital Supply Voltage	3.6	V
Maximum Charge Pump Supply Voltage	5.5	V
Storage Temperature	-65 ~ +150	℃
Operating Temperature	-40 ~ 125	℃
Soldering Temperature (10s)	260	℃

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit
Analog RF Power Supply	2.7	3	3.3	V
Power Supply of Crystal Oscillator Circuit	2.7	3	3.3	V
Digital Power Supply	2.7	3	3.3	V
Charge Pump Power Supply	2.7		5.25	V
Operating Temperature	-40	25	125	℃

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, Power Supply: 3V, Operating Temperature: 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Dissipation						
Total Power Dissipation	P_{TOTAL}	Charge-pump Current: 200μA, Main and Auxiliary Loops Fully Open, Both Synthesizer Fractional, f_{ref_main} =20MHz, f_{ref_aux} = 1MHz		48		mW
		Charge-pump Current: 200μA, Auxiliary Loop Closed, Synthesizer Fractional, f_{ref_main} = 20MHz		25.5		mW
Power-down Current	$I_{CC-PWDN}$	3V Charge Pump		1.6		mA
		5V Charge Pump		2.0		mA
Reference Oscillator						
Reference Oscillator Frequency	f_{OSC}				50	MHz
Oscillator Sensitivity (As a Buffer)	V_{OSC}	AC Coupled, Single-ended	0.05		0.4	Vpp
Frequency Shift VS. Voltage	F_{SHIFT_SUPPLY}	2.7V ≤ V_{XTAL} ≤ 3.3V	-0.5		0.5	ppm
Voltage Controlled Oscillator VCO						
Synthesizer Operating Frequency	f_{VCO_MAIN}	Sinusoidal, -40°C to 125 °C, Main-loop	100 [1]		2100	MHz
	f_{VCO_AUX}	Sinusoidal, -40°C to 125 °C, Auxiliary-loop	100 [1]		500	MHz
RF Input Sensitivity	V_{VCO}	AC Coupled	50		350	mV_{peak}
RF Input Resistance	Z_{VCO_IN}	Single-ended		58–j70 @1200MHz		Ω

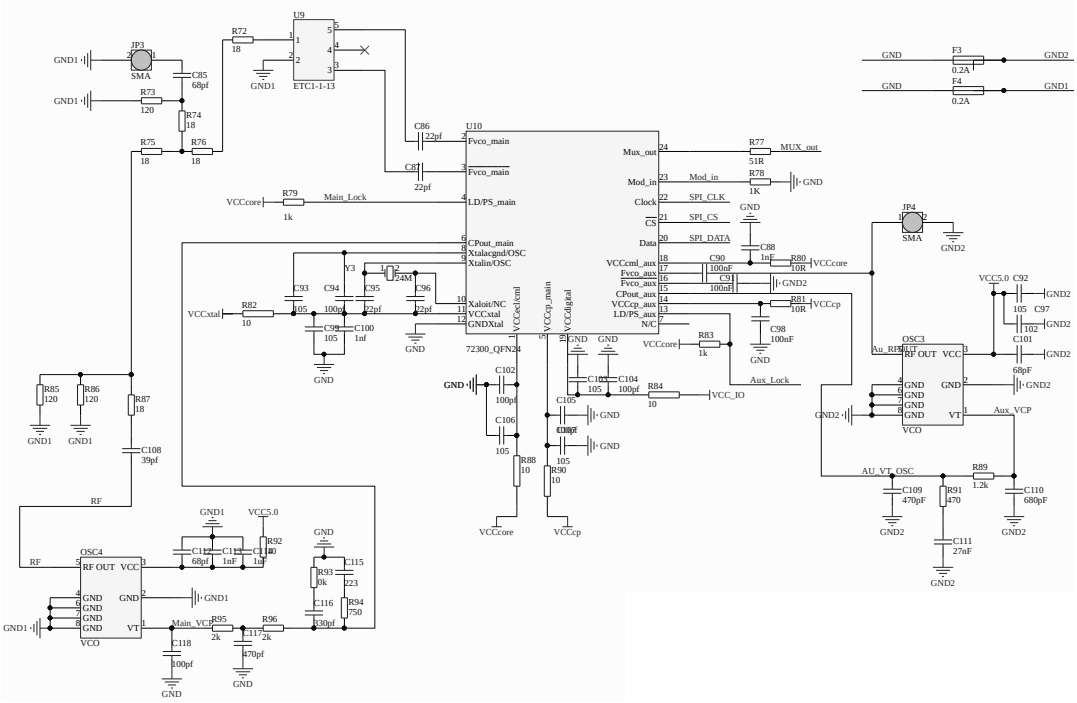
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Fractional-N Frequency Resolution	f_{STEP_MAIN}		$F_{ref\_main}/2^{18}$ or $F_{ref\_main}/2^{10}$			Hz
	f_{STEP_AUX}		$F_{ref\_aux}/2^{10}$			Hz
Noise						
Phase Noise Floor	P_{nf}	Using 25MHz Reference Frequency, inside the Loop Bandwidth		-131 +20Log(N) [2]		dBc/Hz
Phase Detectors and Charge Pumps						
Phase Detectors Operating Frequency	f_{ref_main}	-40°C to 125 °C			25	MHz
	f_{ref_aux}	-40°C to 125 °C			12.5	MHz
Charge-pump Source Current	$I_{CP-SOURCE}$	VCP = 0.5 VCC_{CP}	100		800	μA
Charge-pump Sink Current	$I_{CP-SINK}$	VCP = 0.5 VCC_{CP}	-100		-800	μA
Charge-pump Accuracy	$I_{CP\_ACCURACY}$				±25	%
Charge-pump Output Voltage Linear Range	I_{CP} VS. V_{CP}	0.5 V ≤V_{CP} ≤(VCC_{CP}– 0.5 V)	GND+ 400		VCC_{CP} -400	mV
Charge-pump Current VS. Temperature	I_{CP} VS. T	V_{CP} = 0.5 VCC_{CP} -40°C to 125 °C			5	%
Charge-pump Current VS. Voltage	I_{CP} VS. V_{CP}	0.5 V ≤V_{CP} ≤(VCC_{CP}– 0.5 V)			8	%
Digital Pins						
High-level Input Voltage	V_{IH}		0.7×V_{DIGITL}			V
Low-level Input Voltage	V_{IL}				0.3×$V_{DIGITAL}$	V
High-level Output Voltage	V_{OH}	I_{OH} = -2mA	$V_{DIGITAL}$ -0.2			V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low-level Output Voltage	V_{OL}	I_{OL} = +2mA			GND+0.2	V
Timing-serial Interface						
Clock Frequency	f_{CLOCK}	Clock Pin			100	MHz
Set-up Time	t_{SU}	Time for Data and $\overline{CS}$ to Remain Unchanged before the Rising Edge of CLOCK	3			ns
Hold Time	t_{HOLD}	Time for Data and $\overline{CS}$ to Remain Unchanged after the Rising Edge of CLOCK	1			ns

Note: 1. The minimum synthesizer frequency is $12 \times f_{OSC}$, f_{OSC} is the clock frequency on the X_{talin}/OSC pin.

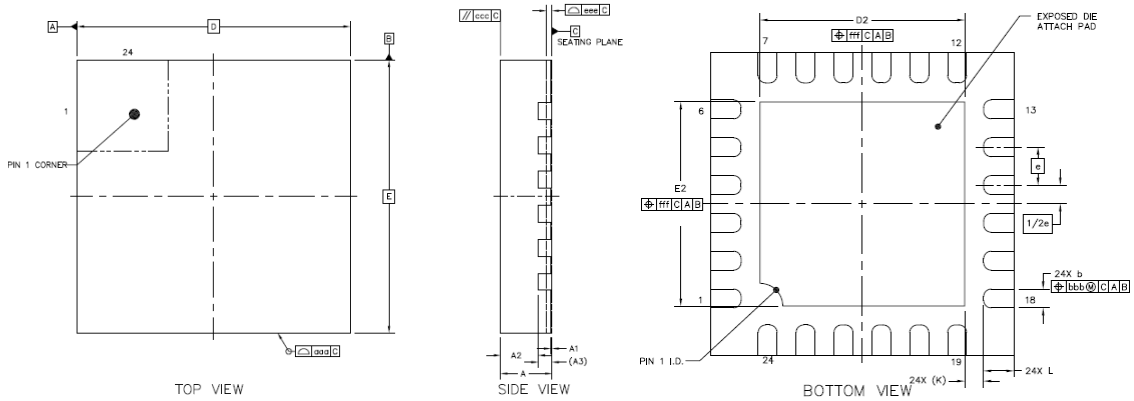
2. N is the synthesizer division ratio.

TYPICAL APPLICATION



PACKAGE OUTLINE DIMENSIONS

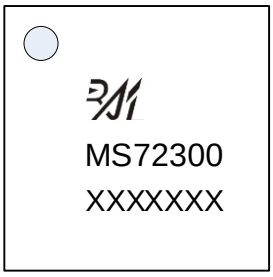
QFNWB4×4-24L (P0.5T0.75)



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.2	0.25	0.3
D	4 BSC		
E	4 BSC		
e	0.5 BSC		
D2	2.6	2.7	2.8
E2	2.6	2.7	2.8
L	0.3	0.4	0.5
K	0.2 MIN		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name: MS72300

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS72300	QFN24	4000	1	4000	8	32000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.


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