

4-bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Application

PRODUCT DESCRIPTION

The MS4554N/MS4554N1 is a bidirectional voltage-level translator that can be used in a mixed-voltage digital signal system. It is powered by two separate architectures. The power supply range of terminal A is 1.65V to 5.5V, and that of terminal B is 2.3V to 5.5V. It can be used in logic signal conversion systems with power supply voltage of 1.8V, 2.5V, 3.3V and 5V. When OE terminal is low level, all IO terminals are in high impedance state, which significantly reduces the static power dissipation. To ensure that the terminal maintains high impedance during power up or power down, OE terminal should be grounded by a pulldown resistor whose resistance value is determined by the ability to drive the current source.

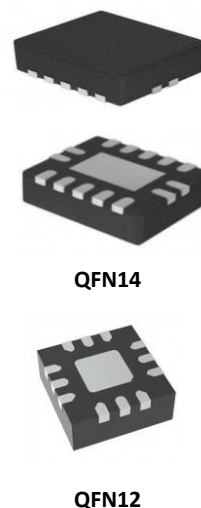
The MS4554N has lead QFN14 package, and the MS4554N1 has lead QFN12 package. Operating temperature range is from -40°C to +125°C.

FEATURES

- No Need for Direction Control
- Data Rate: 10Mbps (Push-Pull Mode) , 2Mbps (Open-Drain Mode)
- A Terminal Voltage Range: 1.65V to 5.5V
- B Terminal Voltage Range: 2.30V to 5.5V($V_{CCA} \leq V_{CCB}$)
- VCC Isolation: If VCCA or VCCB is low level to GND, IO terminals are in high impedance state
- No Power Up Sequencing Requirement
- Support Power Down Mode

APPLICATIONS

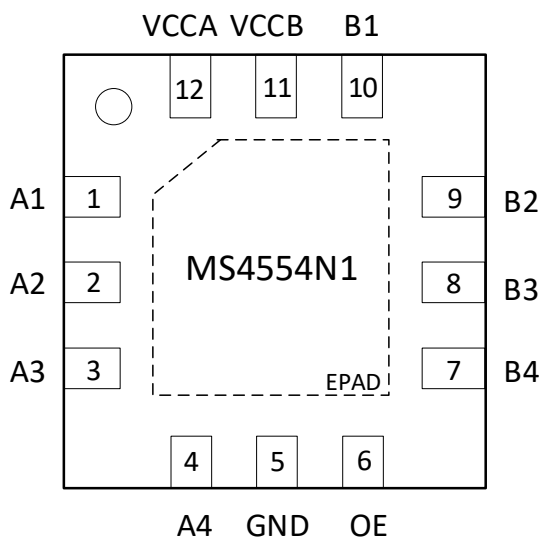
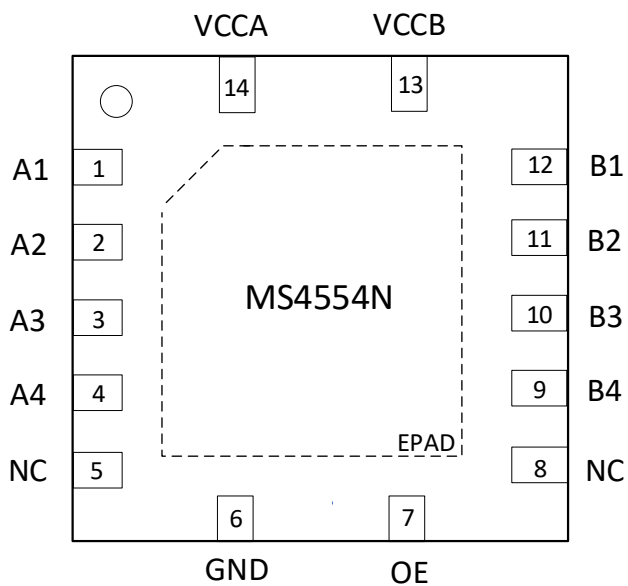
- SPI, MICROWIRE, and I²C Level Translation
- Low-Voltage ASIC Level Translation
- Smart Card Readers
- Cell-Phone Cradles
- Portable POS Systems
- Portable Communication Devices
- Low-Cost Serial Interfaces



PRODUCT SPECIFICATION

Part Number	Package	Marking
MS4554N	QFN14	MS4554N
MS4554N1	QFN12	MS4554

PIN CONFIGURATION



PIN DESCRIPTION

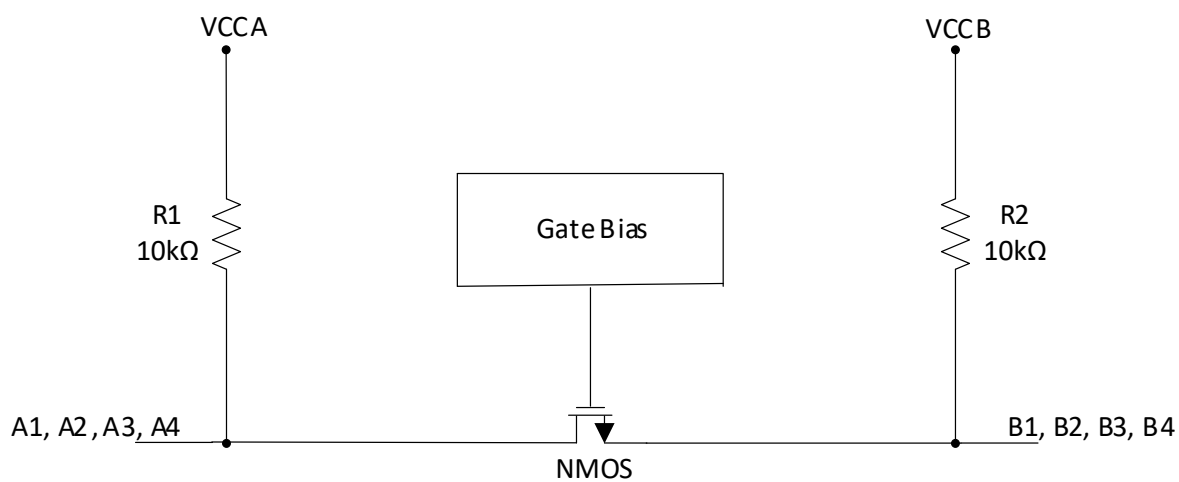
MS4554N

Pin	Name	Type	Description
1	A1	I/O	Input/Output A1, Referenced VCCA
2	A2	I/O	Input/Output A2, Referenced VCCA
3	A3	I/O	Input/Output A3, Referenced VCCA
4	A4	I/O	Input/Output A4, Referenced VCCA
5	NC	-	No Connection
6	GND	-	Ground
7	OE	I	Enable Output, pull OE low, all outputs are set to high impedance state
8	NC	-	No Connection
9	B4	I/O	Input/Output B4, Referenced VCCB
10	B3	I/O	Input/Output B3, Referenced VCCB
11	B2	I/O	Input/Output B2, Referenced VCCB
12	B1	I/O	Input/Output B1, Referenced VCCB
13	VCCB	-	B Terminal Power Supply, $2.3V \leq V_{CCB} \leq 5.5V$
14	VCCA	-	A Terminal Power Supply, $1.65V \leq V_{CCA} \leq 5.5V$, $V_{CCA} \leq V_{CCB}$
-	EPAD	-	Connect to Ground or Not Connection

MS4554N1

Pin	Name	Type	Description
1	A1	I/O	Input/Output A1, Referenced VCCA
2	A2	I/O	Input/Output A2, Referenced VCCA
3	A3	I/O	Input/Output A3, Referenced VCCA
4	A4	I/O	Input/Output A4, Referenced VCCA
5	GND	-	Ground
6	OE	I	Enable Output, pull OE low, all outputs are set to high impedance state
7	B4	I/O	Input/Output B4, Referenced VCCB
8	B3	I/O	Input/Output B3, Referenced VCCB
9	B2	I/O	Input/Output B2, Referenced VCCB
10	B1	I/O	Input/Output B1, Referenced VCCB
11	VCCB	-	B Terminal Power Supply, $2.3V \leq V_{CCB} \leq 5.5V$
12	VCCA	-	A Terminal Power Supply, $1.65V \leq V_{CCA} \leq 5.5V$, $V_{CCA} \leq V_{CCB}$
-	EPAD	-	Connect to Ground or Not Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Condition	Range	Unit
VCCA Power Supply		-0.3 ~ +6.0	V
VCCB Power Supply		-0.3 ~ +6.0	V
Input Voltage Range		-0.3 ~ +6.0	V
Voltage Applied to Output in High-Impedance or Power-down State		-0.3 ~ +6.0	V
Voltage Applied to Output in Normal State	A Terminal	-0.3 ~ V _{CCA} +0.3V	V
	B Terminal	-0.3 ~ V _{CCB} +0.3V	V
Input Clamp Current	V _I <0V	-50	mA
Output Clamp Current	V _O <0V	-50	mA
Output Continuous Current		±50	mA
Continuous Current through VCCA, VCCB and GND		±100	mA
Operating Temperature		-40 ~ +125	°C
Junction Temperature		150	°C
Storage Temperature		-65 ~ +150	°C
Lead Temperature (10s)		260	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Power Supply ²	V _{CCA}			1.65		5.5	V
	V _{CCB}			2.3		5.5	
High Level Input Voltage	V _{IH}	A Terminal	V _{CCA} =1.65V ~ 1.95V V _{CCB} =2.3V ~ 5.5V	V _{CCI} -0.4		V _{CCI} ¹	V
			V _{CCA} =2.3V ~ 5.5V V _{CCB} =2.3V ~ 5.5V	V _{CCI} -0.4		V _{CCI}	
		B Terminal		V _{CCI} -0.4		V _{CCI}	
		OE Terminal		V _{CCA} ×0.8		5.5	
Low Level Input Voltage	V _{IL}	A Terminal		0		0.4	V
		B Terminal		0		0.4	
		OE Terminal		0		V _{CCA} ×0.2	
Change for Input Signal Edge	Δt/ΔV	A Terminal Push-Pull Driving				10	ns/V
		B Terminal Push-Pull Driving				10	
		Control Input				10	

Note:

1. V_{CCI} is relevant to input terminal. V_{CCO} is relevant to output terminal.
2. V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} can't exceed 5.5V.

ELECTRICAL CHARACTERISTICS

$V_{CCA}=1.65V-5.5V$, $V_{CCB}=2.3V-5.5V$, typical values at $T_A=25^{\circ}C$, unless otherwise noted.

Electrical Characteristics

Parameter	Symbol	Condition		Min	Typ	Max	Unit
A Terminal High Level Output Voltage	V_{OHA}	$I_{OH}=-20\mu A$, $V_{IB}\geq V_{CCB}-0.4V$			$V_{CCA}\times 0.8$		V
A Terminal Low Level Output Voltage	V_{OLA}	$I_{OL}=1mA$, $V_{IB}\leq 0.15V$			0.2		
B Terminal High Level Output Voltage	V_{OHB}	$I_{OH}=-20\mu A$, $V_{IA}\geq V_{CCA}-0.4V$			$V_{CCB}\times 0.8$		
B Terminal Low Level Output Voltage	V_{OLB}	$I_{OL}=1mA$, $V_{IA}\leq 0.15V$			0.2		
OE Input Current	I_I	OE			0.1		μA
Power down Leakage Current	I_{OFF}	A Terminal	$V_{CCA}=0V$, $V_{CCB}=0V\sim 5.5V$		0.1		
		B Terminal	$V_{CCA}=0V\sim 5.5V$, $V_{CCB}=0V$		0.1		
Three-state Output Leakage Current	I_{OZ}	A or B Terminal	OE=0V		0.1		
Quiescent Current	I_{CCA}	$V_I=V_O=OPEN$, $I_O=0$	$V_{CCA}=1.65V\sim V_{CCB}$, $V_{CCB}=2.3V\sim 5.5V$		0.1		μA
			$V_{CCA}=5.5V$, $V_{CCB}=0V$		0.1		
			$V_{CCA}=0V$, $V_{CCB}=5.5V$		0.1		
	I_{CCA+} I_{CCB}	$V_I=V_O=OPEN$, $I_O=0$	$V_{CCA}=1.65V\sim V_{CCB}$, $V_{CCB}=2.3V\sim 5.5V$		11.5		μA
	I_{CCB}	$V_I=V_O=OPEN$, $I_O=0$	$V_{CCA}=1.65V\sim V_{CCB}$, $V_{CCB}=2.3V\sim 5.5V$		11		μA
			$V_{CCA}=5.5V$, $V_{CCB}=0V$		0.1		
			$V_{CCA}=0V$, $V_{CCB}=5.5V$		0.1		

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Quiescent Current	I _{CCZA}	V _I =V _O =OPEN I _O =0,OE=GND	V _{CCA} =1.65V~V _{CCB} , V _{CCB} =2.3V~5.5V	0.1		μA
			V _{CCA} =5.5V, V _{CCB} =0V	0.1		
			V _{CCA} =0V, V _{CCB} =5.5V	0.1		
	I _{CCZB}	V _I =V _O =OPEN, I _O =0,OE=GND	V _{CCA} =1.65V~V _{CCB} , V _{CCB} =2.3V~5.5V	0.1		μA
			V _{CCA} =5.5V, V _{CCB} =0V	0.1		
			V _{CCA} =0V, V _{CCB} =5.5V	0.1		
OE Input Capacitance	C _I	V _{CCA} =3.3V, V _{CCB} =3.3V		5		pF
A Terminal Input Capacitance	C _{IO}	V _{CCA} =3.3V, V _{CCB} =3.3V		6.5		pF
B Terminal Input Capacitance				6.5		

Timing Requirement

		V _{CCB} =2.5V	V _{CCB} =3.3V	V _{CCB} =5V	Unit
		Typ	Typ	Typ	
T _A = +25°C, V _{CCA} = 1.8V, unless otherwise noted					
Data Rate	Push-Pull Mode	10	10	10	Mbps
	Open-Drain Mode	2	2	2	
T _A = +25°C, V _{CCA} =2.5V, unless otherwise noted					
Data Rate	Push-Pull Mode	10	10	10	Mbps
	Open-Drain Mode	2	2	2	
T _A = +25°C, V _{CCA} = 3.3V, unless otherwise noted					
Data Rate	Push-Pull Mode		10	10	Mbps
	Open-Drain Mode		2	2	
T _A = +25°C, V _{CCA} = 5V, unless otherwise noted					
Data Rate	Push-Pull Mode			9	Mbps
	Open-Drain Mode			2	

Switching Characteristics

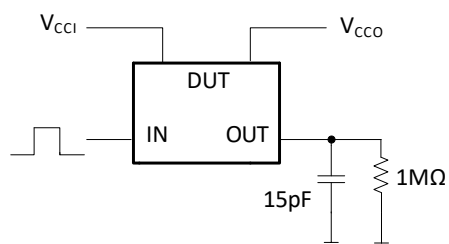
T_A = +25°C, V_{CCA} = 1.8V, unless otherwise noted.

Parameter	Symbol	Condition	V _{CCB} = 2.5V	V _{CCB} = 3.3V	V _{CCB} = 5V	Unit
			Typ	Typ	Typ	
V _{CCA} = 1.8V						
A to B Delay	t _{PHL}	Push-Pull Mode	2.4	3.0	5.4	ns
		Open-Drain Mode	26.0	26.3	26.7	
	t _{PLH}	Push-Pull Mode	4.0	3.6	3.5	
		Open-Drain Mode	175	145	110	
B to A Delay	t _{PHL}	Push-Pull Mode	2.0	2.6	3.6	ns
		Open-Drain Mode	26.0	26.1	26.2	
	t _{PLH}	Push-Pull Mode	1.7	1.5	1.4	
		Open-Drain Mode	133	69	51	
OE Enable Time (t _{PZH} and t _{PZL})	t _{EN}		5.2	4.4	3.8	ns
OE Disable Time (t _{PHZ} and t _{PLZ})	t _{DIS}		614	616	626	
A Terminal Rise Time	t _{rA}	Push-Pull Mode	4	4.5	5.5	ns
		Open-Drain Mode	89	31	10	
B Terminal Rise Time	t _{rB}	Push-Pull Mode	7	6	5.5	ns
		Open-Drain Mode	128	98	58	
A Terminal Fall Time	t _{fA}	Push-Pull Mode	5	4.5	3.5	ns
		Open-Drain Mode	1.9	1.7	1.6	
B Terminal Fall Time	t _{fB}	Push-Pull Mode	5.5	7	11	ns
		Open-Drain Mode	2.2	2.3	2.9	
Channel to Channel Skew	t _{sk(0)}		0.5	0.5	0.5	ns
Data Rate		Push-Pull Mode		10	12	Mbps
		Open-Drain Mode	2	2	2	
V _{CCA} = 2.5V						
A to B Delay	t _{PHL}	Push-Pull Mode	2.7	3.3	4.8	ns
		Open-Drain Mode	26.2	26.4	26.7	
	t _{PLH}	Push-Pull Mode	2.6	2.4	2.3	
		Open-Drain Mode	169	144	110	
B to A Delay	t _{PHL}	Push-Pull Mode	2.4	2.3	2.4	ns
		Open-Drain Mode	26.3	26.4	26.5	
	t _{PLH}	Push-Pull Mode	2.0	1.9	1.8	
		Open-Drain Mode	165	118	55	

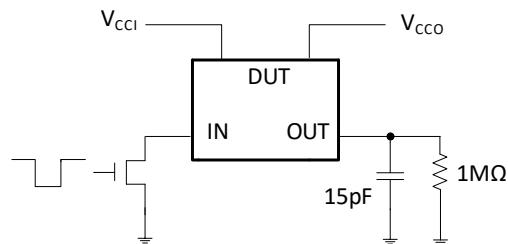
Parameter	Symbol	Condition	V _{CCB} = 2.5V	V _{CCB} = 3.3V	V _{CCB} = 5V	Unit
			Typ	Typ	Typ	
OE Enable Time (t _{PZH} and t _{PZL})	t _{EN}		14	13	12	ns
OE Disable Time (t _{PHZ} and t _{PLZ})	t _{DIS}		630	635	640	
A Terminal Rise Time	t _{rA}	Push-Pull Mode	13	13	12	ns
		Open-Drain Mode	120	70	10	
B Terminal Rise Time	t _{rB}	Push-Pull Mode	4.5	3.4	2.6	ns
		Open-Drain Mode	122	96	62	
A Terminal Fall Time	t _{fA}	Push-Pull Mode	8	7	6	ns
		Open-Drain Mode	2.0	1.9	1.7	
B Terminal Fall Time	t _{fB}	Push-Pull Mode	8	12	15	ns
		Open-Drain Mode	1.9	2.1	2.7	
Channel to Channel Skew	t _{sk(0)}		0.5	0.5	0.5	ns
V _{CCA} = 3.3V						
A to B Delay	t _{PHL}	Push-Pull Mode		3.5	4.9	ns
		Open-Drain Mode		26.3	26.7	
	t _{PLH}	Push-Pull Mode		2.2	2.0	
		Open-Drain Mode		133	104	
B to A Delay	t _{PHL}	Push-Pull Mode		3.0	3.2	ns
		Open-Drain Mode		26.6	26.8	
	t _{PLH}	Push-Pull Mode		1.8	1.7	
		Open-Drain Mode		132	83	
OE Enable Time (t _{PZH} and t _{PZL})	t _{EN}			12	11	ns
OE Disable Time (t _{PHZ} and t _{PLZ})	t _{DIS}			630	635	
A Terminal Rise Time	t _{rA}	Push-Pull Mode		12	11	ns
		Open-Drain Mode		87	36	
B Terminal Rise Time	t _{rB}	Push-Pull Mode		10	9	ns
		Open-Drain Mode		87	56	
A Terminal Fall Time	t _{fA}	Push-Pull Mode		12	11	ns
		Open-Drain Mode		2.3	2.0	
B Terminal Fall Time	t _{fB}	Push-Pull Mode		13	16	ns
		Open-Drain Mode		2.0	2.5	
Channel to Channel Skew	t _{sk(0)}			0.5	0.5	ns

Parameter	Symbol	Condition	V _{CCB} = 2.5V	V _{CCB} = 3.3V	V _{CCB} = 5V	Unit
			Typ	Typ	Typ	
V _{CCA} = 5.0V						
A to B Delay	t _{PHL}	Push-Pull Mode			5.4	ns
		Open-Drain Mode			26.7	
	t _{PLH}	Push-Pull Mode			1.9	
		Open-Drain Mode			120	
B to A Delay	t _{PHL}	Push-Pull Mode			5.6	ns
		Open-Drain Mode			27.3	
	t _{PLH}	Push-Pull Mode			1.7	
		Open-Drain Mode			126	
OE Enable Time (t _{PZH} and t _{PZL})	t _{EN}				10	ns
OE Disable Time (t _{PHZ} and t _{PLZ})	t _{DIS}				636	
A Terminal Rise Time	t _{rA}	Push-Pull Mode			8	ns
		Open-Drain Mode			79	
B Terminal Rise Time	t _{rB}	Push-Pull Mode			7	ns
		Open-Drain Mode			73	
A Terminal Fall Time	t _{fA}	Push-Pull Mode			8.7	ns
		Open-Drain Mode			2.7	
B Terminal Fall Time	t _{fB}	Push-Pull Mode			8.6	ns
		Open-Drain Mode			2.4	
Channel to Channel Skew	t _{sk(0)}				0.5	ns

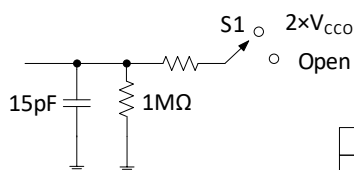
TEST CIRCUIT



Push-Pull Mode

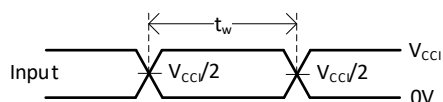


Open-Drain Mode

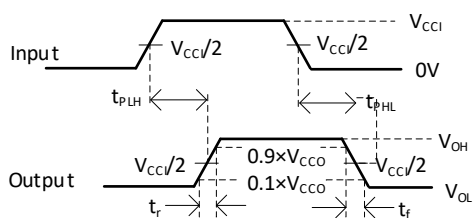


OE input enable and disable timing measurement

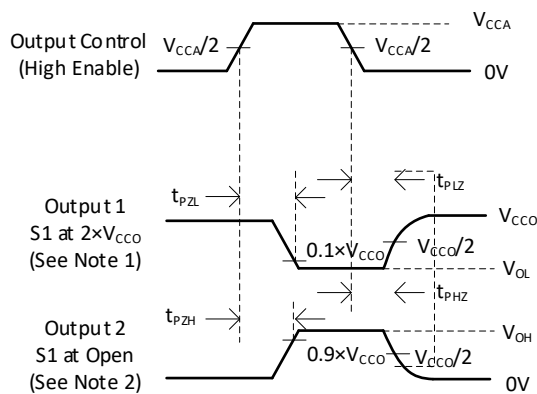
TEST	S1
t_{PZL}/t_{PLZ}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	Open



Pulse Time



Propagation Delay Time



Enable and Disable Time

Note:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is used for outputs with internal conditions to make the output low unless the output control terminal to be disabled, Waveform 2 is used for outputs with internal conditions to make the output high unless the output control terminal to be disabled.
3. All input pulses are supplied by a generator with the following characteristics: $PRR \leq 10\text{MHz}$, $Z_o = 50\Omega$, $dv/dt \geq 1\text{V/ns}$.
4. Output measurements once, each measurement needs to be converted once.
5. t_{PLZ} , t_{PHZ} and t_{DIS} are the same.
6. t_{PZL} , t_{PZH} and t_{EN} are the same.
7. t_{PLH} , t_{PHL} and t_{PD} are the same.
8. V_{CCI} is the V_{CC} associated with input terminal.
9. V_{CCO} is the V_{CC} associated with output terminal.
10. All parameters and waveforms are not applicable to all devices.

APPLICATION DESCRIPTION

The MS4554N/MS4554N1 could be applied to interface two different voltage nodes, in order to connect logic level in electronic system. The MS4554N/MS4554N1 is used in point-to-point topology to connect the device or system which mutually operate in different interface voltages. The main purpose is to connect open-drain driver and I/O terminals, such as I²C and 1-Wire. And the data is bidirectional transmission without control signal. It's also used to data connection between push-pull driver and I/O terminals.

Input Driver Requirement

The fall time (t_{fA} , t_{fB}) depends on the output impedance of external driver, which could drive the data I/O of the MS4554N/MS4554N1. In addition, t_{PHL} and data rate also are up to the output impedance of external driver. t_{fA} , t_{fB} , t_{PHL} and conversion rate are defined as the value where the output impedance of external driver is less than 50Ω.

Power up

During operation, ensure $V_{CCA} \leq V_{CCB}$. And each power sequencing couldn't destroy device. Therefore, elevating any power would be no problem.

Output Load Caution

It's recommended to apply PCB layout with short traces, in order to avoid overlarge capacitance load and ensure correct one trigger. PCB signal traces should be enough short to make sure that the reflex go-back delay is less than one trigger duration. Signal integrity can be improved by ensuring that there is low impedance at driver in any reflex. The period of one trigger approaches to 30ns. In addition, the maximum capacitance driving total lumped loads is also directly up to one trigger duration. For very large capacitive load, one trigger could be overtime before the signal is driven completely. Through balancing dynamic characteristic I_{CC} , load driving capacity and the maximum bit rate, set one trigger duration is the best condition. The PCB trace length and connector would increase the capacitance value seeing from of the MS4554N/MS4554N1 output. Therefore, recommend to use lumped load capacitor to avoid system-stage influences, such as one trigger, bus competition, output signal shock and so on.

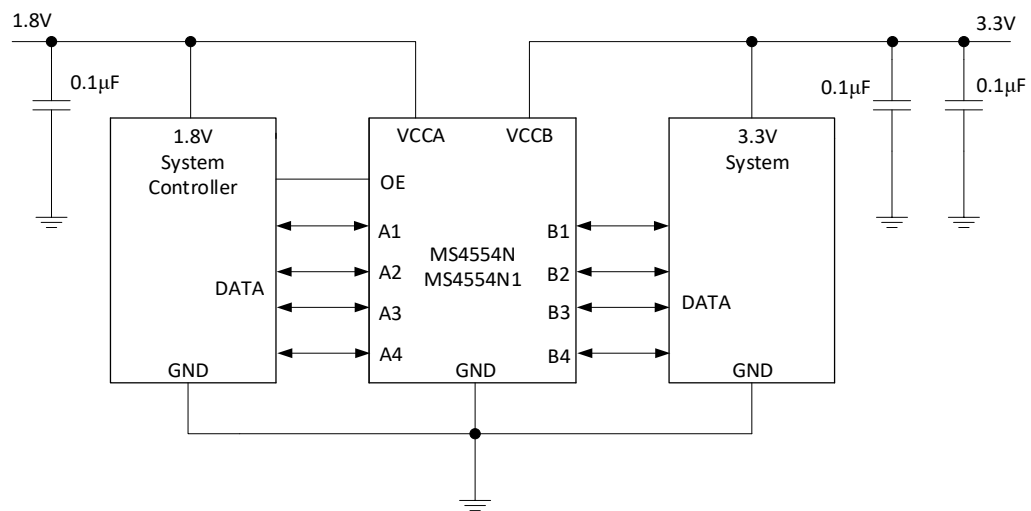
Enable and Disable

The MS4554N /MS4554N1 has one OE input terminal, which is used to disable device when OE is low level state, thus all I/Os are in high impedance state. Only VCCA is supplied, OE would have one internal pulldown current source. Disable time(t_{DIS}) represents that the delay time between OE becoming low and output in high impedance state. Enable time(t_{EN}) represents the time when user must allow that one trigger circuit just starts to operate after OE goes high.

I/O Pullup and Pulldown Resistors

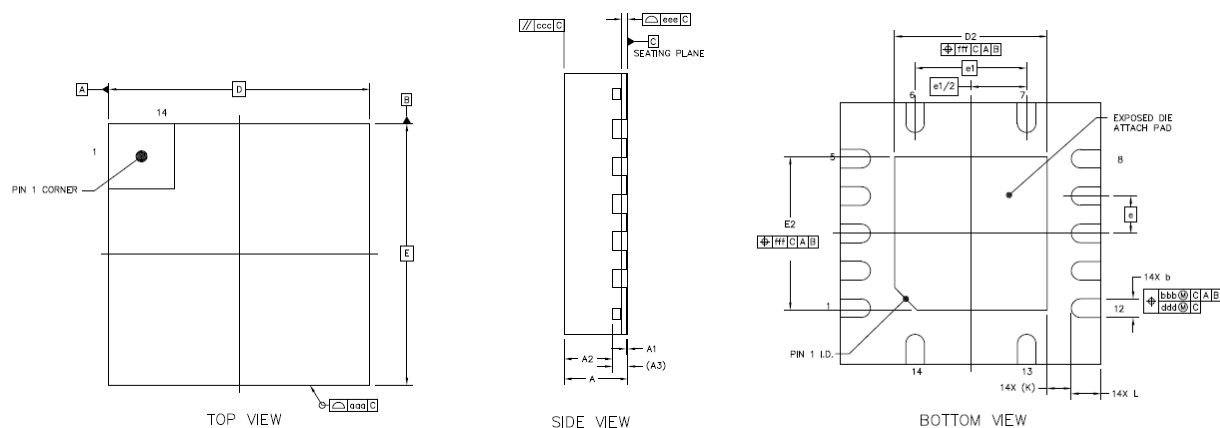
Each A terminal has an internal 10kΩ pullup resistor for VCCA. Each B terminal has an internal 10kΩ pullup resistor for VCCB. If a smaller pullup resistor is required, must connect an external resistor between I/O and VCCA/VCCB. While applying a smaller pullup resistor would affect V_{OL} . When OE goes low, internal pullup resistor would be disabled.

TYPICAL APPLICATION



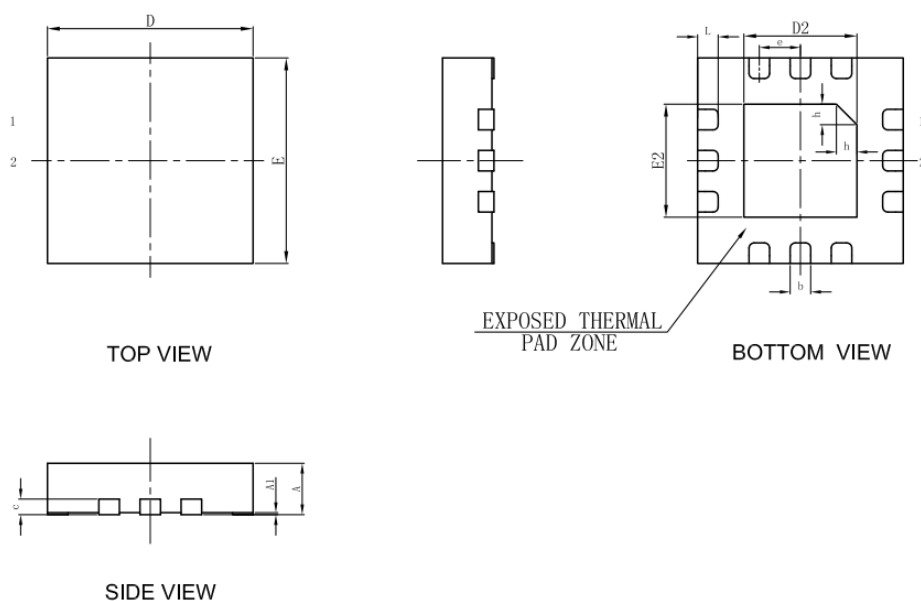
PACKAGE OUTLINE DIMENSIONS

QFN14



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	-	0.65	-
A3	0.203 REF		
b	0.2	0.25	0.3
D	3.5 BSC		
E	3.5 BSC		
e	0.5 BSC		
e1	1.5 BSC		
D2	1.95	2.05	2.15
E2	1.95	2.05	2.15
L	0.3	0.4	0.5
K	0.325 REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
ddd	0.05		
fff	0.1		

QFN12



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.45	0.50	0.55
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	1.90	2.00	2.10
D2	1.00	1.10	1.20
e	0.40 BSC		
E	1.90	2.00	2.10
E2	1.00	1.10	1.20
L	0.15	0.20	0.25
h	0.15	0.20	0.25

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS4554N, MS4554

Product Code: XXXXXXX, XXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS4554N	QFN14	4000	1	4000	8	32000
MS4554N1	QFN12	3000	10	30000	4	120000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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