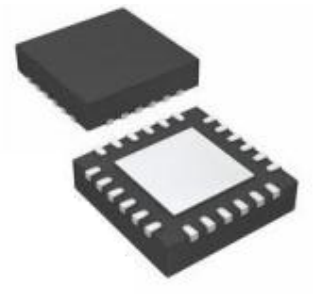
Three-Phase Brushless Motor Driver

PRORODUCT DESCRIPTION

The MS39361N is a three-phase brushless motor driver chip. Its power supply ranges from 3V to 10V, which is suitable for one or two lithium battery applications. And its maximum continuous output drive current is 2A.

The chip adopts the PWM pulse drive way to reduce output power dissipation and adjusts the motor speed by changing the duty ratio of the external signal. The chip has a built-in lock protection circuit, which can protect the chip when the motor operates normally but the Hall input signal is abnormal.



QFN24

FEATURES

- Continuous Output Current: 2A
- Power Supply: 3V ~ 10V
- Low Output Resistance on Upper-side Bridge: 0.16Ω, Lower-side Bridge: 0.16Ω
- Using Direct PWM Input for Speed Control and Synchronous Rectification
- 1-Hall and 3-Hall FG Output
- CSD Lock Protection Circuit
- Switch Forward/Reverse Operation Mode
- Power Saving in Stop Mode
- Overheat Protection, Overcurrent Protection, Current Limit Protection
- Low-voltage Protection, 3V or 5V Optional
- 3.4V LDO Regulated Output Supplies Power to Hall

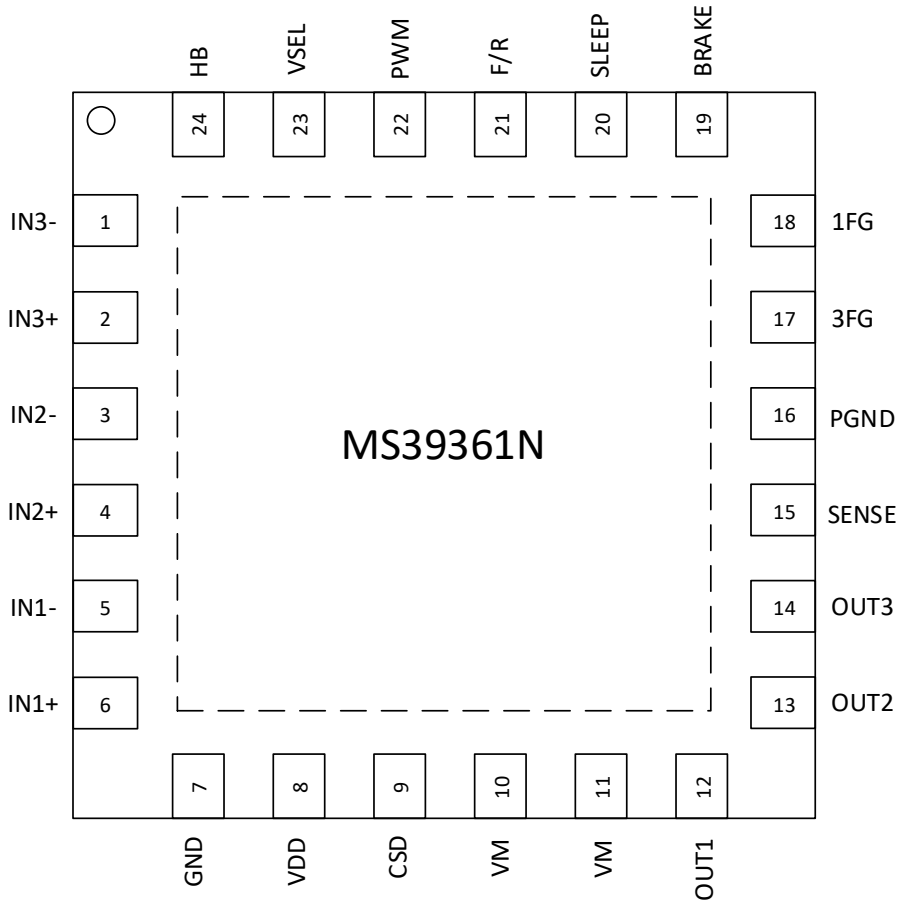
APPLICATIONS

- Small Appliance
- Hair Dividers
- Shaver
- Electric Fan

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS39361N	QFN24	MS39361N

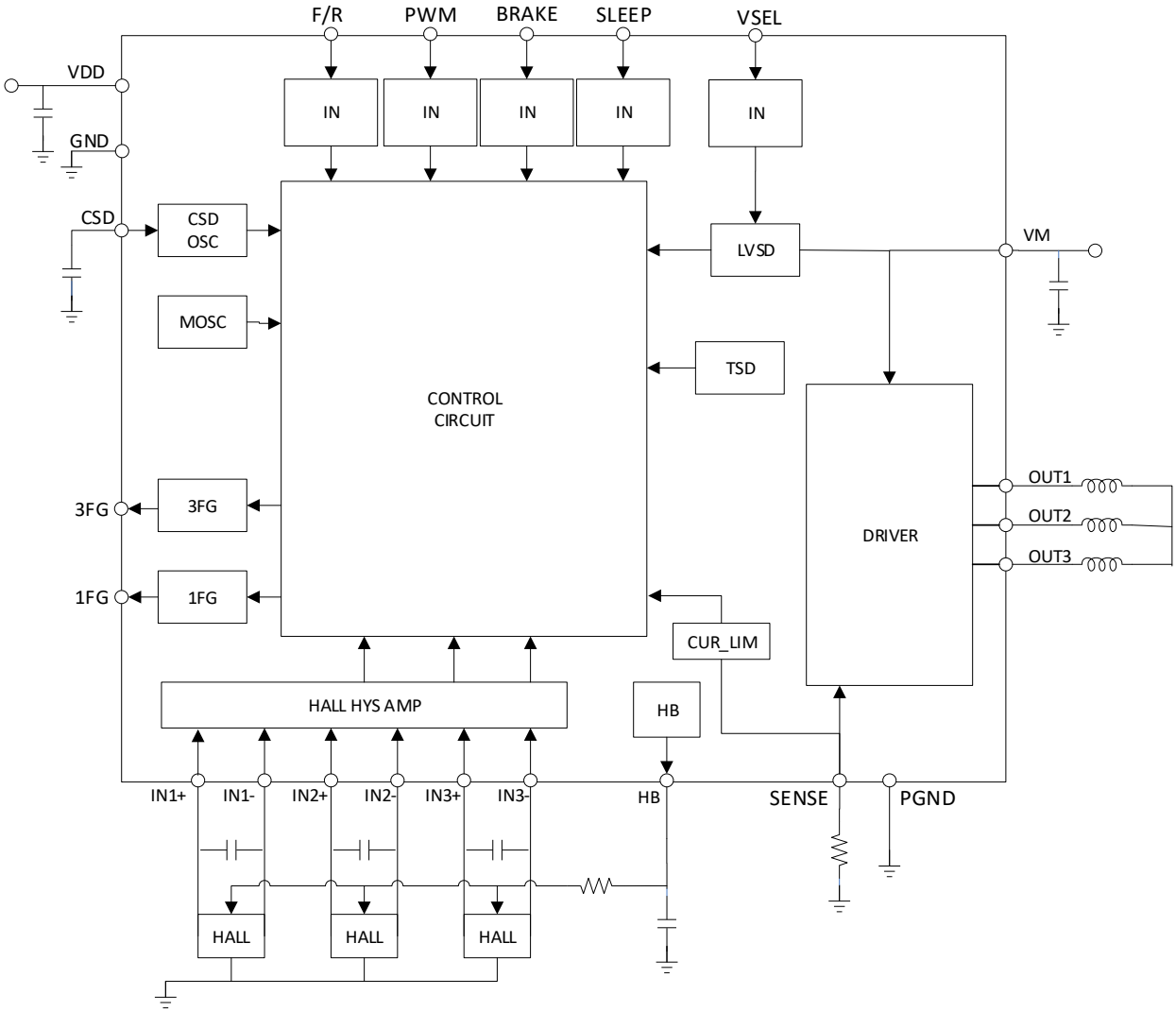
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	IN3-	I	Hall Signal Input H: IN+>IN-; L: IN->IN+
2	IN3+		
3	IN2-		
4	IN2+		
5	IN1-		
6	IN1+		
7	GND	-	Logic Ground
8	VDD	-	Logic Power Supply Input
9	CSD	I	CSD Lock Protection Capacitor
10, 11	VM	-	Power Ground, Internal Shorting
12	OUT1	O	Output 1
13	OUT2	O	Output 2
14	OUT3	O	Output 3
15	SENSE	-	Output Current Detection Resistor
16	PGND	-	Power Ground
17	3FG	O	3-Hall Signal Output
18	1FG	O	1-Hall Signal Output
19	BRAKE	I	Brake Input (Brake in High Level)
20	SLEEP	I	Sleep Input (Sleep in Low Level)
21	F/R	I	Motor Direction Input
22	PWM	I	PWM Input (Effective in Low Level)
23	VSEL	I	Voltage Setting Pin for Low-voltage Protection, 3V or 5V can be set.
24	HB	I	3.4V Regulated Output, Supply Power to Hall

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Condition	Ratings	Unit
Maximum Power Supply	VDD_{Max}		6	V
	VM_{Max}		12	V
Output Current	I_{Max}	Long-firing Operation	2	A
Maximum Power Dissipation	Pd_{Max}	Connect the Circuit Board	1.35	W
Junction Temperature	T_J		150	°C
Operating Temperature	T_A		-40 ~ 125	°C
Storage Temperature	T_{STG}		-65 ~ 150	°C
ESD (HBM)	V_{ESD}		>4	kV

ELECTRICAL CHARACTERISTICS

Pin Parameters

Unless otherwise noted, T_A=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply	V_M		3.0		10	V
VDD Pin Voltage	V_{VDD}		2.9		6	V
HB Pin Current	I_{HB}				10	mA
FG Pin Applied Voltage	V_{FG}		0		6	V
FG Pin Current	I_{FG}				10	mA

Electrical Characteristics

Unless otherwise noted, T_A=25°C, V_M=9V, V_{DD}=3.3V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Current 1	$ICC1_{VM}$	Duty Ratio: 50%, No Load, HB without Load		1.1		mA
	$ICC1_{VDD}$			2.5		mA
Power-down Current 2	$ICC2_{VM}$	PWM keeps high in a long term.		0.44		mA
	$ICC2_{VDD}$			2.4		mA
Sleep Current 3	$ICC3_{VM}$	SLEEP=0 or Hanging			1	μA
	$ICC3_{VDD}$	SLEEP=0 or Hanging			1	μA
Output Block						
Lower-side Transistor on-resistance	$R_{ON(L1)}$	I_O=1A		0.16		Ω
Upper-side Transistor on-resistance	$R_{ON(H1)}$	I_O=-1A		0.16		Ω
Lower-side Leakage Current	$I_{L(L)}$				50	μA
Upper-side Leakage Current	$I_{L(H)}$		-50			μA
Lower-side Bridge Diode Forward Bias Voltage	$V_{D(L1)}$	I_D=-2A		1		V
Upper-side Bridge Diode Forward Bias Voltage	$V_{D(H1)}$	I_D=2A		1		V
Hall Amplifier						
Input Current	$I_{B(HA)}$		-130			nA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Common-mode Voltage 1	VI_{CM1}	Use Elements	0.3		V_{DD}-1.3	V
Common-mode Voltage 2	VI_{CM2}	At One-side Input Bias (Hall IC Application)	0		V_{DD}	V
Hall Input Sensitivity	V_{HIN}	Sine Wave	50			mV_{P-P}
Hysteresis Width	$\Delta V_{IN(HA)}$			15		mV
CSD Oscillator						
High Voltage on CSD Pin	$V_{OH(CSD)}$			V_{DD}×2/3		V
Low Voltage on CSD Pin	$V_{OL(CSD)}$			V_{DD}×1/3		V
Amplitude	$V_{(CSD)}$			V_{DD}×1/3		V_{P-P}
Charge Current of External Capacitor	I_{CHG1}	V_{CHG1}=2V		-5.7		µA
Discharge Current of External Capacitor	I_{CHG2}	V_{CHG2}=2V		7		µA
Internal Oscillator Frequency	$f_{(CSD)}$	C=0.022µF		123		Hz
Internal PWM Frequency						
Oscillation Frequency	$f_{(PWM)}$			43		kHz
Current Limit Protection						
Limit Voltage	V_{SENSE}			0.2		V
Overcurrent Protection						
Output Transistor Overcurrent Protection	I_{OCPUP}	OUT is shorted to GND	3			A
	I_{OCPDW}	VM is shorted to OUT	3.2			A
Trigger Time of Overcurrent Protection	t_{LITCH}	Duration of Triggering Overcurrent Protection		3		µs
Restart Time of Overcurrent Protection	t_{RETRY}	Self Restart Time after Overcurrent Shutdown		11.5		ms

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Overheat Protection						
Shutdown Temperature	T_{SD}	Junction Temperature	140	147	160	°C
Hysteresis	ΔT_{SD}	Junction Temperature		40		°C
HB Pin						
Voltage	V_{HB}	I_{HB}=100μA, V_M=9V		3.4		V
Low Voltage Detection (VDD)						
Activation Voltage	V_{SD0}	V_{DD} Rising		2.5		V
Hysteresis Width	ΔV_{SD}			100		mV
Low Voltage Detection (VM)						
Activation Voltage	V_{SD1}	V_M Rising, VSEL=0		2.7		V
	V_{SD2}	V_M Rising, VSEL=1		5.5		V
Hysteresis Width	ΔV_{SD1}	Rising Minus Falling		150		mV
	ΔV_{SD2}	Rising Minus Falling		700		mV
3FG, 1FG Pins						
On-resistance	$R_{ON(FG)}$	I_{FG}=5mA		7		Ω
Leakage Current	$I_{L(FG)}$	V_O=5V			1	μA
SLEEP, PWM, BRAKE, VSEL, F/R Logic Input Pins						
High-level Input Voltage	V_{IH}		1.8		V_{DD}	V
Low-level Input Voltage	V_{IL}		0		1.1	V
Pull-down Resistance	R_{IN}			268		kΩ
Hysteresis Width	V_{IS}			400		mV

Three-phase Motor Logic Truth Table

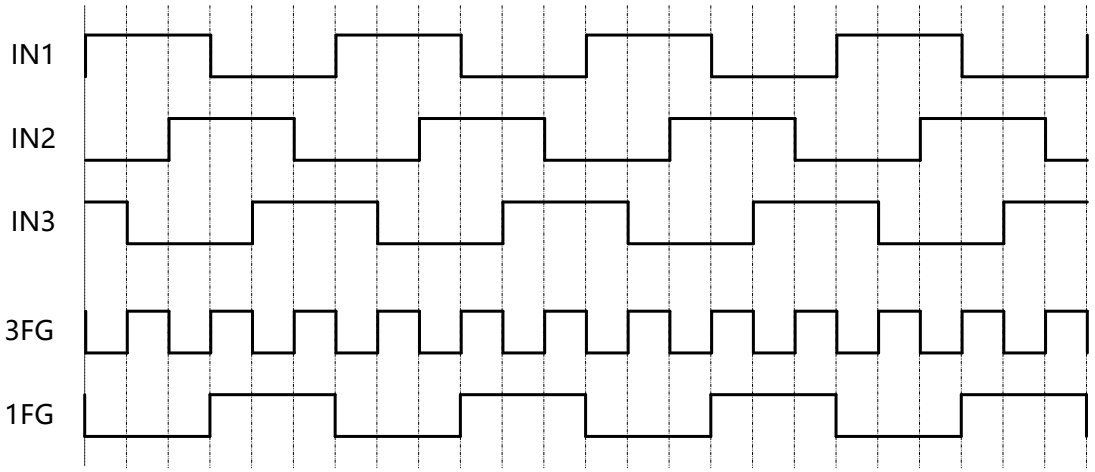
(IN="High" indicates $IN^+ > IN^-$), (outputs from 1 to 3,"H"=SOURCE,"L"=SINK, M=OFF)

F/R=H			F/R=L			OUTPUT		
IN1	IN2	IN3	IN1	IN2	IN3	OUT1	OUT2	OUT3
H	L	H	L	H	L	L	H	M
H	L	L	L	H	H	L	M	H
H	H	L	L	L	H	M	L	H
L	H	L	H	L	H	H	L	M
L	H	H	H	L	L	H	M	L
L	L	H	H	H	L	M	H	L

3FG, 1FG Output Logic

The input hall signal is not processed by the chip internally, and can be output directly according to logic. If the waveform width of 3FG is inconsistent, please detect hall position and uniformity of magnetization. The output logic table and timing diagram of 3FG and 1FG is as follows:

IN1	IN2	IN3	3FG	1FG
H	L	H	L	L
H	L	L	H	L
H	H	L	L	L
L	H	L	H	H
L	H	H	L	H
L	L	H	H	H



SLEEP, BRAKE, PWM, F/R Logic Table

Control Pins / Logic Input State	BRAKE	PWM	F/R	SLEEP
High	Brake	OFF	Reverse	Normal Operation
Low (Default State)	ON	ON	Forward	Sleep Mode

FUNCTION DESCRIPTION

Drive Module

The chip adopts the PWM drive way to reduce power dissipation and achieves regulation by adjusting ON and OFF of the upper-side transistor output module. And the drive force of the motor is determined by its duty ratio.

When PWM is normally shutdown, synchronous rectification performs. Compared with LDMOS parasitic diode freewheeling, the upper-side transistor on-freewheeling largely reduces heat generation.

Current Limit Protection

The current limit protection circuit is used to limit the peak value of output current, which is determined by V_{RF}/R_f (V_{RF}=0.21(Typical), R_f is the current detection resistor). This circuit limits the output current by reducing the output on duty ratio.

Overcurrent protection circuit detects when PWM is operating, there is a 700ns delay for the reverse current that flows through the diode, which prevents the current limit circuit from operating abnormally. If the coil resistance of the motor is small, or the inductance is low, when starting up, the current (there is no back electromotive force generated in the motor) will change rapidly. As a result, the operation delay may cause the current limit operation to take place when the value is above the set current. Therefore, it is necessary to consider the increase in current due to the delay when setting the current limit value.

Be aware that the PWM frequency in the current limit circuit is determined by the internal oscillator, and is approximately 43kHz.

Overcurrent Protection

Overcurrent protection circuit monitors the current flowing through drive transistors. When these abnormal conditions occur: output is shorted to power supply, output is shorted to GND and short between outputs, if the chip monitors that the current exceeds overcurrent protection threshold and time exceeds 3μs, controller would turn off output transistors. The duration is 11ms. And after 11ms, transistors are enabled again.

Speed Control Method

Pulse inputs from PWM pin and the motor speed can be controlled by adjusting the PWM duty ratio.

When PWM=0, it can be set to ON; when PWM=1, it can be set to OFF.

If it is necessary to use inverted logic, an additional NPN transistor can be added. When the PWM pin remains high-level for a long time, the duty ratio judged by the chip is 0, thus causing the CSD circuit count to be reset and the output on HB pin is 0.

CSD Protection Circuit

The MS39361N includes a lock protection circuit. This circuit operates when the motor operates normally but the Hall signal remains unchanged for a certain period. When CSD circuit is operating, all upper-side transistor will be OFF.

Time is determined by the capacitor on CSD pin. Setting time=90×C(μF)。

When a 0.022μF capacitor is connected, the protection time is about 2s. The setting time must be large enough to meet the startup time of the motor.

The conditions for resetting count are as follows:

- When the SLEEP pin is low-level → Protection released and count reset (Initial state reset)
- When the BRAKE pin is high-level → Protection released and count reset (Initial state reset)
- When the F/R pin is switched → Protection released and count reset
- When 0% duty ratio is detected on the PWM pin → Protection released and count reset
- When low-voltage condition is detected → Protection released and count reset (Initial state reset)
- When TSD condition is detected → Stop counting

When CSD pin is connected to the ground, the logic circuit will go into an initial state to prevent speed control. When CSD protection is not used, connect a resistor of approximately 220kΩ and a capacitor of about 4700pF in parallel to the ground.

Low Voltage Protection

The MS39361N incorporates a comparator that uses the band gap voltage as the reference. The circuit detects VM voltage. When the SLEEP pin is high and the VDD voltage falls below VSD, all output transistors would be set to OFF.

The chip provides select pin VSEL. When VSEL=0, VSD is about 2.7V; When VSEL=1, VSD is about 4.8V. And they correspond to one and two lithium batteries applications respectively.

Overheat Protection

When the chip junction temperature exceeds 147°C, the overheat protection circuit is activated and all the output transistors are set to OFF. When temperature recovers to 107°C (147°C - hysteresis temperature 40°C), all output transistors recover operations.

But because the overheat protection circuit is only activated when the chip junction temperature exceeds the setting value, there is no guarantee that the chip is free from damage.

Hall Input Signal

The Hall input signal can be recognized with the amplitude exceeding the hysteresis (35mV maximum). But when considering the noise effect and phase drift, the amplitude should be at least more than 100mV.

In order to reduce the output noise interference, it is necessary to connect a capacitor to the ground on Hall input pins. In the CSD protection circuit, the Hall input is used as a judgment signal. Even if the circuit can ignore much noise, paying attention to it is necessary. If all Hall input signal is HHH or LLL at the same time, it is regarded as the fault state and all output transistors are set to OFF.

If Hall chip is used, one side of the inputs (regardless of positive or negative) is fixed within the common-mode voltage range (0.3V ~ VDD-1.3V) and allows the other voltage range between 0V and VDD.

Method for connecting Hall elements:

(1) Connection in series

Advantages:

- Because the current is shared by Hall elements in series, the current consumption is less than that of parallel connection.
- Current limit resistor can be abandoned.
- Amplitude changing with temperature is small.

Disadvantages:

- Because each Hall element only can be divided to 1V, there is possible that amplitude cannot be satisfied.
- The current flowing through the Hall element changes with temperature.
- Asymmetry of Hall element (different input resistance) is easy to influence the amplitude.

(2) Connection in parallel

Advantages:

- The current flowing through the Hall element can be determined by the current limit resistor.
- The voltage on Hall element can be various, and can satisfy enough amplitude.

Disadvantages:

- Because it needs to provide current for each Hall element separately, the current consumption is larger.
- Need a current limit resistor.
- Amplitude changes with temperature.

HB Pin

HB pin can be used for turning off the Hall element current in power saving mode.

The HB pin would be turned off as follows.

- When the SLEEP pin becomes low, entering the power saving mode.
- PWM input detects 0% duty ratio.

Power Saving Mode

The MS39361N provides two-stage power saving modes. The triggering method of the first-stage power saving mode is that when PWM input is high-level exceeding a certain period, the chip would turn off the power supplies for HB, drive and some circuits. The triggering method of the second-stage power saving mode is to make SLEEP input in low-level. All circuits are turned off and current is less than 1μA at this time.

VM Stability

The MS39361N generates large output current and uses a switching drive method, so the power supply line must be easy to be disturbed. For ensuring the stable voltage, it is necessary to connect a large capacitor between the VM pin and ground. The ground of the capacitor is connected to the PGND pin (power ground), which is placed as close as possible to the pin. If it is impossible to connect a large capacitor on the VM pin, a 0.1μF ceramic capacitor is connected near the pin.

If a diode is inserted on the power supply line to prevent reverse connection, the power supply line is easier to be disturbed, which needs larger capacitors.

VDD

VDD supplies for input interface, logic control and analog part. It is necessary to connect a stable capacitor between VDD and GND. The operating voltage of VDD ranges from 2.9V to 6V. When one lithium battery supplies for VM, it also can supply for VDD directly. When two lithium batteries are used, VDD is supplied by external MCU or LDO.

Charge Pump

The MS39361N has an internal charge-pump and there is no need for additional pins and capacitors.

Using Notes

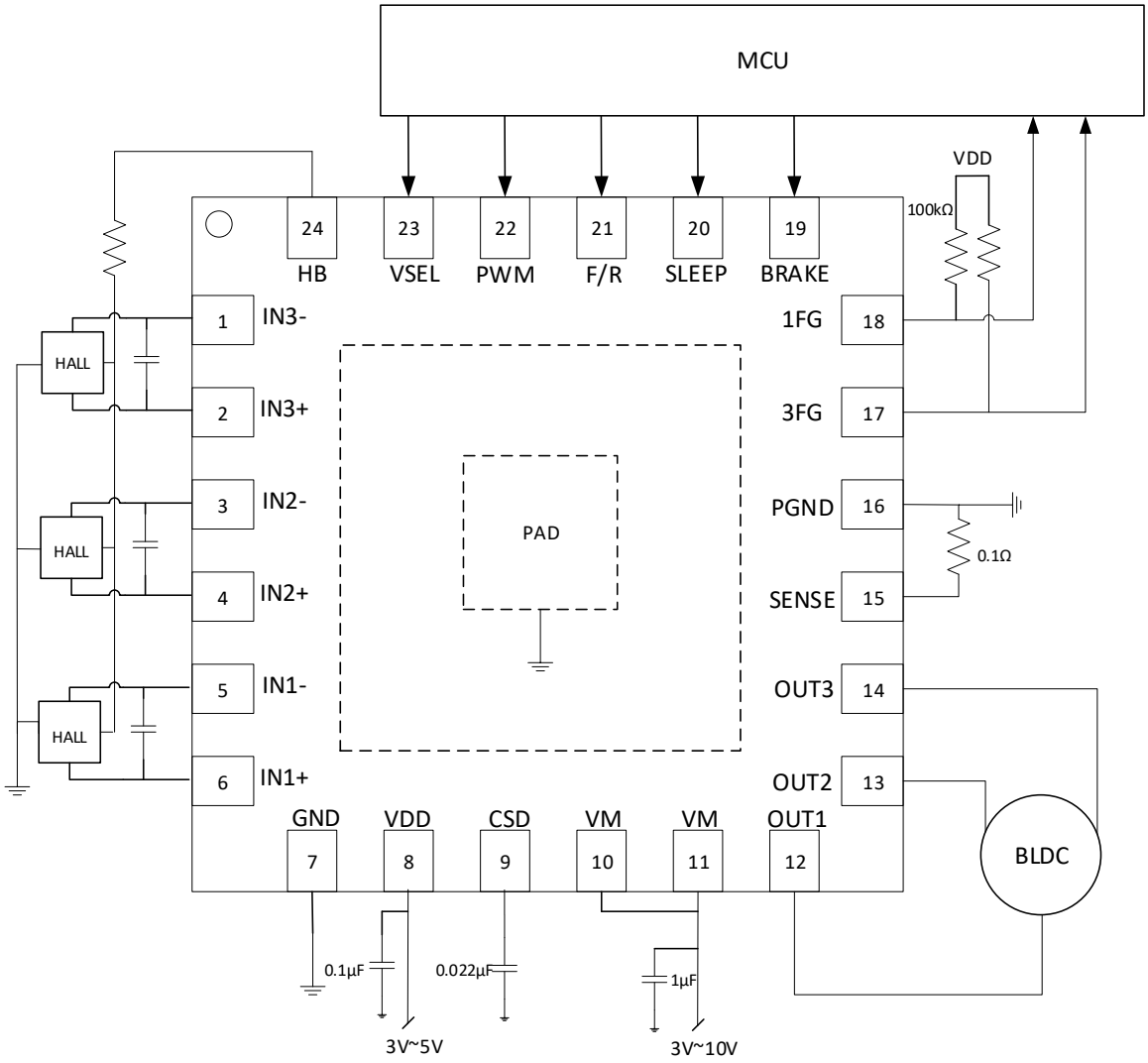
The MS39361N has synchronous rectification function, which can improve drive efficiency. When synchronous rectification performs, compared with LDMOS parasitic diode freewheeling, the upper-side transistor on-freewheeling largely reduces heat generation. However, synchronous rectification may cause the power supply to rise, such as the following conditions:

- Output duty ratio reduces suddenly.
- PWM input frequency reduces suddenly.

To ensure the maximum ratings are not exceeded even when the power supply voltage is increasing, effective measures must be adopted as follows:

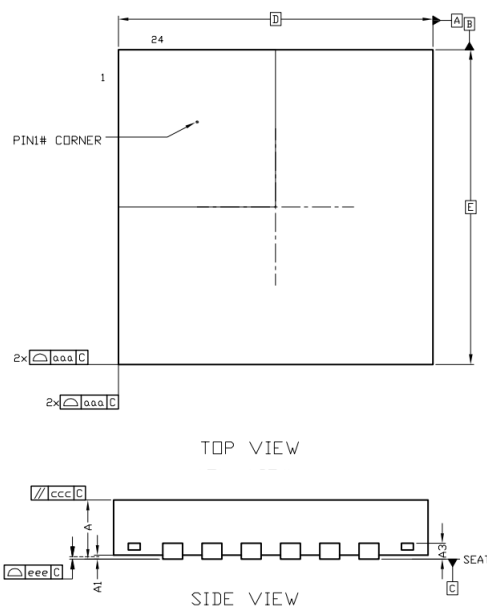
- Selection for the large capacitor between power supply and ground.
- Connection for the diode between power supply and ground.

TYPICAL APPLICATION



PACKAGE OUTLINE DIMENSIONS

QFN24



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	-	0.20REF	-
b	0.18	0.25	0.30
D		4.00BSC	
E		4.00BSC	
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.50BSC	
L	0.35	0.40	0.45
K	0.20	-	-
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description

Product Name: MS39361N

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS39361N	QFN24	4000	1	4000	8	32000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1、The operator shall ground through the anti-static wristband.

2、The equipment shell must be grounded.

3、The tools used in the assembly process must be grounded.

4、Must use conductor packaging or anti-static materials packaging or transportation.

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