# 2.7V to 5.5V, 12Bit, Eight-Channel Rail-to-Rail Output DAC

## FEATURES

- Ensure Monotonicity
- Low Power Dissipation
- Rail-to-Rail Output
- Daisy Chain Mode
- Power-up Rest to 0
- Operating Temperature: -40°C to 125°C
- INL: ±2LSB (Typ.)
- DNL: -0.4LSB to 0.75LSB
- Setup Time: 8.5μs (Max.)
- Zero Scale Error: 15mV (Max.)
- Full Scale Gain Error: -0.75%FSR (Max.)
- Power Supply: 2.7V~5.5V

## APPLICATIONS

- Portable Device
- Industrial Process Control
- Medical and Mobile Control Device
- Programmable Voltage Source and Current Source

## PRODUCT DESCRIPTION

The MS5208T/MS5208N is a 12bit, eight-channel output voltage DAC. It integrates power-up reset circuit and rail-to-rail output buffer. The interface adopts three-wire serial port mode, whose operating frequency can reach 40MHz and can be compatible with SPI, QSPI, DSP and Microwire serial ports. The output is connected to a rail-to-rail output amplifier. The MS5208T/MS5208N has power-down mode, which can provide daisy chain operating mode. The MS5208T/MS5208N integrates two external reference terminals. One reference is used for channel A to channel D, and another reference is used for channel E to channel H.

The MS5208T/MS5208N operating voltage ranges from 2.7V to 5.5V. The MS5208 is available in TSSOP16 and QFN16 packages.

## PRODUCT SPECIFICATION

| Part Number | Package | Marking |
|---|---|---|
| MS5208T | TSSOP16 | MS5208T |
| *MS5208N | QFN16 | MS5208N |

*The package is not available temporarily. If necessary, please contact Hangzhou Ruimeng Sales Department Center.

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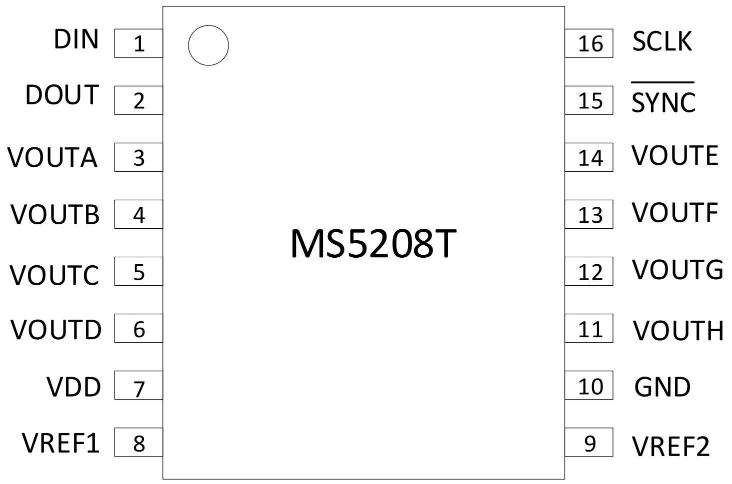
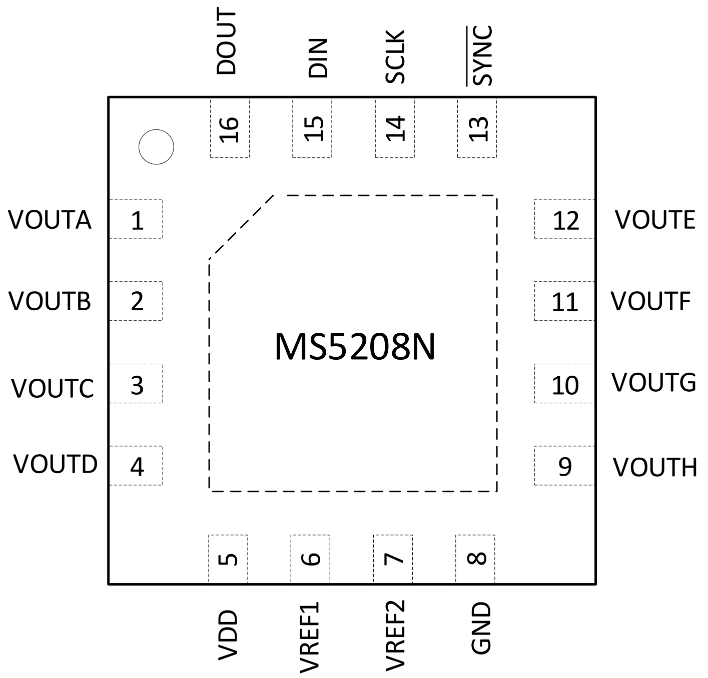
## PIN CONFIGURATION



## PIN DESCRIPTION

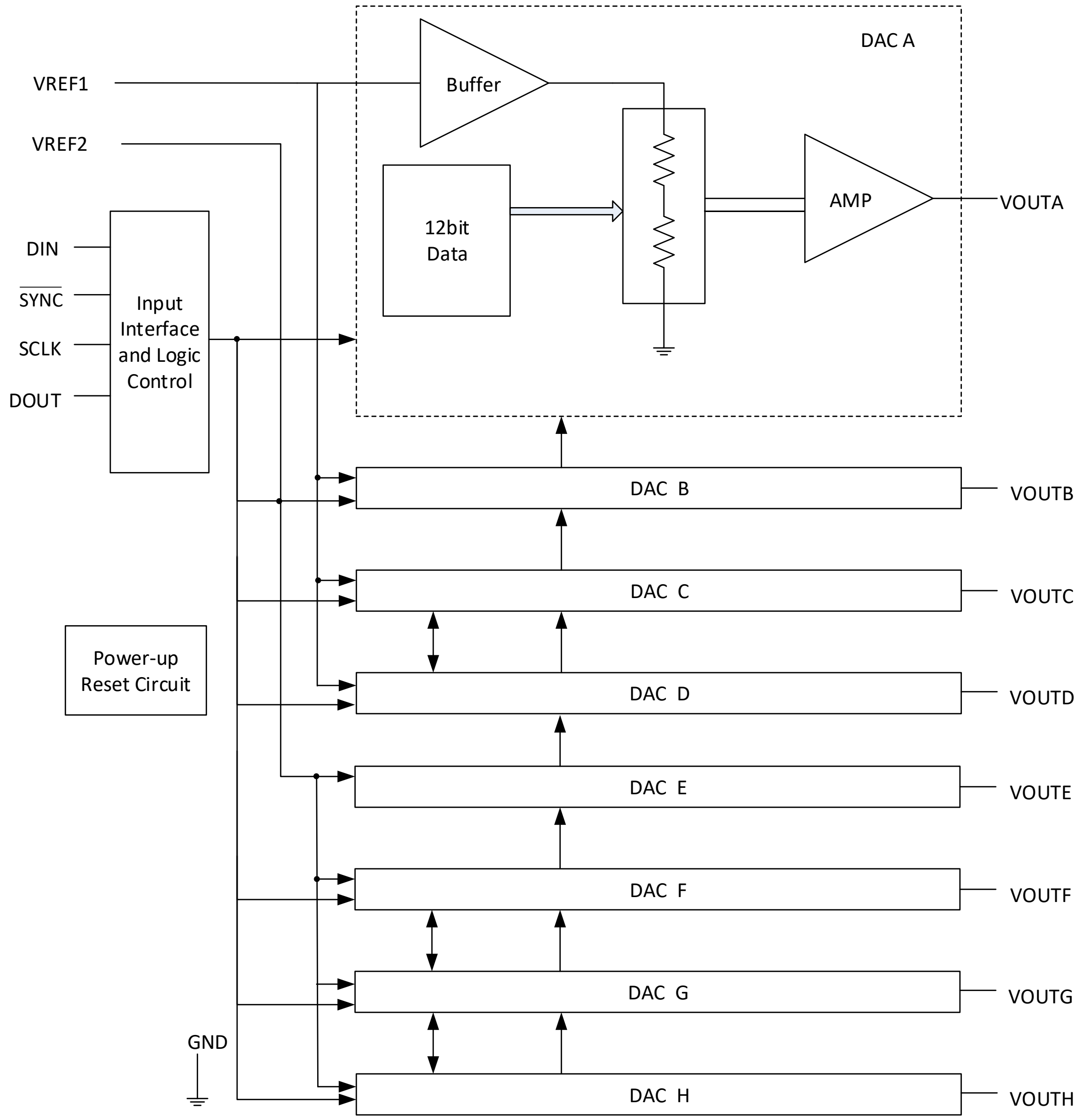
**MS5208T**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | DIN | I | Data Input for SPI Interface. When $\overline{\text{SYNC}}$ is pulled low, data is latched to 16bit conversion register on the falling edge of SCLK. |
| 2 | DOUT | O | Data Output for SPI Interface. In daisy chain, it can be connected to DIN terminal of the another MS5208T. |
| 3 | VOUTA | O | Analog Output for Channel A |
| 4 | VOUTB | O | Analog Output for Channel B |
| 5 | VOUTC | O | Analog Output for Channel C |
| 6 | VOUTD | O | Analog Output for Channel D |
| 7 | VDD | - | Power Supply |
| 8 | VREF1 | I | External Reference Input 1 |
| 9 | VREF2 | I | External Reference Input 2 |
| 10 | GND | - | Ground |
| 11 | VOUTH | O | Analog Output for Channel H |
| 12 | VOUTG | O | Analog Output for Channel G |
| 13 | VOUTF | O | Analog Output for Channel F |
| 14 | VOUTE | O | Analog Output for Channel E |
| 15 | $\overline{\text{SYNC}}$ | I | Frame Synchronous Pin for SPI Interface. When $\overline{\text{SYNC}}$ is low-level, the data input from DIN pin is latched to register on the falling edge of SCLK; DAC data is updated if $\overline{\text{SYNC}}$ is pulled high after the 16th falling edge. If $\overline{\text{SYNC}}$ is pulled high before the 16th clock, the rising edge of $\overline{\text{SYNC}}$ is used as interrupt and data is invalid. |
| 16 | SCLK | I | Clock Input for SPI Interface. The data input from DIN pin would be latched to input conversion register on the falling edge of SCLK. |

**MS5208N**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | VOUTA | O | Analog Output for Channel A |
| 2 | VOUTB | O | Analog Output for Channel B |
| 3 | VOUTC | O | Analog Output for Channel C |
| 4 | VOUTD | O | Analog Output for Channel D |
| 5 | VDD | - | Power Supply |
| 6 | VREF1 | I | External Reference Input 1 |
| 7 | VREF2 | I | External Reference Input 2 |
| 8 | GND | - | Ground |
| 9 | VOUTH | O | Analog Output for Channel H |
| 10 | VOUTG | O | Analog Output for Channel G |
| 11 | VOUTF | O | Analog Output for Channel F |
| 12 | VOUTE | O | Analog Output for Channel E |
| 13 | $\overline{\text{SYNC}}$ | I | Frame Synchronous Pin for SPI Interface. When $\overline{\text{SYNC}}$ is low-level, the data input from DIN pin is latched to register on the falling edge of SCLK; DAC data is updated if $\overline{\text{SYNC}}$ is pulled high after the 16th falling edge. If $\overline{\text{SYNC}}$ is pulled high before the 16th clock, the rising edge of $\overline{\text{SYNC}}$ is used as interrupt and data is invalid. |
| 14 | SCLK | I | Clock Input for SPI Interface. The data input from DIN pin would be latched to input conversion register on the falling edge of SCLK. |
| 15 | DIN | I | Data Input for SPI Interface. When $\overline{\text{SYNC}}$ is pulled low, data is latched to 16bit conversion register on the falling edge of SCLK. |
| 16 | DOUT | O | Data Output for SPI Interface. In daisy chain, it can be connected to DIN terminal of the another MS5208N. |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Power Supply | $V_{DD}$ | -0.3 ~ +7 | V |
| Digital Input Voltage | $V_{IN}$ | -0.3 ~ $V_{DD}$+0.3 | V |
| Reference Input Voltage | $V_{REF1}$, $V_{REF2}$ | -0.3 ~ $V_{DD}$+0.3 | V |
| Operating Temperature | $T_A$ | -40 ~ +125 | °C |
| Storage Temperature | $T_{STG}$ | -65 ~ +150 | °C |
| Maximum Junction Temperature | $T_{JMAX}$ | 150 | °C |
| Soldering Temperature (10s) | $T_{SOLDER}$ | 260 | °C |
| ESD (HBM) | $V_{ESD}$ | ±3000 | V |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply | | 2.7 | | 5.5 | V |
| Reference Input Voltage | | 0.5 | | $V_{DD}$ | V |
| Digital Input High-level Voltage ($V_{IH}$) | $V_{DD}$ =3V | 0.7×$V_{DD}$ | | | V |
| | $V_{DD}$ = 5V | 0.7×$V_{DD}$ | | | |
| Digital Input Low-level Voltage ($V_{IL}$) | $V_{DD}$ = 3V | | | 0.3×$V_{DD}$ | V |
| | $V_{DD}$ = 5V | | | 0.3×$V_{DD}$ | |
| SCLK Rate | | | | 40 | MHz |

## ELECTRICAL CHARACTERISTICS

**Static DAC**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Resolution | | | 12 | | Bits |
| Differential Non-linearity (DNL) | See Note 1 | | ±0.5 | ±2 | LSB |
| Integral Non-linearity (INL) | See Note 2 | | ±2 | ±8 | LSB |
| Zero Scale Offset | See Note 3 | | 5 | 15 | mV |
| Zero Scale Offset Temperature Drift | See Note 4 | | 20 | | ppm/°C |
| Gain Error | See Note 5 | | -0.1 | -0.75 | %FSR |
| Gain Error Temperature Drift | See Note 6 | | 12 | | ppm/°C |

Note:

1. Differential non-linearity (DNL), differential error, refers to the maximum amplitude change adjacent to LSB.
2. Integral non-linearity (INL) refers to linearity error, which condition is input digital code from 1/128×FSR to 127/128×FSR.
3. Zero scale offset refers to the analog output of zero digital input.
4. Zero scale temperature drift refers to temperature change of the analog output when digital input is zero.
5. Gain error refers to the deviation between analog output and ideal output after zero scale offset is removed.
6. Gain error temperature drift refers to the variation of the deviation between analog output and ideal output with temperature after zero scale offset is removed.

**DAC Output**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage | $R_L$=10kΩ | 0 | | $V_{REF1}/V_{REF2}$ | V |
| DC Output Impedance | | | 8 | | Ω |
| Short-circuit Current | $V_{DD}$=5V | | 32 | | mA |
| Power-up Time | Exit from Power-down mode, $V_{DD}$=5V | | 4 | | µs |

**Reference Input Voltage**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage | See Note 7 | 0 | | $V_{DD}$ | V |
| Input Resistance | | | 14.4 | | kΩ |

Note 7: The reference input voltage greater than $V_{DD}/2$ will cause output saturation distortion.

**Digital Input**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Digital Input High-level Current | $V_I=V_{DD}$ | | | ±3 | μA |
| Digital Input Low-level Current | $V_I$=0V | | | ±3 | μA |
| Input Capacitance | | | 3 | | pF |

**Power Dissipation**

| Parameter | Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply Current | $f_{SCLK}$=30MHz, No Load | $V_A$=2.7V~3.6V | | 2300 | | μA |
| | | $V_A$=4.5V~5.5V | | 2400 | | |
| | 3V, No Load, All input 0V or VDD, all channels enabled | $V_A$=2.7V~3.6V | | | | μA |
| | | $V_A$=4.5V~5.5V | | | | |
| Power-down Current | $V_{DD}$=5V | | | 66 | | μA |
| | $V_{DD}$=3V | | | 0.15 | | |

**Analog Output Dynamic**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SR | $C_L$=100pF, $R_L$=10kΩ, $V_O$=10% to 90%, $V_{REF}$=2.048, 1.024 | | 1.4 | | V/μs |
| Ts | To ±0.5LSB, $C_L$=100pF, $R_L$=10kΩ | | 2.2 | 7 | V/μs |
| Glitch Energy | From 7FF to 800, $V_{DD}$=5V | | 8 | | nV-sec |
| Analog Crosstalk | $V_{DD}$=5V | | 0.5 | | nV-sec |
| Channel Crosstalk | $V_{DD}$=5V | | 0.8 | | nV-sec |
| Multiplying Bandwidth | $V_{REF}$=2V±0.2Vp-p | | 340 | | kHz |
| Output Noise Spectral Density | Digital Code=0x840, 1kHz | | 110 | | nV/√Hz |
| | Digital Code=0x840, 10kHz | | 90 | | |

**AC and Timing**

$V_{DD}$=2.7V~5.5V, $V_{REF1,2}$=VDD, $C_L$=200pF to ground, $f_{SCLK}$=30MHz, input data between 48 to 4047, unless otherwise noted, $T_A$=25°C.

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Clock Frequency | $f_{SCLK}$ | | | 40 | | MHz |
| | | $T_{MIN} \leq T_A \leq T_{MAX}$ | | | 30 | |
| SCLK Cycle | $1/f_{SCLK}$ | | | 25 | | ns |
| | | $T_{MIN} \leq T_A \leq T_{MAX}$ | 33 | | | |
| SCLK High-level Time | $t_{CH}$ | | | 7 | | ns |
| | | $T_{MIN} \leq T_A \leq T_{MAX}$ | 10 | | | |
| SCLK Low-level Time | $t_{CL}$ | | | 7 | | ns |
| | | $T_{MIN} \leq T_A \leq T_{MAX}$ | 10 | | | |
| Setup Time, $\overline{SYNC}$ to SCLK Falling Edge | $t_{SS}$ | | | 3 | $1/f_{SCLK}$-3 | ns |
| | | $T_{MIN} \leq T_A \leq T_{MAX}$ | 10 | | | |
| Data Setup Time | $t_{DS}$ | | | 1 | | ns |
| | | $T_{MIN} \leq T_A \leq T_{MAX}$ | 2.5 | | | |
| Data Hold Time | $t_{DH}$ | | | 1 | | ns |
| | | $T_{MIN} \leq T_A \leq T_{MAX}$ | 2.5 | | | |
| $\overline{SYNC}$ Hold Time after the 16th SCLK Falling Edge | $t_{SH}$ | | 3 | | $1/f_{SCLK}$-3 | ns |
| | | $T_{MIN} \leq T_A \leq T_{MAX}$ | 3 | | | |
| $\overline{SYNC}$ High-level Time | $t_{SYNC}$ | | | 5 | | ns |
| | | $T_{MIN} \leq T_A \leq T_{MAX}$ | 15 | | | |

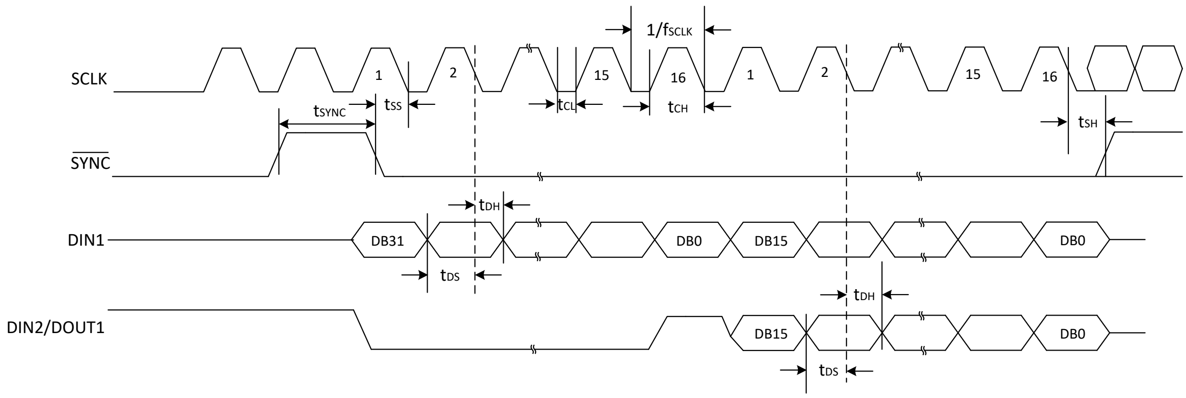



Figure 1. Serial Timing

## TYPICAL CHARACTERISTIC CURVE

Unless otherwise noted, $V_{DD}$=2.7V~5.5V, $f_{SCLK}$=30MHz, $V_{REF1,2}$=$V_{DD}$, $T_A$=25°C。

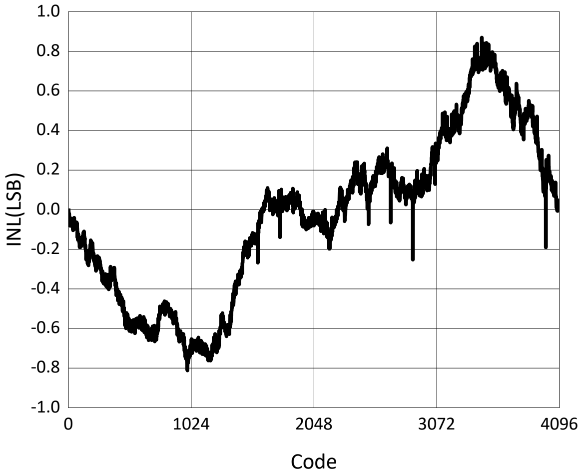



Figure 2. INL VS.Code

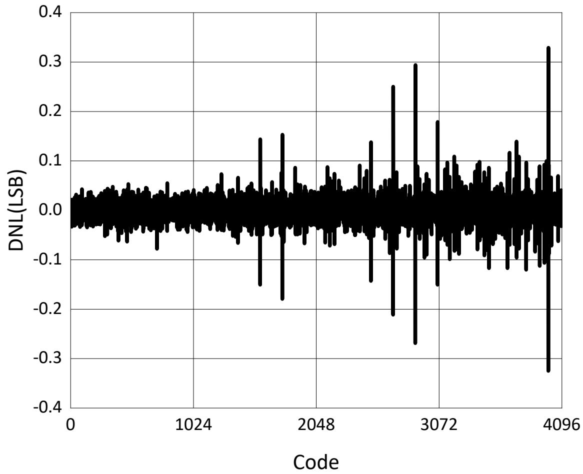



Figure 3. DNL VS.Code

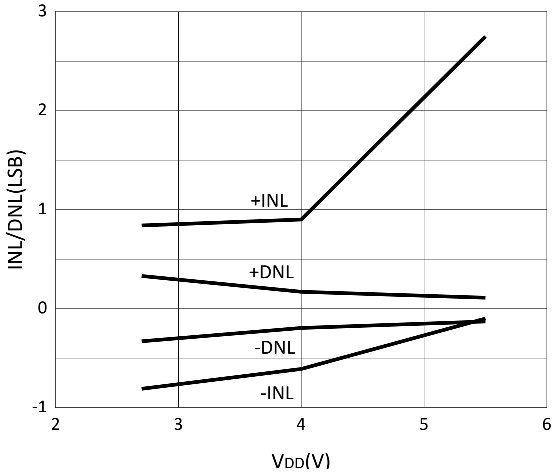



Figure 4. INL/DNL VS. $V_{DD}$

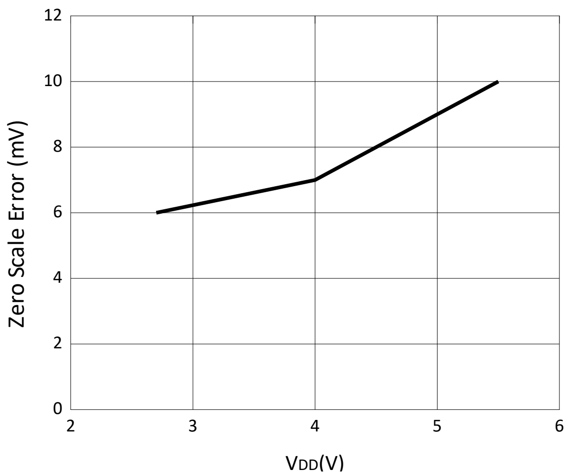



Figure 5. Zero Scale Error VS. $V_{DD}$

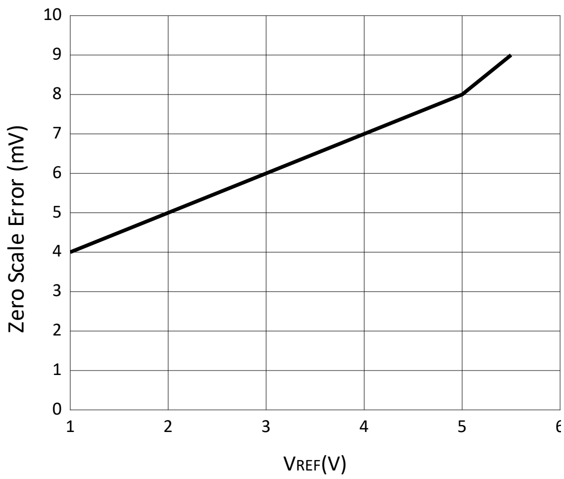



Figure 6. Zero Scale Error VS. $V_{REF}$

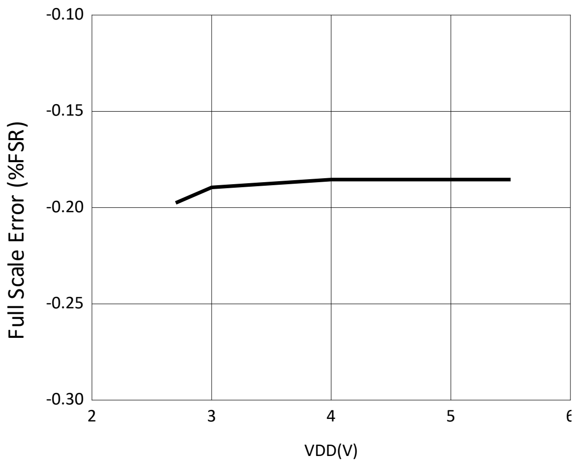



Figure 7. Full Scale Error VS. VDD

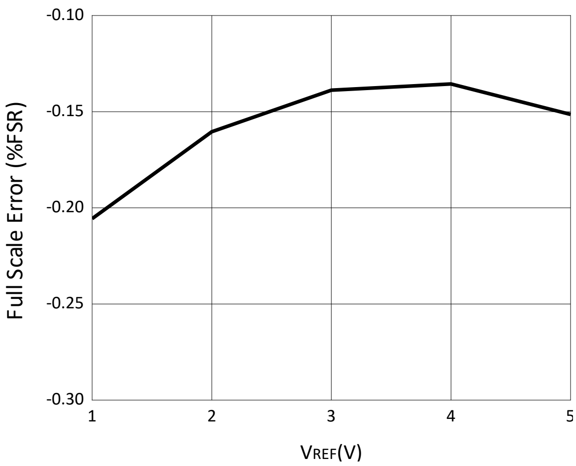



Figure 8. Full Scale Error VS. VREF

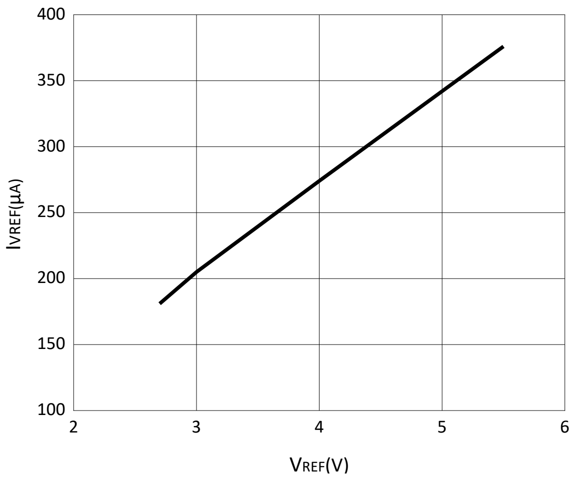



Figure 9. IVREF VS. VREF

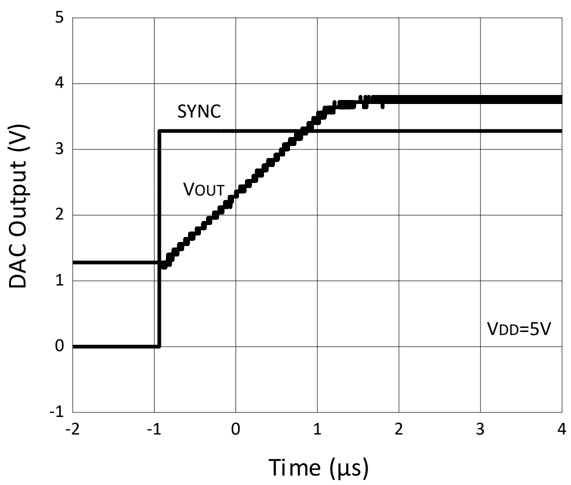



Figure 10. Setup Time

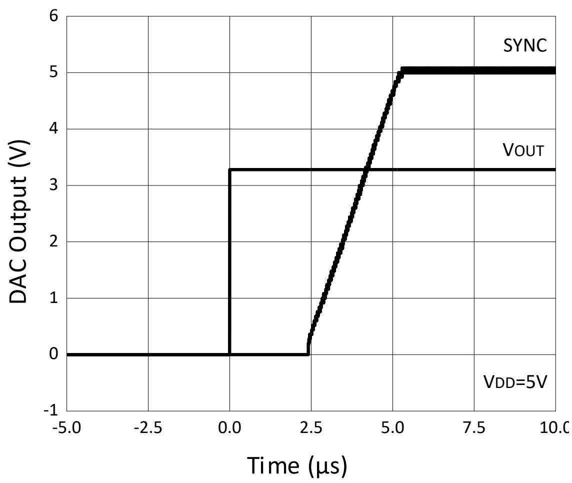



Figure 11. Wake Time

## FUNCTION DESCRIPTION

### Overall Function

The MS5208T/MS5208N is a 12bit, single power supply DAC. It adopts resistor string architecture and integrates serial interface and rail-to-rail output buffer.

Output voltage can be expressed:

$$VOUT=\frac{VREF\times D}{2^{n}}$$

### Reference Voltage

The MS5208T/MS5208N provides reference voltage for internal DAC by VREF1 and VREF2. VREF1 provides the reference voltage for channel A to channel D. VREF2 provides the reference voltage for channel E to channel H.

### Serial Interface

The 3-wire serial interface is compatible with SPI, QSPI, MICROWIRE and most DSP. The maximum operation frequency can reach 40MHz. A valid serial sequence includes 16 SCLK falling edges (see Figure 1).

After $\overline{SYNC}$ is pulled low, the data on DIN is successively input to register on the 16 SCLK falling edges. When $\overline{SYNC}$ is pulled high, the input ends between the 16th and 17th SCLK falling edge. Then the last 16bit data is processed.

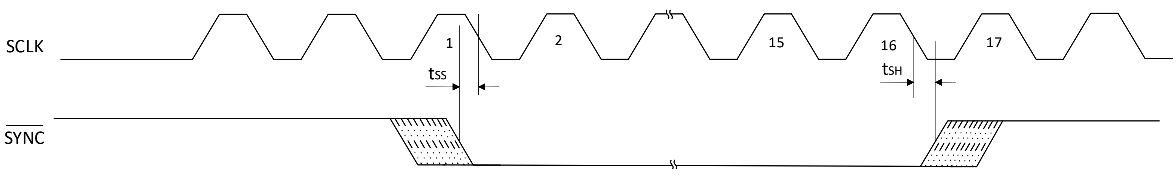



Figure 12. $\overline{SYNC}$ Setup and Hold Time

Write operation would be stopped if $\overline{SYNC}$ is pulled high in advance before the 16th falling edge. And the data written to register would be invalid. The MS5208T/MS5208N would enter daisy chain mode if $\overline{SYNC}$ is pulled high after the 17th falling edge. The input for last 16 SCLK falling edges is as data and proceed subsequent operation.

### Daisy Chain Mode

Daisy chain mode allows to use single serial interface and communicate with any number of the MS5208T/MS5208N. As long as 16*n data is input, all DACs in system would be updated together when $\overline{SYNC}$ is pulled high.

All DACs in system must share with the same SCLK and $\overline{SYNC}$ . At the same time, the prior DAC’s DOUT is connected with next DAC’s DIN (see Figure 13). Daisy chain mode starts with $\overline{SYNC}$ falling edge and ends with $\overline{SYNC}$ rising edge. Write sequence is 16*n if daisy chain consists of n DACs. The maximum SCLK rate of daisy chain mode is 30MHz.

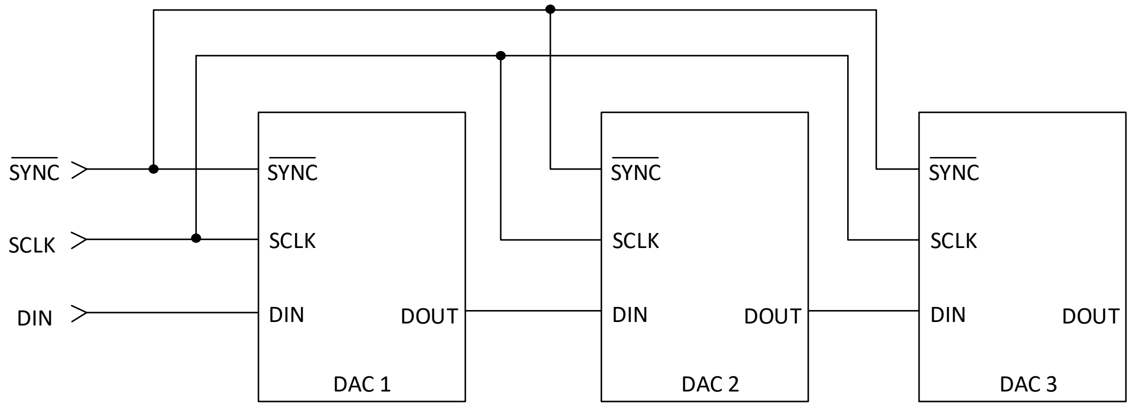



Figure 13. Daisy Chain Configuration

After $\overline{\text{SYNC}}$ falling edge, DOUT outputs 0x0001 in prior 16 SCLK clock cycles. From 17th SCLK clock cycle, the data for delay 16bit on DIN terminal starts to be output successively (see Figure 14).

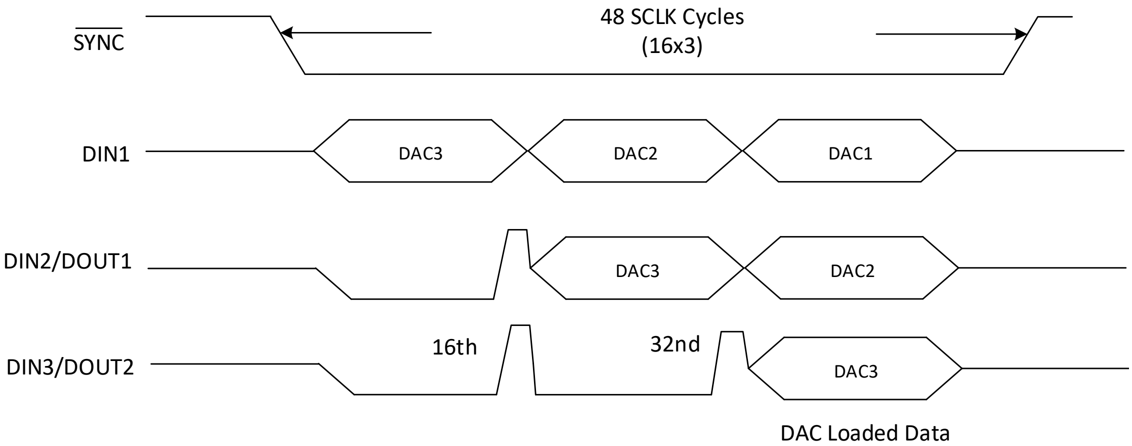



Figure 14. Daisy Chain Timing

**DAC Input Data Update**

The MS5208T/MS5208N has two operation modes, write register mode (WRM) and write through mode (WTM). It is decided by the 4bit MSB of input data (DB15 to DB12) (see Table 1). The defaulted state is WRM state after power-up. Each state can be kept until another operation mode is switched by command.

Tab1e. Operation Mode

| DB[15:12] | DB[11:0] | Description |
|---|---|---|
| 1000 | XXXXXXXXXXXX | WRM: Write Data but Not Update Output Result |
| 1001 | XXXXXXXXXXXX | WTM: Write Data and Update Output Result |

When DB15 is 0, DB14-DB12 are address bits, select output channel. The final result is combined by current mode (see Table 2).

Table 2. Command Affected by WRM and WTM

| DB15 | DB[14:12] | DB[11:0] | Description |
|---|---|---|---|
| 0 | 000 | D11 D10 ... D1 D0 | WRM: Only Write Data to Channel A<br>WTM: Write Data to Channel A and Update Output Result |
| 0 | 001 | D11 D10 ... D1 D0 | WRM: Only Write Data to Channel B<br>WTM: Write Data to Channel B and Update Output Result |
| 0 | 010 | D11 D10 ... D1 D0 | WRM: Only Write Data to Channel C<br>WTM: Write Data to Channel C and Update Output Result |
| 0 | 011 | D11 D10 ... D1 D0 | WRM: Only Write Data to Channel D<br>WTM: Write Data to Channel D and Update Output Result |
| 0 | 100 | D11 D10 ... D1 D0 | WRM: Only Write Data to Channel E<br>WTM: Write Data to Channel E and Update Output Result |
| 0 | 101 | D11 D10 ... D1 D0 | WRM: Only Write Data to Channel F<br>WTM: Write Data to Channel F and Update Output Result |
| 0 | 110 | D11 D10 ... D1 D0 | WRM: Only Write Data to Channel G<br>WTM: Write Data to Channel G and Update Output Result |
| 0 | 111 | D11 D10 ... D1 D0 | WRM: Only Write Data to Channel H<br>WTM: Write Data to Channel H and Update Output Result |

In additional to above commands, there are three special commands. These special commands can be done in any time and are independent of current mode (see Table 3).

Table 3. Special Command

| DB[15:12] | DB[11:0] | Description |
|---|---|---|
| 1010 | X X X X H G F E D C B A | Select Several Channels and Update Output. |
| 1011 | D11 D10 ... D1 D0 | Data is written to channel A and update 8 channels. |
| 1100 | D11 D10 ... D1 D0 | Data is written to 8 channels simultaneously and update. |

Command 1010: If channel address in input data is set as 1, the corresponding channel can update output result. The function can update several channels simultaneously.

Command 1011: D11-D0 data is written to channel A and update 8 channels simultaneously.

Command 1100: D11-D0 data is written to 8 channels simultaneously and update 8 channels. The mode is called as broadcast mode. The same data is broadcast to all channels. The command is usually used to set all DAC outputs to certain voltage.

**Power-up Reset**

Power-up reset circuit controls the output voltage of 8 channels at power-up. Output always keeps 0 at power-up until a group of valid data is written.

**Power-down Mode**

There are three power0down modes to select differential outputs (see Table 4). DB15-DB12 command bits select power-down mode. Power-down channel is selected by DB7-DB0 bits and several channels can be selected at a time.

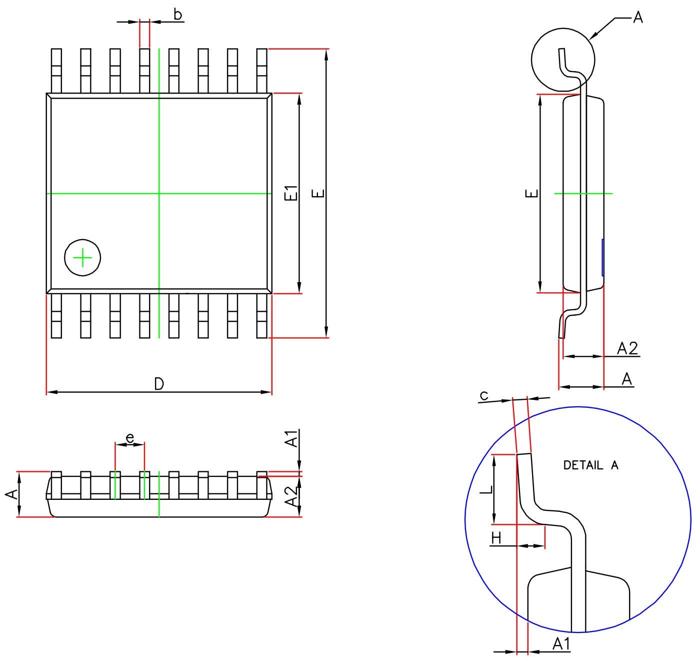
The value of DAC register is not affected at power-down. The minimum power dissipation can be realized by pulling $\overline{\text{SYNC}}$ high, pulling DIN low and disabling SCLK.

Table 4. Power-down Mode

| DB[15:12] | DB[11:8] | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Output Impedance |
|---|---|---|---|---|---|---|---|---|---|---|
| 1101 | XXXX | H | G | F | E | D | C | B | A | Hi-Z |
| 1110 | XXXX | H | G | F | E | D | C | B | A | 100kΩ |
| 1111 | XXXX | H | G | F | E | D | C | B | A | 2.5kΩ |

## PACKAGE OUTLINE DIMENSIONS

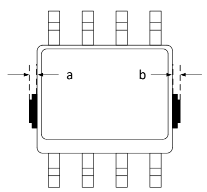
**TSSOP16**




| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | - | 1.200 | - | 0.047 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| A2 | 0.800 | 1.000 | 0.031 | 0.039 |
| b | 0.190 | 0.300 | 0.007 | 0.012 |
| c | 0.090 | 0.200 | 0.004 | 0.008 |
| D | 4.900 | 5.100 | 0.193 | 0.201 |
| E | 6.250 | 6.550 | 0.246 | 0.258 |
| E1 | 4.300 | 4.500 | 0.169 | 0.177 |
| e | 0.650(BSC) | | 0.026(BSC) | |
| L | 0.500 | 0.700 | 0.020 | 0.028 |
| H | 0.250(TYP) | | 0.010(TYP) | |
| θ | 1° | 7° | 1° | 7° |

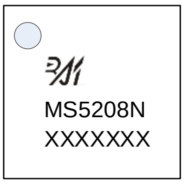
Note: In addition to the package size, a and b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.



## MARKING and PACKAGING SPECIFICATION

### 1. Marking Drawing Description




Product Name: MS5208T, MS5208N

Product Code: XXXXXXX

### 2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

### 3. Packaging Specification

| Device | Package | Piece/Reel | Reel/Box | Piece /Box | Box/Carton | Piece/Carton |
|---|---|---|---|---|---|---|
| MS5208T | TSSOP16 | 3000 | 1 | 3000 | 8 | 24000 |
| MS5208N | QFN16 | 4000 | 1 | 4000 | 8 | 32000 |

**STATEMENT**

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.
  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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