

## 16bit, Single-Channel, 200kSPS, SAR ADC

### FEATURES

- No Missing Resolution: 16bit
- Dynamic Range: 88dB
- SINAD: 87dB(20kHz)
- Analog Input Range: 0 to VREF  
(VREF up to VDD)
- External Reference
- VDD Single Power Supply: 2.7V to 5.5V,  
Logic Power Supply: 1.8V to VDD
- Serial Interface: Compatible with SPI,  
MICROWIRE, QSPI and DSP
- Power Dissipation: 7.5mW (5V@100kSPS),  
23mW (5V@200kSPS)
- Standby Current: 200nA@5V

### APPLICATIONS

- Battery-powered Equipment
- Medical Device
- Mobile Communication
- PDAs
- Data Acquisition
- Instrumentation
- Process Control

### PRODUCT DESCRIPTION

The MS5172M/MS5172D is single-channel, 16bit SAR ADC and is powered by single power.

The MS5172M/MS5172D includes a low power dissipation, high-speed data sample and no missing code 16bit SAR ADC and an internal conversion clock.

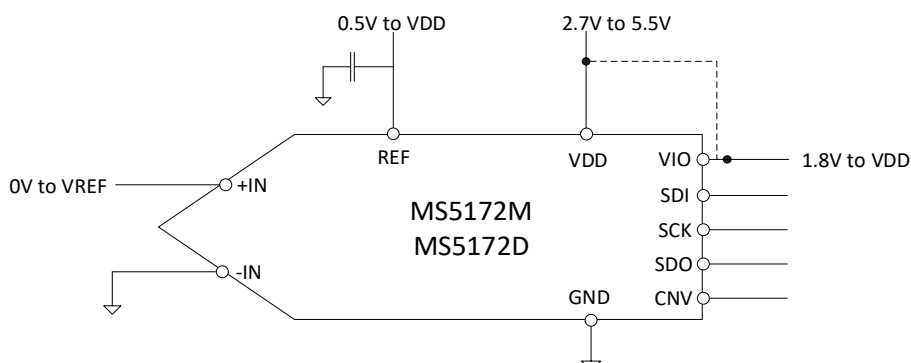
The MS5172M/MS5172D uses general serial interface to receive the conversion result. The MS5172M/MS5172D also integrates track and hold circuit featured by low noise, wide bandwidth, short aperture delay. SPI interface can also connect several ADCs to a 3-wire bus in daisy chain.

The MS5172M is available in MSOP10 package and The MS5172D is available in DFN10 package. The operating temperature is from -40°C to +125°C.

### PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5172M	MSOP10	MS5172M
MS5172D	DFN10	MS5172D

### BLOCK DIAGRAM

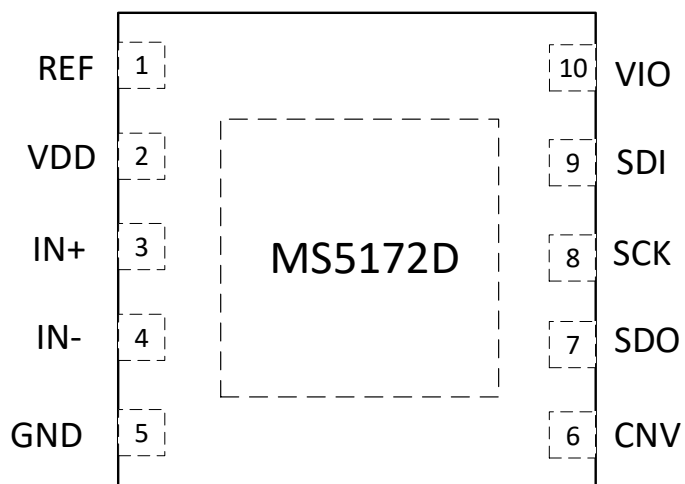
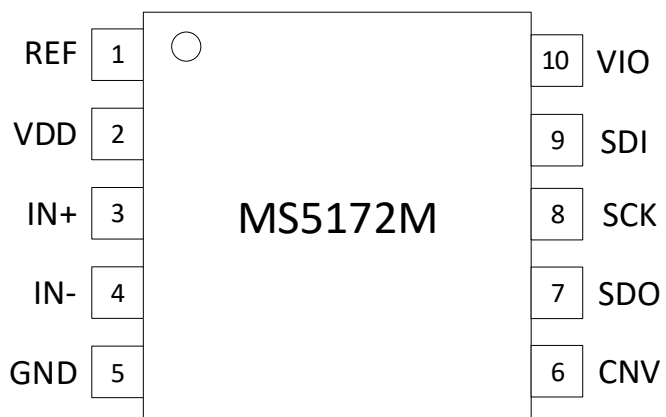


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## PIN CONFIGURATION



## PIN DESCRIPTION

Pin	Name	Type	Description
1	REF	I	Reference Voltage Input. A 10 $\mu$ F decoupling capacitor is required and is placed as close to REF as possible. The range is from 0.5V to VDD.
2	VDD	-	Power Supply
3	IN+	I	Analog Channel Positive Input Pin
4	IN-	I	Analog Channel Negative Input Pin
5	GND	-	Ground
6	CNV	I	Conversion Input. CNV initiates the conversion on the rising edge. Select the interface adopts chain mode or chip select mode. In chain mode, data is read when CNV is high-level. In chip select mode, SDO is enabled when CNV is low-level.
7	SDO	O	Serial Data Output
8	SCK	I	Serial Data Clock Input
9	SDI	I	Serial Data Input. ADC interface mode is selected by following way. On the rising edge of CNV, chain mode is selected if SDI is low-level. In this mode, SDI is as data input and links several ADC's conversion results to single SDO line. The data on SDI is output to SDO after the delay for 16 SCK periods. On the rising edge of CNV, chip select mode is selected if SDI is high-level. In this mode, when SDI and CNV are low-level, serial output signal can all be enabled. When conversion is completed, if SDI or CNV is low-level, busy indicator is enabled.
10	VIO	-	Digital Input/Output Interface Power Supply.

## ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	$V_{DD}$	-0.3 ~ +7.0	V
Analog Input Voltage	IN	-0.3 ~ $V_{DD}+0.3$	V
Reference Voltage	$V_{REFIN}$	-0.3 ~ $V_{DD}+0.3$	V
Digital Input Voltage		-0.3 ~ $V_{IO}+0.3$	V
Digital Output Voltage		-0.3 ~ $V_{IO}+0.3$	V
Input Port Current		10	mA
Operating Temperature	$T_A$	-40 ~ 125	°C
Storage Temperature	$T_{STG}$	-65 ~ 150	°C
Lead Temperature (10s)		260	°C
ESD(HBM)	$V_{ESD}$	±3000	V

## ELECTRICAL CHARACTERISTICS

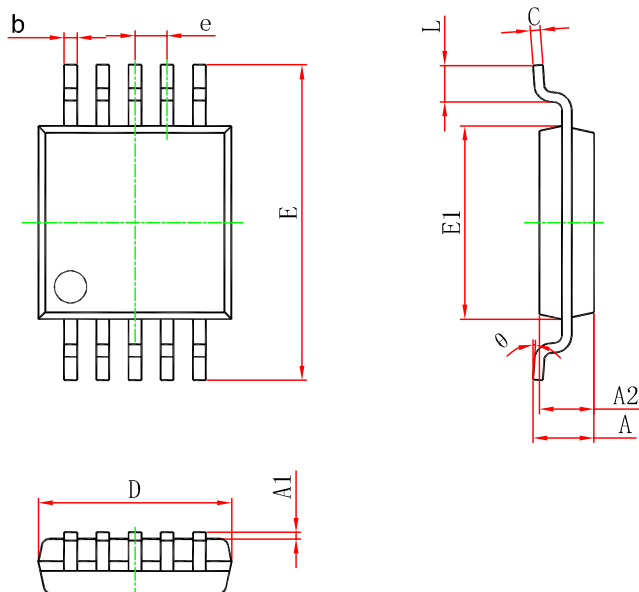
Unless otherwise noted,  $V_{DD} = 2.7V$  to  $5.5V$ ,  $V_{REF} = V_{DD}$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .

Parameter	Condition	Min	Typ	Max	Unit
<b>Analog Input</b>					
Analog Input Voltage	+IN - (-IN)	0		$+V_{REF}$	V
Analog Absolute Input Voltage	+IN	-0.1		$V_{DD}+0.1$	V
	-IN	-0.1		+0.1	V
Analog Input CMRR	$f_{IN}=200kHz$		68		dB
Leakage Current@25°C	Acquisition phase		1		nA
<b>Conversion Rate</b>					
Transmission Rate	$V_{DD}=4.5V$ to $5.0V$	0		200	kSPS
Transient Response	Full-scale step		0.4		$\mu s$
<b>Accuracy</b>					
No Missing Codes			16		Bits
Integral Non-linearity Error	$V_{REF}=2.048V$	-6		+6	LSB
	$V_{REF}=4.096V$	-7.5		+7.5	
Differential Non-linearity Error	$V_{REF}=2.048V$	-1.5	$\pm 0.5$	+1.5	LSB
	$V_{REF}=4.096V$	-1.5	$\pm 0.5$	+1.5	
Gain Error		-30		+30	LSB
Gain Error Temperature Drift			$\pm 0.3$		ppm/ $^{\circ}C$
Offset Error	$V_{DD}=2.7V$ to $5.5V$	-3.5	$\pm 0.7$	+3.5	mV
Offset Error Temperature Drift			$\pm 0.3$		ppm/ $^{\circ}C$
Power Supply Sensitivity	$V_{DD}=5V \pm 5\%$		$\pm 1.5$		LSB
<b>AC Accuracy</b>					
Signal-to-Noise Ratio (SNR)	$f_{IN}=20kHz$ , $V_{REF}=2.048V$		88		dB
Signal-to- Noise-and-Distortion Ratio (SINAD)	$f_{IN}=20kHz$ , $V_{REF}=2.048V$		87		dB
	$f_{IN}=20kHz$ , -60dB input, $V_{REF}=2.048V$		33.5		

Parameter	Condition	Min	Typ	Max	Unit
Total Harmonic Distortion (THD)	$f_{IN}=20\text{kHz}$ , $V_{REF}=2.048\text{V}$		-92		dB
Spurious-Free Dynamic Range	$f_{IN}=20\text{kHz}$ , $V_{REF}=2.048\text{V}$		100		dB
<b>Sampling Dynamics</b>					
-3dB Input Bandwidth	Full bandwidth		12		MHz
Aperture Delay	$V_{DD}=5\text{V}$		2.5		ns
<b>Reference Voltage</b>					
Voltage Range	REF input	0.5		$V_{DD}+0.1$	V
Leakage Current	200kSPS, $V_{REF}=5\text{V}$		100		$\mu\text{A}$
<b>Digital Input</b>					
Input Low-level Voltage		-0.3		$+0.3 \times V_{IO}$	V
Input High-level Voltage		$0.75 \times V_{IO}$		$V_{IO}+0.3$	V
Input Low-level Current			$\pm 1$		$\mu\text{A}$
Input High-level Current			$\pm 1$		$\mu\text{A}$
<b>Digital Output</b>					
Output High-level Voltage	$I_{SOURCE}=-500\mu\text{A}$	$V_{IO}-0.3$			V
Output Low-level Voltage	$I_{SINK}=+500\mu\text{A}$			0.4	V
<b>Power Supply</b>					
VDD	Specified performance	2.7		5.5	V
VIO	Specified performance	1.8		$V_{DD}+0.3$	V
Standby Current	$V_{DD}=V_{IO}=5\text{V}$ , $25^\circ\text{C}$		200		nA
Power Dissipation	$V_{DD}=5\text{V}$ , 100kSPS conversion rate		7.5		mW
	$V_{DD}=5\text{V}$ , 200kSPS conversion rate		23		mW

# PACKAGE OUTLINE DIMENSIONS

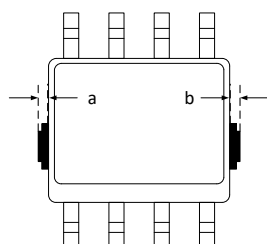
## MSOP10



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	-	1.100	-	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.330	0.007	0.013
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50BSC		0.020BSC	
E	4.750	5.050	0.187	0.199
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

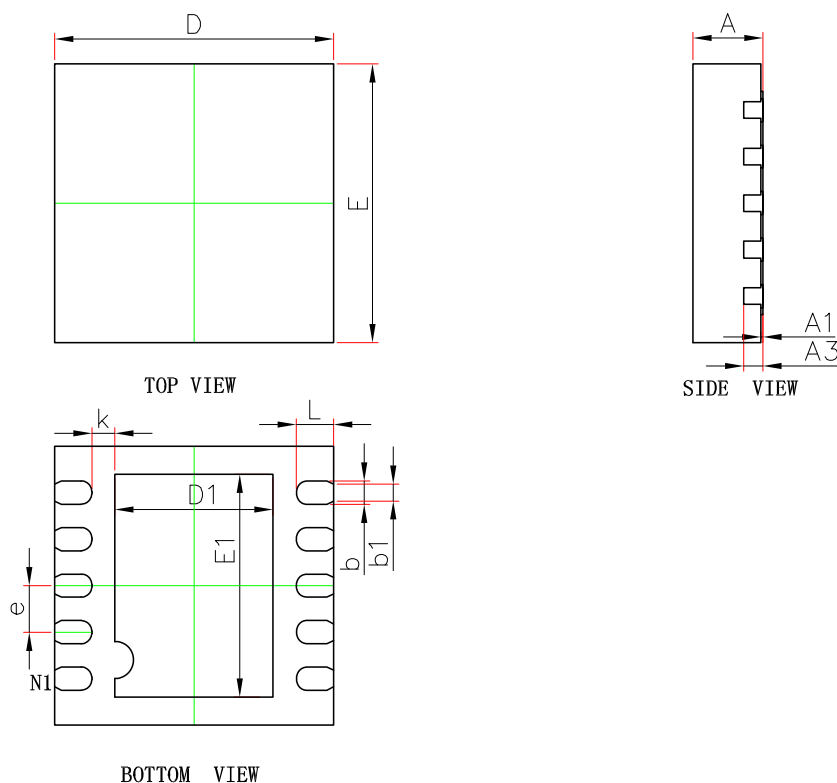
Note: In addition to the package size, a and b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.





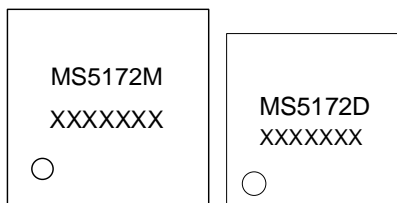
## DFN10



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	1.600	1.800	0.063	0.071
E1	2.300	2.500	0.091	0.098
b	0.200	0.300	0.008	0.012
b1	0.180REF		0.007REF	
e	0.500BSC		0.020BSC	
k	0.250REF		0.010REF	
L	0.324	0.476	0.013	0.019

## MARKING and PACKAGING SPECIFICATION

### 1. Marking Drawing Description



Product Name: MS5172M, MS5172D

Product Code: XXXXXXX

### 2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

### 3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5172M	MSOP10	3000	1	3000	8	24000
MS5172D	DFN10	5000	1	5000	8	40000

**STATEMENT**

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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