

2.7V to 5.5V, Serial Input, Voltage Output, 16-Bit DAC

FEATURES

- 3V and 5V Single Power Supply
- Low Power Dissipation
- Setup Time: 1.2 μ s
- Unbuffered Voltage Output, Directly Drive 60k Ω Load
- Low Glitch: 6nV-s
- Compatible with SPI/QSPI/MICROWIRE and DSP Interface Standards

PRODUCT DESCRIPTION

The MS5531/MS5531M is a single-channel, 16-bit, serial input and voltage output digital-to-analog converter (DAC). It adopts single power supply, which is from 2.7V to 5.5V, and the output range is from 0V to $V_{REF}-1LSB$. Its operating temperature range is from -40°C to +125°C.

The MS5531/MS5531M is featured with unbuffered output, low setup time, low power dissipation and low offset error. These features make it suitable for many kinds of terminal systems.

APPLICATIONS

- Precise Measurement Device
- Automatic Test Device
- Data Acquisition System
- Industrial Process Control

PRODUCT SPECIFICATION

Part Number	Grade	Maximum INL (LSB)	Package	Marking
MS5531	A	± 2	SOP8	MS5531
	B	± 4		
	C	± 8		
	D	± 12		
*MS5531M	-	-	MSOP8	MS5531M

*The package is not available temporarily. If necessary, please contact Hangzhou Ruimeng Sales Department Center.

BLOCK DIAGRAM

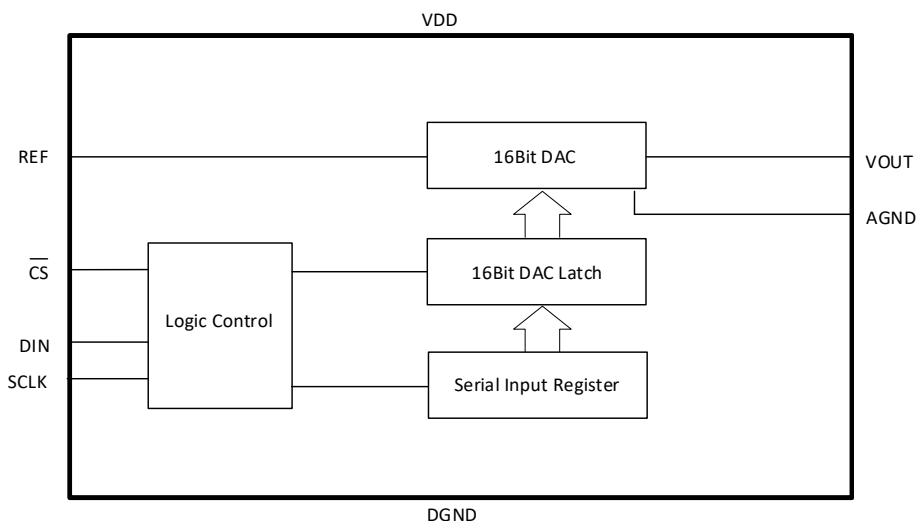
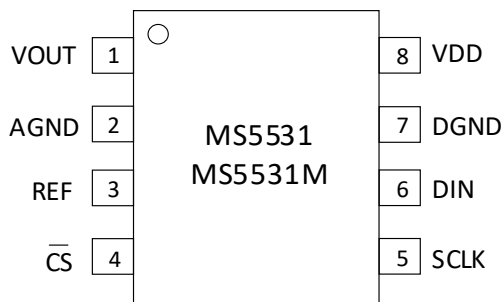


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PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
MS5531/MS5531M			
1	VOUT	O	DAC Analog Output Voltage
2	AGND	-	Analog Reference Ground
3	REF	I	DAC Reference Input Voltage. Voltage Range: 2V to V _{DD}
4	$\overline{\text{CS}}$	I	Chip Select Input Control
5	SCLK	I	Clock Input. Active Rising Edge
6	DIN	I	Serial Data Input
7	DGND	-	Digital Reference Ground
8	VDD	-	Power Supply

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	-0.3 ~ +6.0	V
Input Current	I_{IN}	± 10	mA
Operating Temperature	T_A	-40 ~ +125	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C
ESD (HBM)	V_{ESD}	$>\pm 3000$	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{DD}	2.7	5	5.5	V
Reference Voltage	V_{REF}	2	3	V_{DD}	V

ELECTRICAL CHARACTERISTICS

$V_{DD}=5.0V$, $V_{REF}=3V$, $AGND=DGND=0V$, $T_A=T_{MIN} \sim T_{MAX}$. Note: Unless otherwise noted, $T_A = 25^\circ C \pm 2^\circ C$.

Parameter		Condition	Min	Typ	Max	Unit
Static Characteristic						
Resolution				16		bits
Integral Nonlinearity (INL)	Grade A	$V_{REF}=3V$, $V_{DD}=5V$, $T_A=25^\circ C$		± 0.5	± 2	LSB
	Grade B			± 2	± 4	
	Grade C			± 4	± 8	
	Grade D			± 8	± 12	
Differential Nonlinearity (DNL)		$V_{REF}=3V$, $V_{DD}=5V$, $T_A=25^\circ C$			± 7	LSB
Gain Error		$T_A=25^\circ C$		± 2	± 5	LSB
Gain Error Temperature Coefficient				± 2		ppm/ $^\circ C$
Zero Code Error		$T_A=25^\circ C$		± 2	± 2.5	LSB
Zero Code Error Temperature Coefficient				± 0.1		ppm/ $^\circ C$
Output Characteristic						
Output Voltage			0		$V_{REF}-1LSB$	V
Setup Time, Output Voltage		$C_L=10pF$, $V_{REF}=2.5V$		1.2		μs
Conversion Rate		$C_L=10pF$, 0%-63%, $V_{REF}=2.5V$		4		V/ μs
Digital-to-Analog Glitch Impulse		1LSB, $V_{REF}=2.5V$		3.8		nV-sec
Digital Feedthrough		$V_{REF}=2.048V$		0.2		nV-sec
Output Noise Density		DAC Code=0 \times 8400, $f=1kHz$		11.8		nV/\sqrt{Hz}
Power Supply Rejection Ratio		$\Delta V_{DD} \pm 10\%$		± 1.0		LSB
DAC Reference Input						
Reference Input Range			2.0		V_{DD}	V
Reference Input Impedance ²				13.5		k Ω
Logic Input						
Input Current				± 1		μA
Input Low Voltage					0.8	V
Input High Voltage			2.4			V
Input Capacitance				10		pF
Input Hysteresis Voltage				0.15		V

Parameter	Condition	Min	Typ	Max	Unit
Power Supply					
Power Supply		2.7		5.5	V
Current	Digital Input: 0		2	20	μA
Power Dissipation	Digital Input: 0		10	100	μW

Note 2: Reference input impedance is related to code. When Code=0x8555, the reference input impedance is minimum.

CLOCK CHARACTERISTICS

Unless otherwise noted: $V_{DD}=2.7V \sim 5.5V$, $V_{REF}=3V$, $V_{INH}=90\% V_{DD}$, $V_{INL}=10\% V_{DD}$, $AGND=DGND=0V$,
 $-40^{\circ}C < T_A < +125^{\circ}C$.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Cycle Frequency	f_{SCLK}			50	MHz
SCLK Cycle Time	t_1	20			ns
SCLK High-level Time	t_2	10			ns
SCLK Low-level Time	t_3	10			ns
Setup Time, \overline{CS} Low to SCLK High	t_4	10			ns
Setup Time, \overline{CS} High to SCLK High	t_5	10			ns
Hold Time, SCLK High to \overline{CS} Low	t_6	10			ns
Hold Time, SCLK High to \overline{CS} High	t_7	10			ns
Data Start Time	t_8	10			ns
Data Hold Time	t_9	4			ns
Valid Time, \overline{CS} High	t_{10}	30			ns

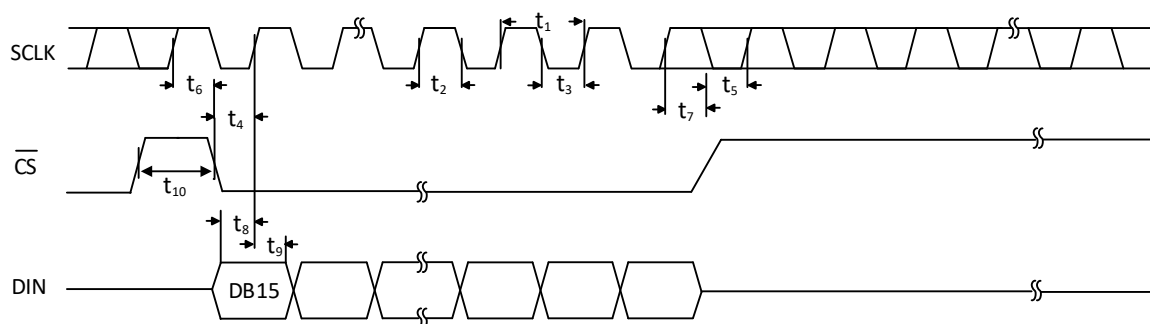


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

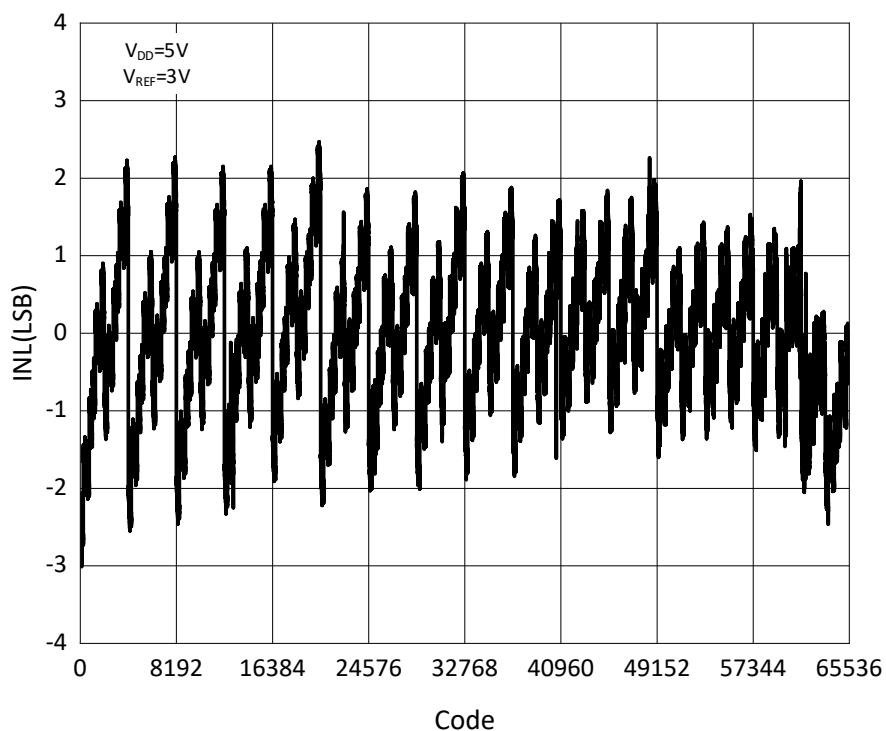


Figure 2. INL VS. Code

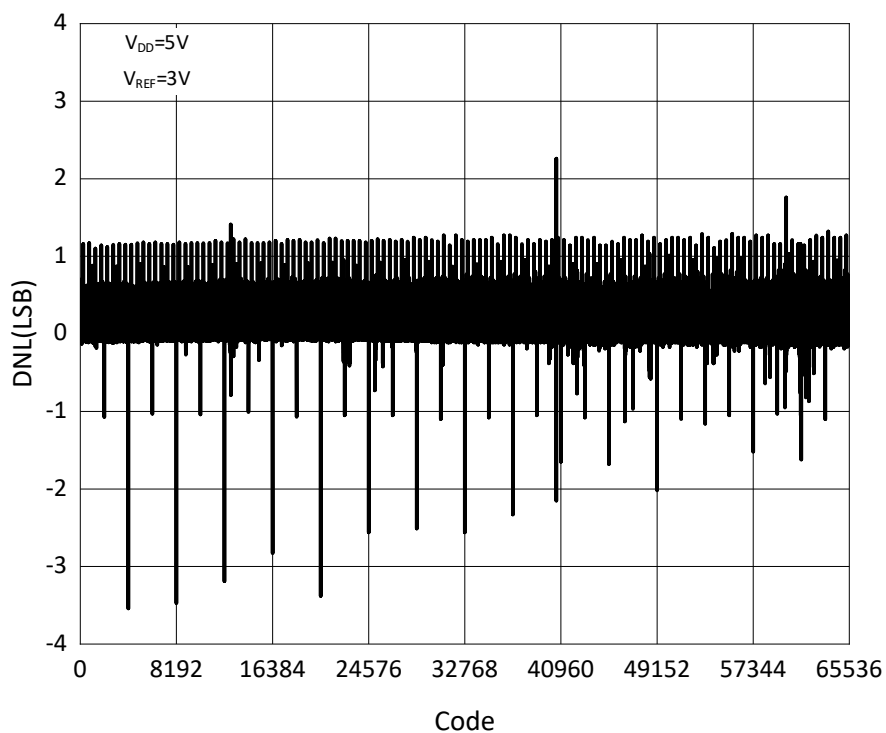


Figure 3. DNL VS. Code

OPERATING PRINCIPLE

The MS5531/MS5531M is a single-channel, 16-bit, serial input and voltage output DAC, whose operating voltage range is from 2.7V to 5.5V. Data is written to the device in 16-bit word format through 3-wire serial interface.

To make sure a known power-up state, the device is designed with power-up reset function.

The defaulted code of the MS5531/MS5531M is 0x8000 after power-up, PIN1(VOUT) output voltage is $0.5 \times V_{REF}$.

Digital-to-Analog Section

DAC architecture includes two matched DAC sections. Figure 4 is simplified circuit diagram. The MS5531/MS5531M adopts segmented DAC architecture. The four MSBs of 16-bit data are decoded to drive 15 switches, E1 to E15. Every switch connects one of 15 matched resistors to AGND or V_{REF} . Other 12 bits in 16-bit data drive S0 to S11 of voltage mode R-2R ladder network.

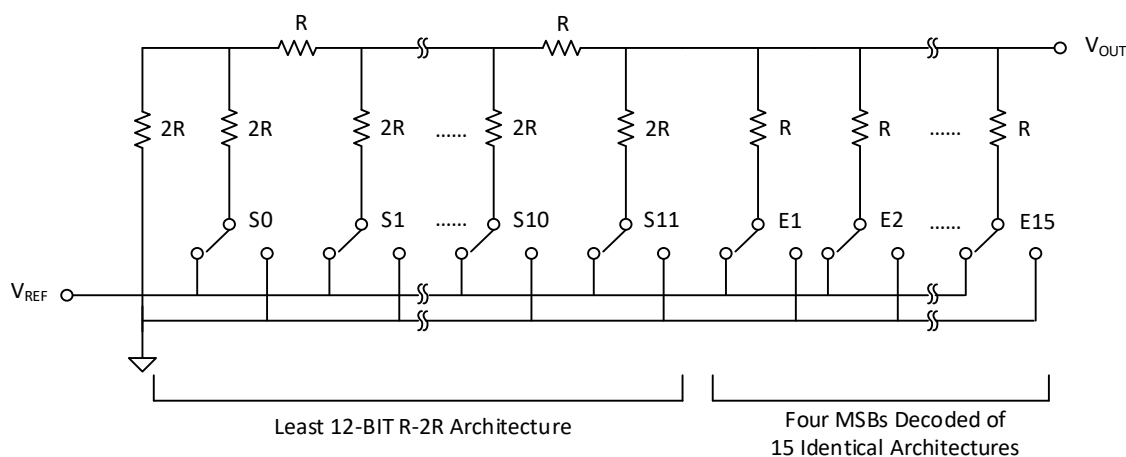


Figure 4. DAC Architecture

With this DAC configuration, output impedance is irrelevant to code, while the input impedance of reference voltage source is highly relevant to code. Output voltage is related to reference voltage, as shown in the following formula:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

Where: D is decimal data word loaded to DAC register. N is DAC resolution. For 2.5V reference voltage, the above formula can be simplified as follows:

$$V_{OUT} = \frac{2.5 \times D}{65536}$$

In this way, V_{OUT} is 1.25V when mid-scale is loaded to DAC; V_{OUT} is 2.5V-1LSB when full-scale is loaded to DAC. LSB is $V_{REF}/65536$.

Serial Interface

The MS5531/MS5531M is controlled by 3-wire serial interface. It can be operated at maximum 50MHz clock frequency and compatible with SPI, QSPI, MICROWIRE and DSP interface standards.

When \overline{CS} is low-level, data is loaded on the rising edge of serial clock SCLK. After 16bit data are all loaded, \overline{CS} becomes from low-level to high-level. DAC updates output voltage.

Data is loaded in 16-bit word format, MSB first.

Output

DAC could drive 60kΩ unbuffered load. The typical output voltage circuit is shown in Figure 5. The reference voltage buffer MS8629 with 3V reference, low offset and zero drift is used in this example.

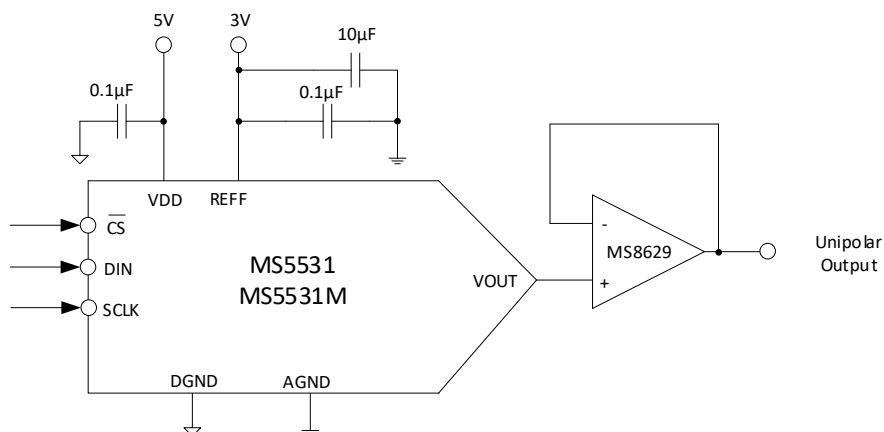


Figure 5. Output Circuit Architecture

If the ideal reference voltage source is used, output voltage in the worst condition could be calculated as follows:

$$V_{OUT-UNI} = \frac{D}{2^{16}} \times (V_{REF} + V_{GE}) + V_{ZSE} + INL$$

Where, $V_{OUT-UNI}$ is output in the worst condition. D is the code loaded into DAC. V_{REF} is the reference voltage applied to device. V_{GE} is gain error with unit(V). V_{ZSE} is zero scale error with unit(V). INL is integral nonlinearity with unit(V).

If use ideal reference voltage source, the relationship is shown as follows.

DAC Code	Output Voltage
1111 1111 1111 1111	$V_{REF} \times (65535/65536)$
1000 0000 0000 0000	$V_{REF} \times (32768/65536) = 1/2 V_{REF}$
0000 0000 0000 0001	$V_{REF} \times (1/65536)$
0000 0000 0000 0000	0V

TYPICAL APPLICATION

Layout Guide

In any circuit focusing on accuracy, the specified performance can be achieved by considering power supply and ground loop layout carefully. The printed circuit board (PCB) used by the MS5531/MS5531M should adopt the design where analog and digital parts are separated and limited within certain field. If the system where the MS5531/MS5531M is located has several devices that require analog ground-digital ground connection, the connection can only be made at one point. And the star point is made as close as possible to the device. The MS5531/MS5531M should have sufficiently large 10 μ F power bypass capacitor, which is parallel to 0.1 μ F capacitor on each power supply and placed as close as possible to the package. It is best to face toward the device. The 10 μ F capacitor is tantalum capacitor. And the 0.1 μ F capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the ceramic capacitor, which provides low impedance ground path at high frequency to process transient current caused by internal logic switch.

Optocoupler Circuit

The MS5531/MS5531M is Schmitt-triggered digital input, which makes it receive slow digital transmission. Therefore, it is suitable for industrial application, which may need to use optocoupler to isolate DAC and controller. The optocoupler isolation circuit structure is shown in Figure 6.

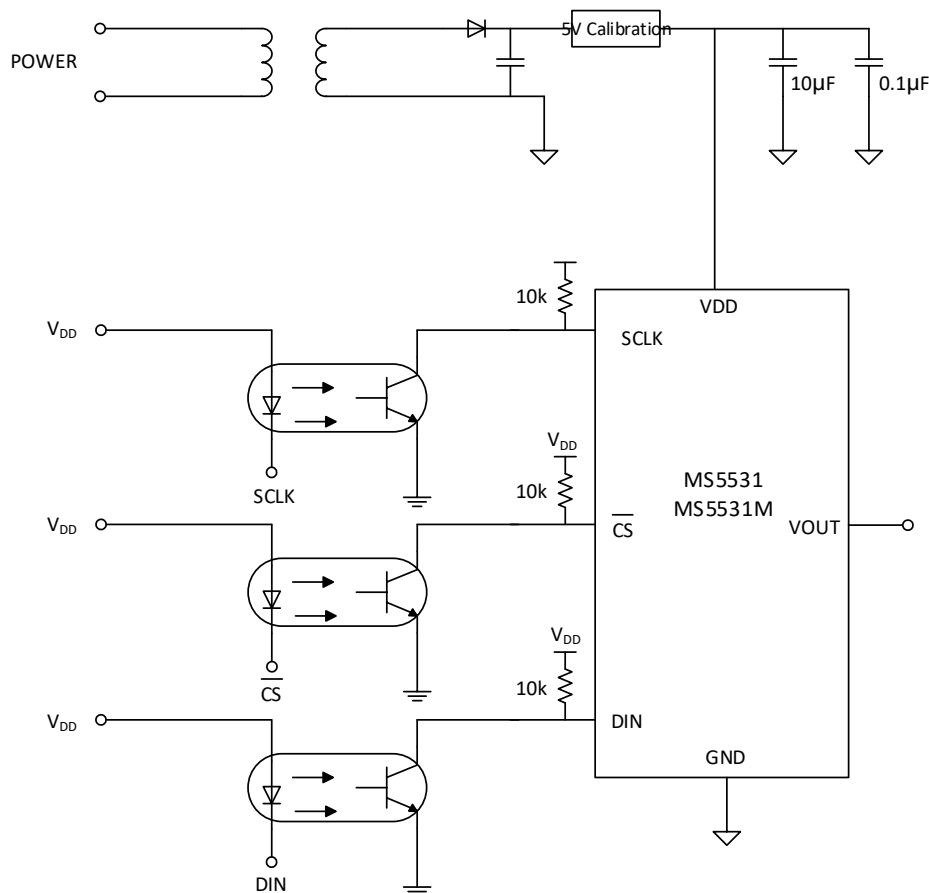


Figure 6. Optocoupler Interface Circuit

Multi-channel Decoding Circuit

The MS5531/MS5531M has the chip select pin $\overline{\text{CS}}$, which can select one or several DACs working together. All the chips receive the same clock and data, but only one chip could receive $\overline{\text{CS}}$ signal at one time. DAC address is decided by decoder. Digital feedthrough exists in digital path. And using burst clock could minimize the impact of digital feedthrough on analog signal channel. The typical circuit structure is shown in Figure 7.

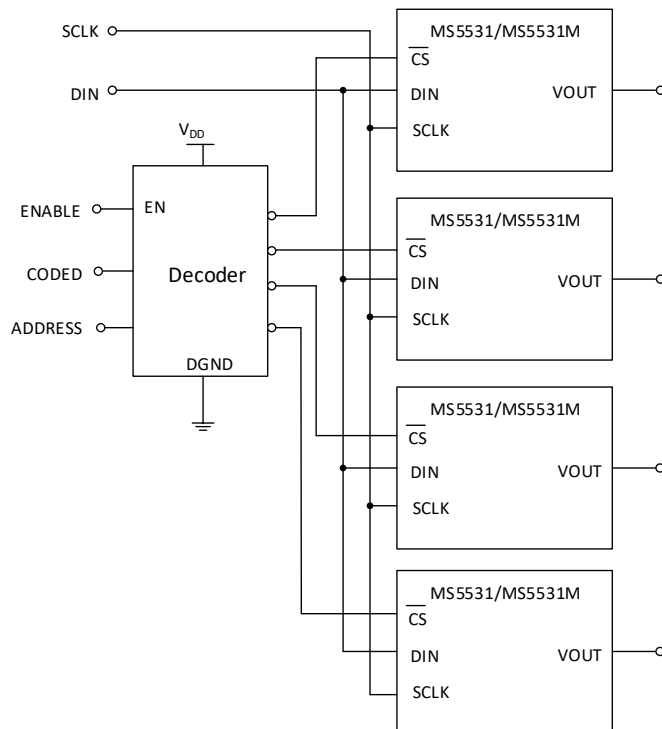
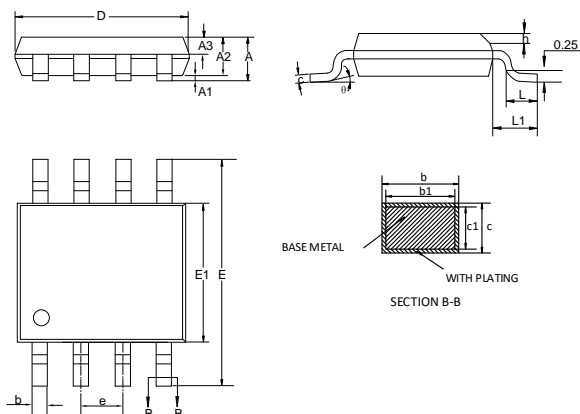


Figure 7. Multiple DACs

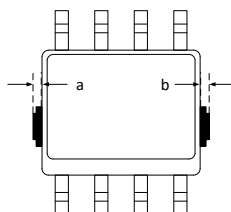
PACKAGE OUTLINE DIMENSIONS

SOP8



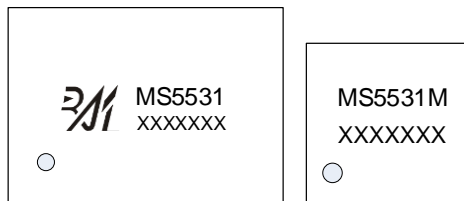
Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0°	-	8°

Note: In addition to the package size, a and b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.



MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS5531, MS5531M

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5531	SOP8	2500	1	2500	8	20000
MS5531M	MSOP8	3000	1	3000	8	24000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.
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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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