High Gain Bandwidth Product FET Input Amplifier

FEATURES

- High Gain Bandwidth Product: 7GHz
- Decompensated, Gain≥ 7V/V (Stable)
- Ultra-Low Bias Current MOSFET input: 2pA
- Low input Voltage Noise: 3nV/ √ Hz
- Slew Rate: 2000V/μs
- Wide Input Common-Mode Range:
  -Less than Positive Power Supply 1.4V
  -High than Negative Power Supply 0.2V
- Output Swing in TIA Configuration: 2.5Vpp (VDD=5V)
- Power Supply: 3.3V to 5.5V
- Quiescent Current: 25mA
- DFN8 Package
- Operating Temperature: -40°C to +125°C

APPLICATIONS

- High-Speed Transimpedance Amplifier
- Laser Distance Measurement
- Laser Radar Receiver
- Level Transmitter (Optical)
- Optical Time Domain Reflectometry (OTDR)
- Distributed Temperature Detection
- 3D Scanner
- Time-of-Flight (ToF) System
- Autonomous Driving System

PRODUCT DESCRIPTION

The MS8258D is a low-noise operational amplifier, suitable for wideband transimpedance and voltage amplifier applications.

When the MS8258D is configured as transimpedance amplifier (TIA), 7GHz gain bandwidth product (GBWP) can support wide closed-loop bandwidth application in high transimpedance gain.

The MS8258D has feedback pin (FB), simplifying the feedback network connection between input and output.

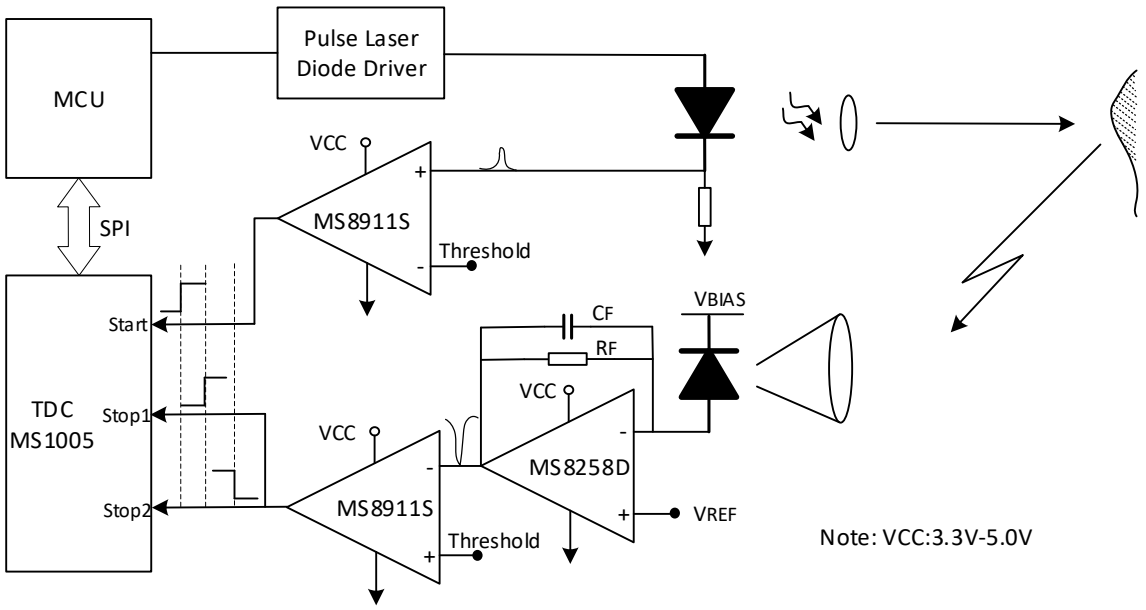
The MS8258D can be used in optical Time-of-Flight (ToF) system. The MS8258D can be used together with time-to-digital converter (TDC). The MS8258D can be used with high-speed analog-to-digital converter (ADC) for high-resolution laser radar system.

The MS8258D is available in DFN8 package. The operating temperature is from -40°C to +125°C.

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS8258D	DFN8	8258D

SYSTEM DIAGRAM



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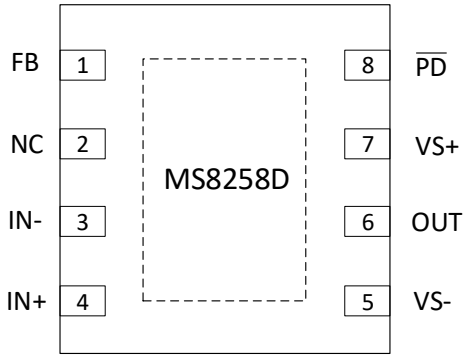
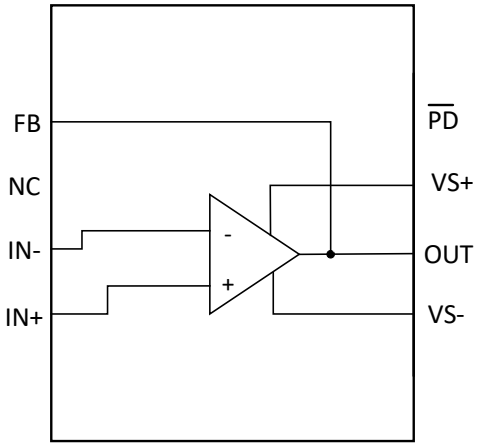
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	FB	I	Feedback Connection to Output of Amplifier
2	NC	-	Not Connection
3	IN-	I	Inverting Input
4	IN+	I	Non-inverting Input
5	VS-	-	Negative Power Supply
6	OUT	O	Positive Output
7	VS+	-	Positive Power Supply
8	$\overline{PD}$	I	$\overline{PD}$ =Logical Low-level: Power Off Mode; $\overline{PD}$ =logical High-level: Normal Operation

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply	V+, V-	5.5	V
Input Voltage	V_{IN+}, V_{IN-}	(V_{S-})-0.5 ~ (V_{S+})+0.5	V
Differential Input Voltage	V_{ID}	1	V
Continuous Input Current	I_{IN}	±10	mA
Continuous Output Current	I_{OUT}	±100	mA
Maximum Junction Temperature	T_{JMAX}	150	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C
ESD(HBM)	V_{ESD}	±4000	V
ESD(CDM)		±750	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V+	3.3	5	5.5	V
Operating Temperature	T_A	-40		+125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{S+} = 5V, V_{S-} = 0V, G = 7V/V, R_F= 453Ω, input common-mode biased at mid-level, R_L= 200Ω at T_A = 25°C.

AC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
-3dB Large Signal Bandwidth	BW_{-3dB}	V_{OUT} = 2Vp-p		740		MHz
		V_{OUT} = 1Vp-p, V_{S+} = 3.3V		600		
-3dB Small Signal Bandwidth	BW_{-3dB}	V_{OUT} = 0.1Vp-p		1.7		GHz
		V_{OUT} = 0.1Vp-p, V_{S+} = 3.3V		1.3		
Gain Bandwidth Product	GBWP	V_{S+} = 5V		7		GHz
		V_{S+} = 3.3V		7		
Slew Rate	SR	V_{OUT} = 2Vp-p		2000		V/μs
		V_{OUT} = 1Vp-p, V_{S+} = 3.3V		1000		
Rise Time	t_R	V_{OUT} = 0.1V step		0.1		ns
Fall Time	t_F	V_{OUT} = 0.1V step		0.1		ns
0.1% Settling Time [1]		V_{OUT} = 2V step		7.5		ns
Overshoot [1]		V_{OUT} = 2V step		12		%
Overload Recovery Time		2 times output overload (0.1％ recovery)		18		ns
Second-order Harmonic Distortion [1]	HD2	V_{OUT} = 2Vp-p, 10MHz		71		dBc
		V_{OUT} = 2Vp-p, 100MHz		51		
		V_{OUT} = 0.5Vp-p, 10MHz, V_{S+} = 3.3V		80		
		V_{OUT} = 0.5Vp-p, 100MHz, V_{S+} = 3.3V		62		
Third-order Harmonic Distortion [1]	HD3	V_{OUT} = 2Vp-p, 10MHz		83		dBc
		V_{OUT} = 2Vp-p, 100MHz		53		
		V_{OUT} = 0.5Vp-p, 10MHz, V_{S+} = 3.3V		84		
		V_{OUT} = 0.5Vp-p, 100MHz, V_{S+} = 3.3V		76		
Input Reference Voltage Noise	e_n	1MHz		3		nV/√Hz
Closed-loop Output Resistance	Z_{OUT}	1MHz		0.40		Ω

DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Open-loop Gain	A_{OL}	V_{S+} = 5V	50	60		dB
		V_{S+} = 3.3V	50	60		
Input Offset Voltage	V_{OS}	T_A=25°C	-5		5	mV
Input Bias Current	I_{BN}	T_A=25°C		2		pA
Offset Current	I_{BOS}	T_A=25°C		2		pA
Common-mode Rejection Ratio	CMRR	V_{CM}=±0.5V	50	60		dB

Input

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Common-mode Input Resistance	R_{CM}			100		MΩ
Common-mode Input Capacitance	C_{CM}			0.6		pF
Differential Input Resistance	R_{DIFF}			100		MΩ
Differential Input Capacitance	C_{DIFF}			0.6		pF
Common-mode Input Voltage	V_{IH}	CMRR > 66 dB, V_{S+} = 3.3V		1.9		V
	V_{IL}	CMRR > 66 dB, V_{S+} = 3.3V		0.2		V
	V_{IH}	CMRR > 66 dB		3.6		V
	V_{IL}	CMRR > 66 dB		0.2		V

Output

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Voltage	V_{OH}	T_A = 25°C, V_{S+} = 3.3 V	2.3	2.4		V
	V_{OL}	T_A = 25°C, V_{S+} = 3.3 V		1.14	1.25	V
	V_{OH}	T_A = 25°C	4.0	4.1		V
	V_{OL}	T_A = 25°C		1.17	1.25	V
Output Driving Current		R_L = 10Ω, A_{OL} > 60 dB	45	50		mA
Output Short-circuit Current	I_{SC}		50	70		mA

Power Supply

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	V_S		3.3		5.5	V
Quiescent Current	I_Q	V_{S+} = 5V	21	25	28	mA
		V_{S+} = 3.3V		23		
		V_{S+} = 5.25V	21	26	29	
Power Supply Rejection Ratio	PSRR+		50	60		dB
	PSRR-		50	60		

Power Down

Parameter	Symbol	Condition	Min	Typ [2]	Max	Unit
Disable Voltage Threshold		V_{S+} = 3.3V		0.7		V
		V_{S+} = 5V		0.7		V
Enable Voltage Threshold		V_{S+} = 3.3V		1.4		V
		V_{S+} = 5V		1.4		V
Power-down Quiescent Current		V_{S+} = 3.3V		120	140	μA
		V_{S+} = 5V		150	170	
$\overline{PD}$ Bias Current		V_{S+} = 3.3V		35		μA
		V_{S+} = 5V		55		
Enable/Disable Delay		V_{S+} = 3.3V, Time to 90%		30		ns
		V_{S+} = 3.3V, Time to 100%		140		
		V_{S+} = 5V, Time to 90%		30		
		V_{S+} = 5V, Time to 100%		110		

Note:

1. Simulation value, just for reference.

2. Typical value represents the normal parameter reference.

APPLICATION INFORMATION

Overview

The MS8258D is featured by 7GHz GBWP and 3nV/ √ Hz low voltage noise and it provides feasible amplifier for wideband transimpedance, high-speed data process and other applications. The MS8258D has excellent dynamic characteristics. In addition to small signal bandwidth, the MS8258D also has 740MHz of large signal bandwidth (V_{OUT} = 2VPP) and a slew rate of 2000 V/μs.

The MS8258D is available in DFN8 package and has a feedback (FB) pin for a simple feedback network connection between the output and inverting input. Excess capacitance on amplifier's input pin can deteriorate phase margin. This problem is especially serious in wide bandwidth application. In order to reduce the effect of stray capacitance on the input node, the MS8258D has an isolation pin (NC) between the feedback and inverting input pin, which increases the physical interval between them, thus reducing parasitic capacitance. The MS8258D also has total capacitance low to 0.6pF.

Slew Rate and Output Voltage

In addition to wide small signal bandwidth, the MS8258D also has high slew rate of 2000 V/μs. The slew rate is a critical parameter in high-speed pulse application. The high slew rate can support the narrow pulse below 10ns such as optical time-domain reflectometry and laser radar. The features of wide bandwidth and high slew rate make it become an ideal high-speed signal amplifier. To achieve high slew rate and low output impedance the output swing of the MS8258D is limited to about 3.0V. The MS8258D is normally used with high-speed pipeline ADC and flash ADC and the latter has limited input range. Therefore, the output swing is coupled with voltage noise, which maximizes the overall dynamic range of the signal chain.

Pin Configuration

The pin configuration is optimized to reduce parasitic inductance and capacitance, which is critical in high-speed analog design. FB pin is internally connected to amplifier output. FB pin is separated from inverting input pin by NC pin. NC pin must keep floating. The pin configuration has two advantages:

1. A feedback resistor (R_F) can be connected between FB and IN- pins on same side rather than bypass package.
2. The isolation function of NC pin is to minimize the capacitance couple between FB and IN- pins.

PCB Layout Guide

To achieve the best performance, pay attention to PCB board layout parasitic effect and external component type. The suggestions to optimize performance:

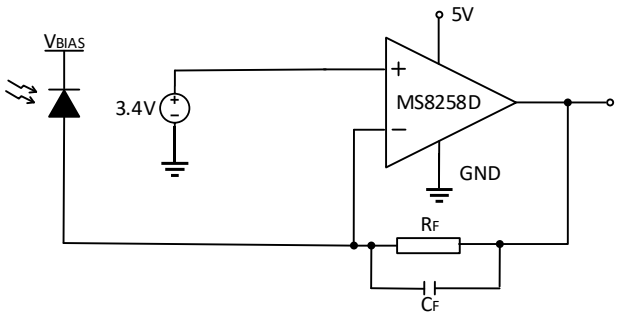
1. Reduce parasitic capacitance from the signal I/O pin to AC ground. Parasitic capacitance on the output and inverting input pins can cause instability. In order to reduce unnecessary capacitance, power and ground traces are not recommended underneath the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. When the amplifier is configured as TIA, if the required feedback capacitance is less than 0.15pF, can consider using two series resistors, each of half the value of a single resistor to reduce the parasitic capacitance of resistor.

2. Reduce the distance from the power-supply pin to high-frequency bypass capacitors (less than 6mm). Use 100pF to 0.1μF C0G and NPO-type decoupling capacitors (rated voltage is at least three times the maximum voltage of amplifier) to ensure that there is a low-impedance path to the amplifier power supply pin. At the device pins, it is not allowed that ground and power plane layout close to the signal I/O pin. Avoid narrow power and ground traces to reduce inductance between the pin and the decoupling capacitor.

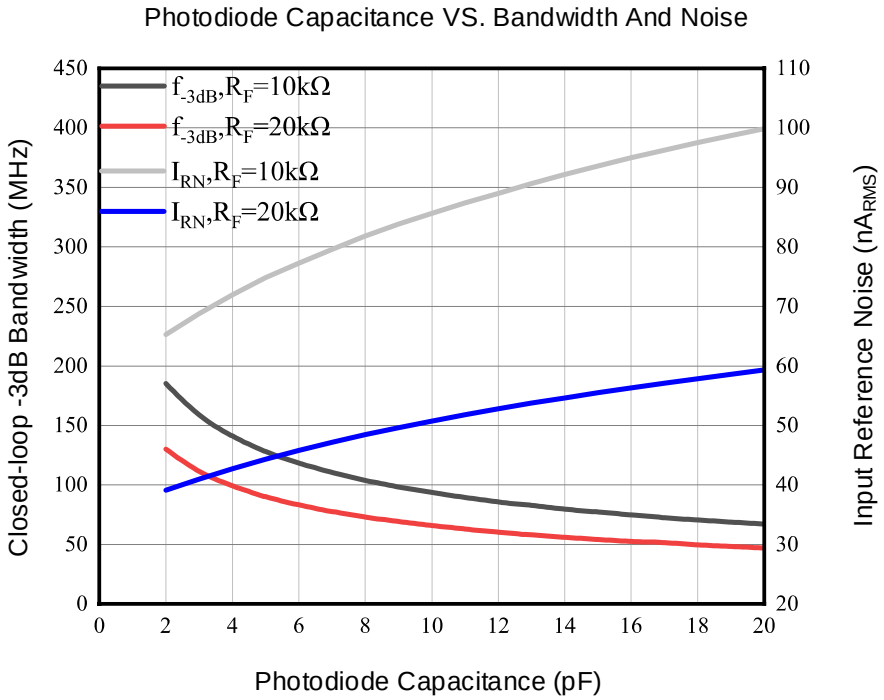
3. It is careful to select and place external components to remain the high-frequency performance of the MS8258D. Use low-reactance resistor and tighter overall layout. Never use wirewound resistor in high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic effect, must place the feedback and series output resistor, if any, as close to the output pin as possible. Place other network components (such as non-inverting input termination resistor) close to output pin. When the MS8258D is configured as voltage amplifier, keep resistor values as low as possible and matched with load drive. Decreasing the resistor value can keep the resistor noise lower and minimize the effect of the parasitic capacitance. It is noted that lower resistor value would increase the dynamic power because R_F and R_G become part of the output load network of the amplifier.

TYPICAL APPLICATION CIRCUIT

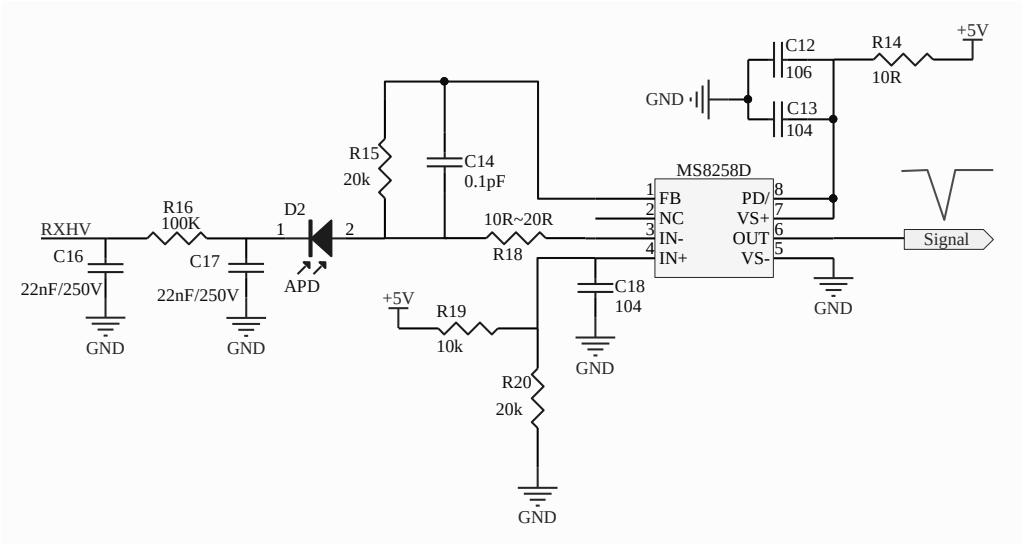
The main application of the MS8258D is as high-speed transimpedance amplifier (TIA). The ratio of total input capacitance and feedback capacitance determines noise gain. In order to improve the TIA closed-loop bandwidth, feedback capacitance is usually smaller than input capacitance, which indicates the high-frequency noise gain is more than 0dB. Therefore, the operational amplifier configured as TIA does not need stable unit gain. The typical application diagram is shown as follows.



When the MS8258D is configured as TIA, the following diagram shows the function relationship between photodiode capacitance and bandwidth, noise. When total noise is calculated, the bandwidth range is from DC to the calculated f_{-3dB} frequency on the left-hand scale.

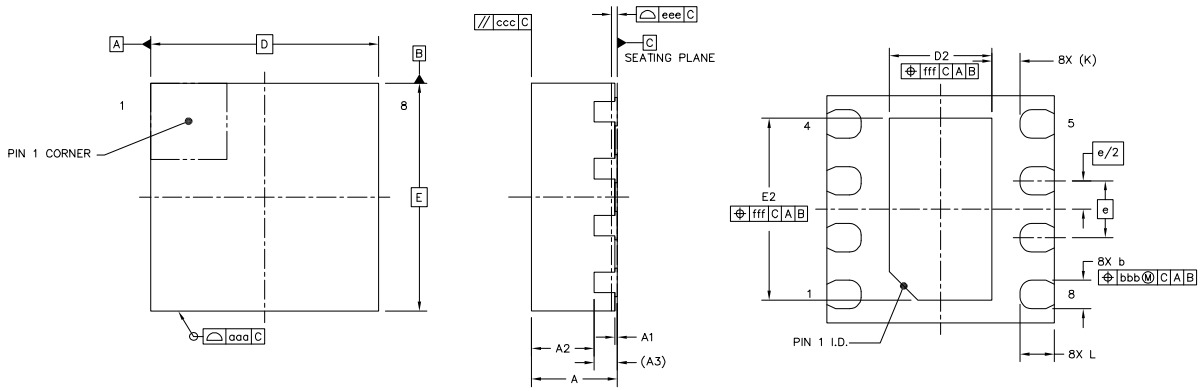


TYPICAL APPLICATION DIAGRAM



PACKAGE OUTLINE DIMENSIONS

DFN8

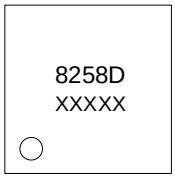


TOP VIEW SIDE VIEW BOTTOM VIEW

Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.20	0.25	0.30
D	2 BSC		
E	2 BSC		
e	0.5 BSC		
L	0.25	0.30	0.35
D2	0.80	0.90	1.00
E2	1.50	1.60	1.70
K	0.15	0.25	0.35
aaa	0.1		
ccc	0.1		
eee	0.05		
bbb	0.1		

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: 8258D

Product Code: XXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS8258D	DFN8	3000	10	30000	4	120000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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