Single-channel, High-speed, Low-side Gate Driver

FEATURES

- Low-cost Gate Driver Device, Providing High-quality Alternative Products of NPN and PNP Discrete Resolution
- 4A Peak Source Current and Peak Sink Current Symmetrical Drive
- Low Propagation Delay: 13ns (TYP)
- Fast Rising and Falling Time: 9ns and 7ns (TYP)
- TTL and CMOS Compatible Logic Threshold (Not Related to Power Supply)
- Dual Input Design (An Inverting (IN- Pin) or Non-inverting (IN+ Pin) Driver Configuration)
- Operating Temperature: -40°C to 125°C
- SOT23-5 Package

PRODUCT DESCRIPTION

The MS30517SA is a single-channel, high-speed and low-side gate driver device, which can drive MOSFET and IGBT switch effectively. The chip is designed to reduce shoot-through current to a great extent. The MS30517SA can provide high peak source and sink current pulses, offering rail-to-rail driving capability and low propagation delay (13ns TYP). The MS30517SA can withstand -5V input.

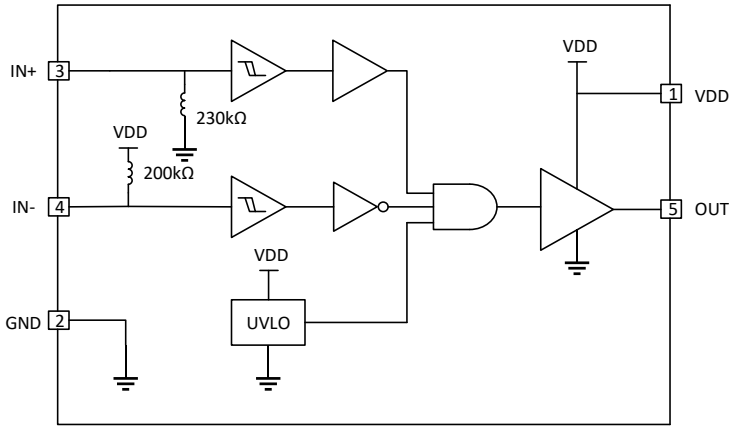
APPLICATIONS

- Switch-mode Power Supply
- DC-to-DC Converter
- Companion Gate Driver for Digital Power Supply Controller
- Solar Power, Motor Control, Uninterruptible Power Supply (UPS)
- Gate Driver with Wide Band-gap Power Device (Such as GaN)

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS30517SA	SOT23-5	30517

BLOCK DIAGRAM



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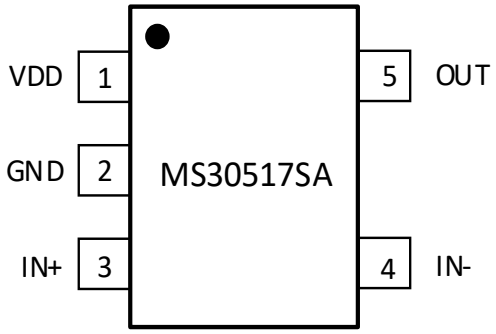
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	VDD	I	Power Supply Input
2	GND	-	Ground
3	IN+	I	Non-inverting Input. Operating in the non-inverting configuration, the PWM control signal can be applied to the pin. Operating in the inverting configuration, IN+ is connected to VDD to enable output. If IN+ is connected in low-level or floating, OUT keeps low.
4	IN-	I	Inverting Input. Operating in the inverting configuration, the PWM control signal can be applied to the pin. Operating in the non-inverting configuration, IN- is connected to GND to enable output. If IN- is connected in high-level or floating, OUT keeps low.
5	OUT	O	Source/Sink Current Output

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter		Symbol	Range	Unit
Power Supply		V_{DD}	-0.3 ~ +20	V
Output Voltage	DC		-0.3 ~ V_{DD} + 0.3	V
	Repetitive Pulses less than 200ns		-2 ~ V_{DD} + 0.3	V
Output Continuous Current		I_{OUT_DC} (Source/Sink)	0.3	A
Output Pulse Current(0.5s)		I_{OUT_pulsed} (Source/Sink)	4	A
Input Voltage[1]		IN+, IN-	-5 ~ + 20	V
Junction Temperature		T_J	-40 ~ +150	°C
Storage Temperature		T_{STG}	-65 ~ +150	°C

Note 1: The maximum voltage on the input pin is not limited by the voltage on the VDD pin.

RECOMMENDED OPERATING CONGITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{DD}	4.5	12	18	V
Logic Inputs	IN+, IN-	0		18	V
Operating Temperature	T_A	-40		125	°C

ELECTRICAL CHARACTERISTICS

VDD = 12V, T_A =-40°C~125°C, 1μF capacitor is connected to VDD and GND.

Note: unless otherwise noted, T_A = 25°C ±2°C.

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Power Supply Current							
Start-up Current	$I_{DD(OFF)}$	VDD = 3.4V	IN+= V_{DD}, IN- = GND		70		μA
			IN+ = IN-= GND or IN+= IN-= V_{DD}		60		
			IN+ = GND, IN-= V_{DD}		50		
Undervoltage Protection (UVLO)							
Power Supply Start-up Threshold	V_{ON}	T_A = 25°C			4.20	4.5	V
		T_A = -40°C ~125°C			4.20		
The Minimum Operating Voltage after Powering up	V_{OFF}				3.9		V
Power Supply Hysteresis	V_{DD_H}				0.3		V
Inputs (IN+, IN-)							
Input Signal High-level Threshold	V_{IN_H}	High-level Output on the IN+ Pin, Low-level Output on the IN- Pin			2.2	2.4	V
Input Signal Low-level Threshold	V_{IN_L}	Low-level Output on the IN+ Pin, High-level Output on the IN- Pin		1	1.3		V
Input Signal Hysteresis	V_{IN_HYS}				0.9		V
Source/Sink Current							
Source, Sink Peak Current[1]	$I_{SRC/SNK}$	C_{LOAD} = 0.22μF, f_{SW} = 1 kHz			±4		A
Output (OUT)							
High Output Voltage	V_{OH}	V_{DD} = 12V, I_{OUT} = -10mA			50		mV
		V_{DD} = 4.5V, I_{OUT} = -10mA			60		
Low Output Voltage	V_{OL}	V_{DD} = 12V, I_{OUT} = 10mA			5		mV
		V_{DD} = 4.5V, I_{OUT} = 10mA			6		
Output Pull-up Resistor[2]	R_{OH}	V_{DD} = 12V, I_{OUT} = -10mA			5		Ω
		V_{DD} = 4.5V, I_{OUT} = -10mA			5		
Output Pull-down Resistor	R_{OL}	V_{DD} = 12V, I_{OUT} = 10mA			0.5		Ω
		V_{DD} = 4.5V, I_{OUT} = 10mA			0.6		

Note: 1. It can be ensured by design.

2. R_{OH} is the on-resistance of the P-channel MOSFET in the pull-up structure of the MS30517SA output stage.

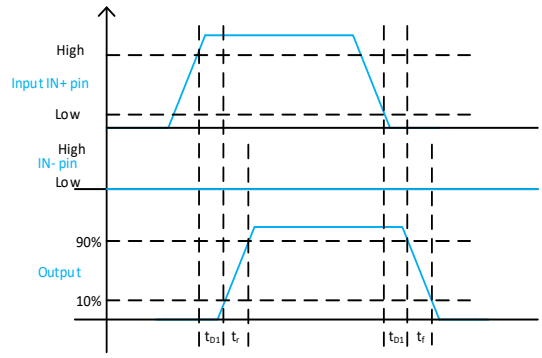
Switch Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Switching Time						
Rising Time	t_R	V_{DD} = 12V, C_{LOAD} = 1.8nF		8		ns
		V_{DD} = 4.5V, C_{LOAD} = 1.8nF		16		
Falling Time	t_F	V_{DD} = 12V, C_{LOAD} = 1.8nF		7		ns
		V_{DD} = 4.5V, C_{LOAD} = 1.8nF		7		
Propagation Delay from IN+ to Output	t_{D1}	V_{DD} = 12V, C_{LOAD} = 1.8nF 5V Input Pulse		13		ns
		V_{DD} = 4.5V, C_{LOAD} = 1.8nF 5V Input Pulse		15		
Propagation Delay from IN- to Output	t_{D2}	V_{DD} = 12V, C_{LOAD} = 1.8nF		13		ns
		V_{DD} = 4.5V, C_{LOAD} = 1.8nF		19		

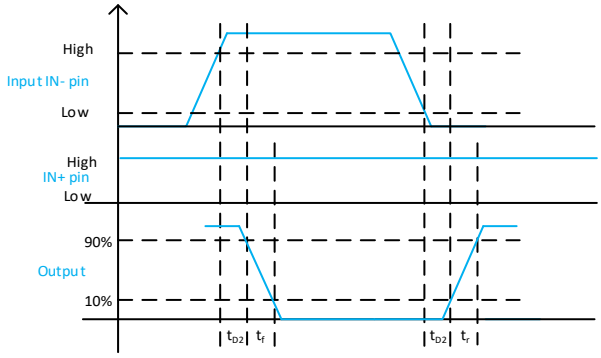
Timing

Non-inverting Function: PWM input is connected to the IN+ pin (IN- is connected to GND).

Inverting Function: PWM input is connected to the IN- pin (IN+ is connected to VDD).



Non-inverting Function

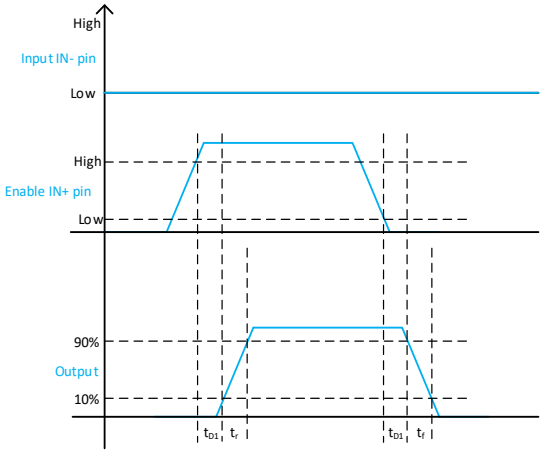


Inverting Function

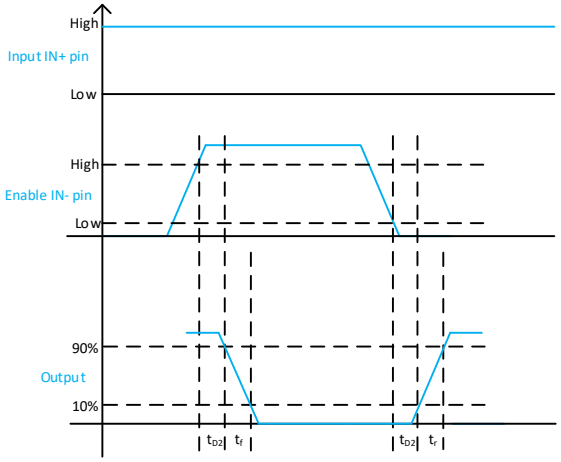
Enabling and Disabling Function

Enabling and disabling signal is applied to IN+ pin (PWM input is connected to IN- pin).

Enabling and disabling signal is applied to IN- pin (PWM input is connected to IN+ pin).



PWM Input Connected to IN+ Pin



PWM Input Connected to IN- Pin

FUNCTION DESCRIPTION

Overview

The MS30517SA is a single-channel, high-speed, low-side driver, which can drive MOSFET and IGBT switches effectively. The chip is designed to reduce shoot-through current to a great extent. The MS30517SA can provide high-peak source and sink current pulses, offering rail-to-rail driving capability and low propagation delay (13ns TYP).

The MS30517SA can provide 4A-peak source/sink (symmetrical drive) current driving capability and can be operated in power supply ranging from 4.5V to 18V and temperature ranging from -40°C to 125°C. The internal under voltage lock out (UVLO) circuit on the VDD pin can keep the output in low level when VDD is less than undervoltage. The device can be operated in low voltage (such as below 5V) and has the best switching characteristics among similar products, so it is very suitable for driving wide band-gap power-switching devices like GaN power-semiconductor devices.

The MS30517SA adopts dual-input design and can realize inverting (IN- pin) and non-inverting (IN+ pin) by using the same device. IN+ or IN- pin is used for controlling the output state of driver. Unused input pins are used for enabling and disabling functions. For protection, when the input pins are in floating state, the internal pull-up and pull-down resistors on the input pin keep the output in low level. So, the unused input pins cannot be in floating state. It must be appropriately biased to make the driver output enabling operated in normal state.

The MS30517SA input pin threshold is based on TTL and CMOS compatible low-voltage logic. The logic is fixed, and it is not related to VDD. The wide hysteresis between high and low threshold provides excellent noise immunity.

The MS30517SA Characteristics and Benefits

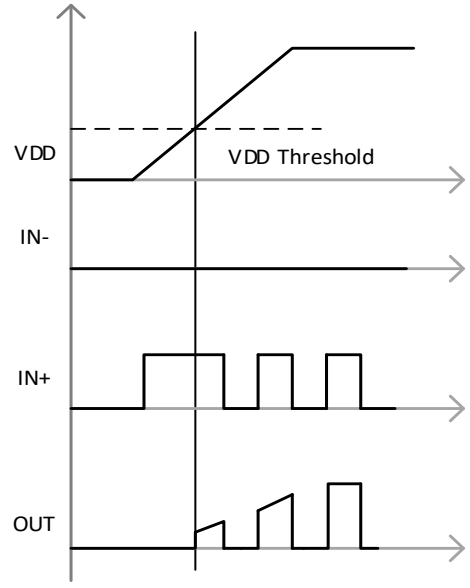
Characteristics	Benefits
High Current Driving Capability (Source/Sink Current (Symmetrical Drive) up to 4A)	High Current Driving Capacity, the MS30517SA can be Used Flexibly to Drive Different Kinds of Switching Devices
Best Propagation Delay among Similar Products (13ns TYP)	Ultra-low Pulse Transmission Distortion
VDD Operating Voltage, Expanded from 4.5 V to 18 V	System Design Flexibility VDD is Compatible with Wide Band-gap Power Devices like GaN under Low Voltage.
Operating Temperature Ranging from -40°C to 125°C	
VDD UVLO Protection	In UVLO Condition, the Output Keeps in Low Level, Ensuring Glitch-free Operation When Powering up and Powering down
When the Input Pins (INx) are in Floating State, the Output Keeps Low.	Protection Function

Characteristics	Benefits
The Ability of Input Pins Handling Voltage Levels is not Restricted by Bias Voltage on the VDD Pin	System Simplification, especially for Simplification related to Auxiliary Bias Power Supply Architecture
TTL and CMOS Compatible Logic Threshold	Enhanced Noise Tolerance Capability, Compatible with Logic Level Input Signal (3.3V, 5V)
Handle -5V DC Voltage on the Input Pins	Improve Stability in Noise

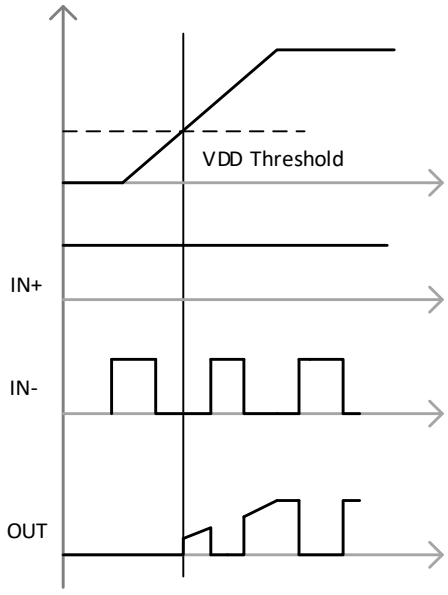
VDD and UVLO

The MS30517SA has internal under voltage lock out (UVLO) protection function. When the driver is in UVLO, the circuit will keep all outputs in low level regardless of the input state. The device can operate under low voltage (such as below 5V) and has the best switching characteristics among similar products. So, it is very suitable for driving wide band-gap power-switch devices like GaN power-semiconductor devices.

Because the current is drawn from the VDD pin by the driver to bias all internal circuits. To realize the best high-speed circuit characteristics, it is recommended to use two V_{DD} bypass capacitors to prevent noise issues. Using the surface mount components is also recommended. A 4.7μF ceramic capacitor is placed as close as possible to VDD to GND pins of the MS30517SA. In addition, a capacitor with the relatively low ESR (such as 1μF) should be connected in parallel and closely to provide the needed high current peak for load, reaching current levels and switching frequencies. The parallel combination of capacitors should present low-resistance characteristics.



Power up (Non-inverting Drive)



Power up (Inverting Drive)

Operating Supply Current

The MS30517SA is featured with ultra-low static I_{DD} current. The typical operating supply current is the I_{DD} current in under voltage lock out (UVLO) state and fully-on (under static and switching conditions) state. The device fully starts up and outputs I_{DD} current in static state, which represents the lowest static I_{DD} current when all the internal logic circuits are fully operated. The total supply current is the sum of averaged I_{OUT} current as well as any current related to pull-up resistors on the unused input pins caused by static I_{DD} current and switches. For example, when the inverting input pin is pulled low, the extra current is drawn from VDD by pull-up resistors (refer to block diagram). Given that operating frequency (f_{SW}) and MOSFET gate (Q_G) charge under used driving voltage, the averaged I_{OUT} current can be calculated as product of Q_G and f_{SW}.

Input Stage

The MS30517SA input pins are based on TTL and CMOS compatible input threshold logic, independent of VDD. The logic level setting can be compatible with 3.3V and 5V simultaneously. Compared to the traditional TTL logic scheme, the wider hysteresis can provide stronger noise immunity.

The MS30517SA is featured with important protection function. Once any input pins are floating, the output of corresponding channel will keep in low level, which is realized by using VDD pull-up resistors on all inverting input pin (IN- pin) or using GND pull-down resistor on all non-inverting input pin (IN+ pin).

The MS30517SA is also featured with dual input configuration, dual input pins can be used to control output state. The state of output pins is determined by the bias on the IN+ and IN- pins. Please refer to the truth table and typical application.

Once one input pin is selected for PWM driving, the other input pin (unused input pin) must be appropriately biased to enable output. As mentioned above, unused pin cannot keep floating. Because as long as any input pins are in floating state, output will be disabled for protection. Or unused input pins can be used for enabling/disabling function effectively.

Enabling Function

Using unused input pins, the MS30517SA can achieve enabling or disabling function. When IN+ is pulled low to GND or IN– is pulled high to VDD, the output is disabled. So, IN+ connected to high level can enable the logic pins, but IN– connected to low level can enable logic pins.

Output Stage

When VDD is 12V, the MS30517SA provides 4A-peak source/sink (symmetrical drive) current driving capability. The MS30517SA output stage adopts mixed pull-up structure, arranging N-channel and P-channel MOSFET in parallel. When the output changes from low level to high level, the MS30517SA enables N-channel MOSFET within short time, thus the peak current can be improved temporarily to make quick response.

Low Propagation Delay

When VDD is 12V, the MS30517SA has the best propagation delay from input to output (13ns TYP). In high-frequency switching applications, it is the lowest pulse transmitting distortion in industry standard gate drivers.

Function Modes

In normal mode, the output state depends on the state of IN+ and IN- pins. The different combinations of pins are as follows:

Truth Table

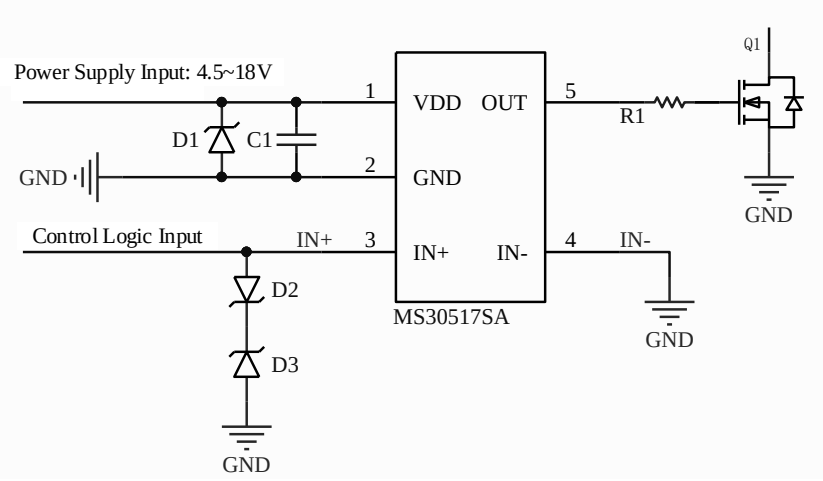
IN+ Pin	IN- Pin	Output Pin
L	L	L
L	H	L
H	L	H
H	H	L
Floating	Any	L
Any	Floating	L

TYPICAL APPLICATION

The MS30517SA power supply ranges from 4.5V to 18V. in applications, it is necessary to connect an ESD electrostatic discharge device in parallel at the power supply VDD end, the clamp voltage of this device is from 18V to 24V. To prevent interference, the power supply VDD should be connected to bypass capacitor C1. The capacitor should be placed as close as possible to the VDD pin. The ceramic capacitor is recommended, and the capacitance should be 4.7μF (the capacitance shall not be less than 2.2μF).

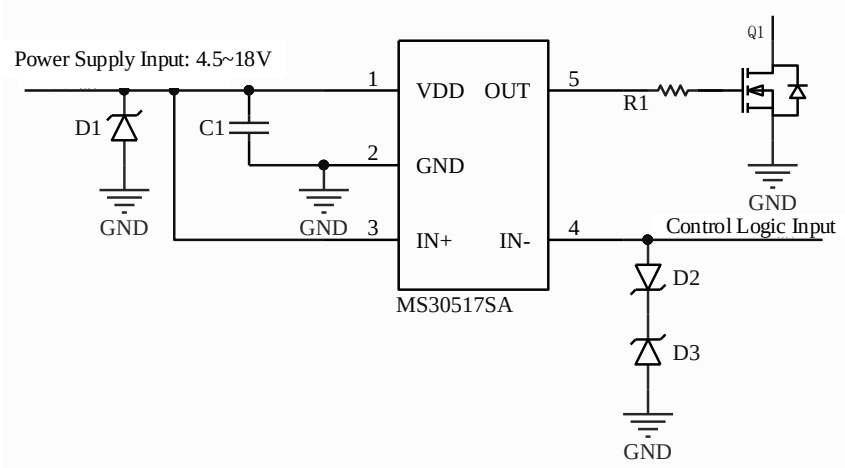
The control logic end and an ESD electrostatic discharge device should be connected in parallel, D2 clamp voltage should be less than 6V, D3 clamp voltage should be greater than the control input voltage, less than or equal to 18V (V_{IN}<D3 clamp voltage ≤18V).

Non-inverting Input



Using Non-inverting Input (IN- Grounded as an Enabling Pin)

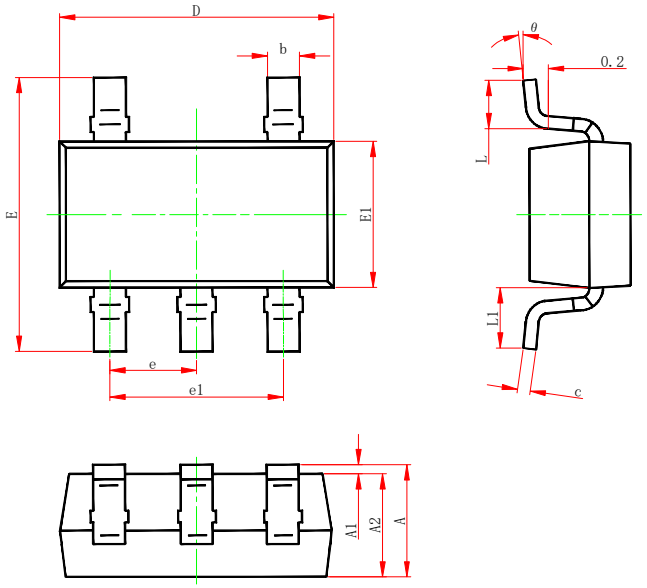
Inverting Input



Using inverting Input (IN+ Connected to VDD as an Enabling Pin)

PACKAGE OUTLINE DIMENSIONS

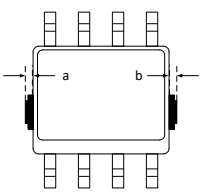
SOT23-5



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF		0.024REF	
θ	0°	8°	0°	8°

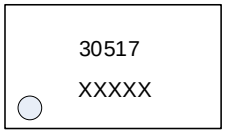
Note: In addition to the package size, a and b are allowed to have the maximum size of 0.15mm for waste glue simultaneously.

The diagram is as follows: taking SOP8 package as an example.



MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: 30517

Product Code: XXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS30517SA	SOT23-5	3000	10	30000	4	120000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com