

16-bit ADC with Input Multiplexer and Onboard Reference

FEATURES

- Small Outline Package
- Two Differential, Three Single-ended Input Channels
- I²C Interface, Eight Programmable Addresses
- Onboard Reference: 2.048V±0.05%
- Temperature Drift: 40ppm/°C (Max)
- Onboard PGA: One to Eight
- Onboard OSC
- 16Bit No Missing Codes
- INL (Integral Nonlinearity): 0.01%
- Single Conversion Function
- Programmable Output Rate: 15SPS to 240SPS
- Operating Voltage: 2.7V to 5.5V
- Low Power Dissipation: 290μA@5V

PRODUCT DESCRIPTION

The MS5112M is a 16bit high-precision ADC with two differential or three single-ended input channels, up to 16 bits resolution. The on-board reference provides differential input range of ±2.048V. The MS5112M uses an I²C compatible interface and has two address pins, allowing user to select eight I²C slave addresses. The power supply range is from 2.7V to 5.5V.

The MS5112M can perform conversions at rates of 15, 30, 60 or 240 samples per second (SPS). It integrates programmable gain amplifier (PGA), which can provide the gain up to 8. In single conversion mode, the MS5112M automatically enters into power-down state after conversion, greatly reducing power dissipation.

The MS5112M is designed for applications requiring high-resolution measurement and where space and power dissipation are major considerations, such as portable instrument, industry control and smart transmitter.

APPLICATIONS

- Portable Instrument
- Industry Control
- Smart Transmitter
- Factory Automation
- Temperature Measurement

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5112M	MSOP10	MS5112M

BLOCK DIAGRAM

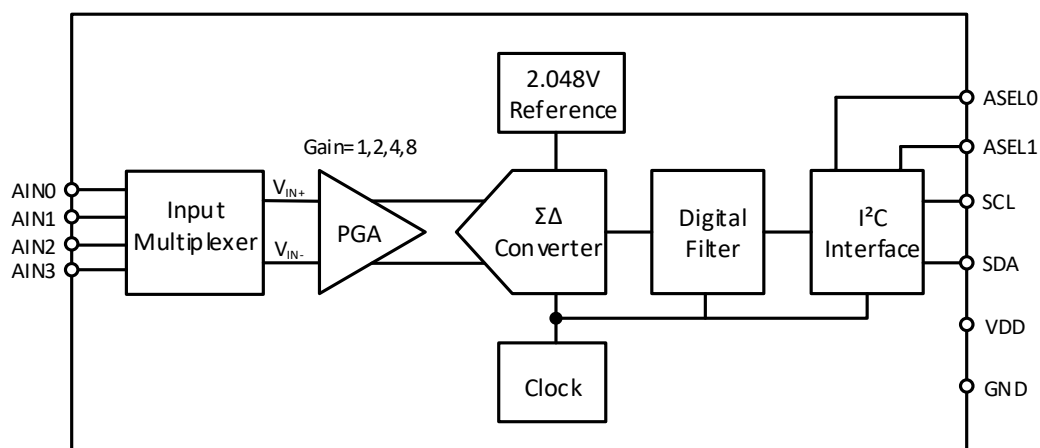
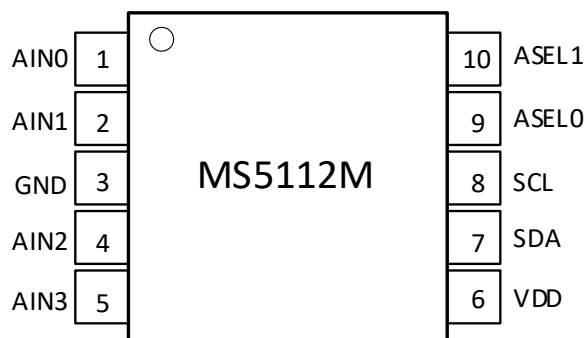


TABLE of CONTENTS

1. FEATURES.....	1
2. PRODUCT DESCRIPTION.....	1
3. APPLICATIONS.....	1
4. PRODUCT SPECIFICATION	1
5. BLOCK DIAGRAM	1
6. TABLE of CONTENTS	2
7. PIN CONFIGURATION	3
8. PIN DESCRIPTION	3
9. ABSOLUTE MAXIMUM RATINGS	4
10. RECOMMENDED OPERATING CONDITIONS.....	4
11. ELECTRICAL CHARACTERISTICS	5
12. FUNCTION DESCRIPTION	7
12.1 Analog-to-Digital Converter	7
12.2 Input Multiplexer	7
12.3 Voltage Reference	7
12.4 Output Code Calculation.....	7
12.5 Clock Oscillator	8
12.6 Input Impedance.....	8
12.7 Aliasing.....	8
12.8 Operation Mode	8
12.9 Reset and Power-up	8
12.10 I ² C Interface	9
12.10.1 Serial Bus Address.....	9
12.10.2 I ² C General Call	10
12.10.3 I ² C Data Rate	10
12.11 Result Register	10
12.12 Configuration Register	10
12.13 Reading from the MS5112M	12
12.14 Writing to the MS5112M	13
13. TYPICAL APPLICATION DIAGRAM.....	14
13.1 Basic Connection.....	14
13.2 Connecting Multiple Devices	14
13.3 Low-Side Current Monitor	15
14. PACKAGE OUTLINE DIMENSIONS.....	16
15. MARKING and PACKAGING SPECIFICATION.....	17
16. STATEMENT	18
17. MOS CIRCUIT OPERATION PRECAUTIONS	19

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	AIN0	I	Differential Input Channel 1, Positive Input/Single-ended Input 1
2	AIN1	I	Differential Input Channel 1, Negative Input/Single-ended Input 2
3	GND	-	Ground
4	AIN2	I	Differential Input Channel 2, Positive Input/Single-ended Input 3
5	AIN3	I	Differential Input Channel 2, Negative Input/Single-ended Common Input
6	VDD	-	Power Supply
7	SDA	I/O	Serial Data
8	SCL	I	Serial Clock
9	ASEL0	I	I ² C Salve Address Selection 1
10	ASEL1	I	I ² C Salve Address Selection 2

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	V_{DD}	-0.3 ~ 6	V
Input Current	I_{IN}	100mA, Momentary	mA
		10mA, Continuous	
Analog Input (ASEL0, ASEL1 to GND)	V_{IN}	-0.3 ~ $V_{DD}+0.3$	V
SDA, SCL Voltage to GND	V	-0.5 ~ 6	V
Maximum Junction Temperature	T_{JMAX}	150	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C
Lead Temperature(10s)	T	260	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Temperature	T_A	$V_{DD}=2.7V$ to 5.5V	-40		125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, $V_{DD}=5V$.

Parameter	Condition	Min	Typ	Max	Unit
Analog Input					
Full-scale Input Voltage	$(V_{IN+})-(V_{IN-})$		$\pm 2.048/PGA$		V
Analog Input Voltage	V_{IN+} to GND, V_{IN-} to GND	GND-0.2		$V_{DD}+0.2$	V
Differential Input Impedance			$2.8/PGA$		MΩ
Common-mode Input Impedance	PGA=1		3.5		MΩ
	PGA=2		3.5		MΩ
	PGA=4		1.8		MΩ
	PGA=8		0.9		MΩ
System Performance					
Resolution and No Missing Codes	DR=00	12		12	Bits
	DR=01	14		14	Bits
	DR=10	15		15	Bits
	DR=11	16		16	Bits
Output Rate	DR=00	180	240	308	SPS
	DR=01	45	60	77	SPS
	DR=10	22	30	39	SPS
	DR=11	11	15	20	SPS
Integral Nonlinearity	DR=11, PGA=1, End Point ¹		± 0.004	± 0.010	% of FSR ²
Offset Error	PGA=1		1	3	mV
	PGA=2		1	3	mV
	PGA=4		1	3	mV
	PGA=8		1	3	mV
Offset Temperature Drift	PGA=1		1.2		$\mu V/^{\circ}C$
	PGA=2		0.6		$\mu V/^{\circ}C$
	PGA=4		0.3		$\mu V/^{\circ}C$
	PGA=8		0.3		$\mu V/^{\circ}C$
Offset VS. VDD	PGA=1		800		$\mu V/V$
	PGA=2		400		$\mu V/V$
	PGA=4		200		$\mu V/V$
	PGA=8		150		$\mu V/V$

Parameter	Condition	Min	Typ	Max	Unit
System Performance					
Gain Error			0.05	0.4	%
PGA Gain Match Error ³	Any two gains match		0.02	0.1	%
Gain Error Temperature Drift				40	ppm/°C
Gain VS. VDD			80		ppm/V
Common-mode Rejection Ratio	DC Input, PGA=8	95	105		dB
	DC Input, PGA=1		100		dB
Digital Input/Output					
Input High-level Voltage		$0.7 \times V_{DD}$		$V_{DD} + 0.5$	V
Input Low-level Voltage		GND-0.5		$0.3 \times V_{DD}$	V
Output Low-level Voltage	$I_{OL} = 3mA$	GND		0.4	V
Input High-level Peak Current				10	μA
Input Low-level Peak Current		-10			μA
Power Supply					
Operating Voltage	VDD	2.7		5.5	V
Power Supply Current	Power down		0.05	2	μA
	Operation		290	350	μA
Power Dissipation	$V_{DD} = 5.0V$		1.45	1.75	mW
	$V_{DD} = 3.0V$		0.87		mW

Note:

1. 99% of full-scale.
2. $FSR = \text{Full-scale Range} = 2 \times 2.048V/PGA = 4.096V/PGA$.
3. Includes all errors from PGA and reference.

FUNCTION DESCRIPTION

The MS5112M is a 16bit, differential, Σ - Δ ADC. It has easy design and configuration, so users can easily achieve accurate measurement values.

The MS5112M consists of a Σ - Δ A/D converter with adjustable gain, a 2.048V voltage reference, a clock oscillator, a digital filter and an I²C interface. Each of these blocks are described in detail as follows.

Analog-to-Digital Converter

The A/D converter core consists of a differential switched-capacitor Σ - Δ modulator and a digital filter. The modulator measures the voltage difference between the positive and negative analog inputs and compares it with reference voltage, which is 2.048V in the MS5112M. The digital filter receives high-speed bitstream from the modulator and outputs digital signal, which is proportional to the input voltage.

Input Multiplexer

The MS5112M has an input multiplexer, which provides two differential and three single-ended input channels. Configuration register controls the setting of input multiplexer.

Voltage Reference

The MS5112M has a 2.048V onboard voltage reference without need for external reference.

Output Code Calculation

The number of bits for the MS5112M depends on update rate, as shown in Table 1.

Table 1. Minimum and Maximum Code

Update Rate	Number Of Bits	Minimum Code	Maximum Code
15SPS	16	-32768	32767
30SPS	15	-16384	16383
60SPS	14	-8192	8191
240SPS	12	-2048	2047

The output code of the MS5112M is in binary two's complement format, right-justified and sign-extended.

Table 2 shows the output codes for various input levels.

Table 2. Output Codes for Different Input Signals

Update Rate	Differential Input Signal				
	-2.048V ¹	-1LSB	0 (Ideal)	+1LSB	+2.048V
15SPS	8000 _H	FFFF _H	0000 _H	0001 _H	7FFF _H
30SPS	C000 _H	FFFF _H	0000 _H	0001 _H	3FFF _H
60SPS	E000 _H	FFFF _H	0000 _H	0001 _H	1FFF _H
240SPS	F800 _H	FFFF _H	0000 _H	0001 _H	07FF _H

Note 1: Differential input; do not drive the MS5112M absolute input voltage below -200mV.

The output code is given by the expression:

$$\text{Output Code} = -1 \times \text{Minimum Code} \times \text{PGA} \times \frac{(V_{\text{IN}+}) - (V_{\text{IN}-})}{2.048\text{V}} \dots\dots\dots (V_{\text{IN}+} < V_{\text{IN}-})$$

$$\text{Output Code} = 1 \times \text{Maximum Code} \times \text{PGA} \times \frac{(V_{\text{IN}+}) - (V_{\text{IN}-})}{2.048\text{V}} \dots\dots\dots (V_{\text{IN}+} \geq V_{\text{IN}-})$$

The maximum code is $2^{n-1}-1$, while the minimum code is $-1 \times 2^{n-1}$.

Clock Oscillator

The MS5112M features an onboard clock oscillator, which drives the modulator and digital filter without need for external clock.

Input Impedance

The input stage of the MS5112M uses switched-capacitor. The equivalent resistance value depends on the capacitor value and switching frequency. The capacitor value depends on the PGA setting. The clock is generated by the onboard clock oscillator. The typical operating frequency is 275kHz.

The common-mode and differential input impedance are different. Details see in “Electrical Characteristics”.

For input source with high output impedance, buffer is necessary externally on input terminal.

Aliasing

If the input signal frequency of the MS5112M exceeds half of the update rate, aliasing will occur. To prevent aliasing, the input signal must be band-limited. The digital filter of the MS5112M provides some attenuation of high-frequency noise to some extent, but sinc filter cannot completely replace an anti-aliasing filter. For a few applications, external filtering is also needed.

When designing input filter, remember to take into account the impedance match between the filter and the MS5112M input.

Operation Mode

The MS5112M has two conversion modes: continuous conversion and single conversion.

In continuous conversion mode, after a conversion has been completed, the MS5112M places the result in the result register and immediately begins another conversion.

In single conversion mode, the MS5112M will wait until the $\overline{\text{ST/DRDY}}$ bit in the configuration register is set to 1. Then the MS5112M starts a conversion. After the conversion is completed, the MS5112M places the result in the result register, resets the $\overline{\text{ST/DRDY}}$ bit to 0 and powers down.

When switched from continuous conversion mode to single conversion mode, the MS5112M completes the current conversion, resets the $\overline{\text{ST/DRDY}}$ bit to 0 and powers down.

Reset and Power-up

When the MS5112M powers up, it automatically performs one reset. All of the bits in the configuration register are set to default values.

The MS5112M responds to the I²C General Call Reset command. When the MS5112M receives a General Call Reset, it performs a reset immediately.

I²C Interface

The MS5112M communicates through I²C interface. A timing diagram is shown in Figure 1. The related parameters for this diagram are given in Table 3.

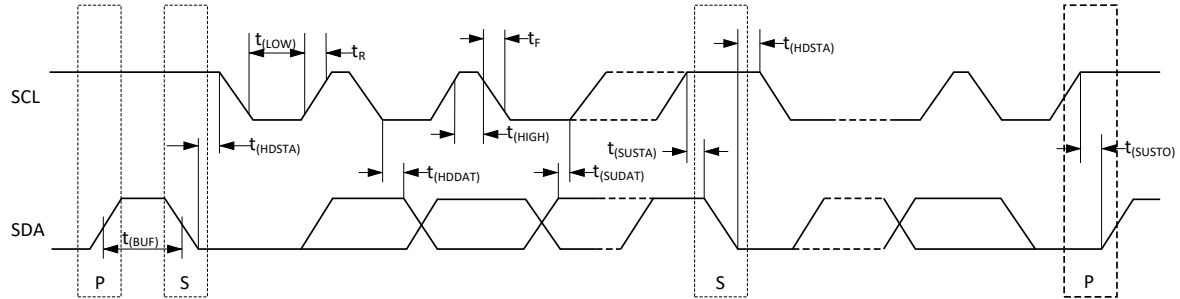


Figure 1. I²C Timing Diagram

Table 3. Related Parameters for Timing Diagram

Parameter	Symbol	Fast-Speed Mode		High-Speed Mode		Unit
		Min	Max	Min	Max	
SCLK Operating Frequency	$t_{(SCLK)}$		0.4		3.4	MHz
Bus START to STOP Idle Time	$t_{(BUF)}$	600		160		ns
START Hold Time	$t_{(HDSTA)}$	600		160		ns
Repeated START Setup Time	$t_{(SUSTA)}$	600		160		ns
STOP Setup Time	$t_{(SUSTO)}$	600		160		ns
Data Hold Time	$t_{(HDDAT)}$	0		0		ns
Data Setup Time	$t_{(SUDAT)}$	100		10		ns
SCLK Clock Low Level Period	$t_{(LOW)}$	1300		160		ns
SCLK Clock High Level Period	$t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time	t_F		300		160	ns
Clock/Data Rise Time	t_R		300		160	ns

Serial Bus Address

In order to read from and write to the MS5112M, the master must address to the slave according to address bit. The slave address bits include seven address bits and one operation bit.

The MS5112M has two address pins, ASELO and ASEL1, setting I²C address. The pin could be set as logic low, logic high or float. Eight different addresses can be set by the two pins, as shown in Table 4. After power-up reset or I²C General Call Reset command, ASELO and ASEL1 pin states are sampled.

Table 4. Address Pin and Slave Address

ASEL0	ASEL1	Slave Address
0	0	1001000
0	Float	1001001
0	1	1001010
1	0	1001100
1	Float	1001101
1	1	1001110
Float	0	1001011
Float	1	1001111
Float	Float	Invalid

I²C General Call

If the eight address is 0, the MS5112M would respond to general call. The device acknowledges and responds to the second byte command. If the command is 04h, the MS5112M would only latch the states of address pins ASEL0, ASEL1 and not reset configuration register. If the command is 06h, the MS5112M would latch the state of address pin and reset configuration register.

I²C Data Rate

I²C bus has three speed modes: standard mode, allowing the clock frequency up to 100kHz; fast-speed mode, allowing the clock frequency up to 400kHz; high-speed mode, allowing the clock frequency up to 3.4MHz.

About more information about high-speed mode, please refer to I²C specification.

Result Register

The 16bit result register contains the conversion result in binary two's complement format. After reset or power-up, the result register is cleared 0, and remains until the first conversion is completed. The format of result register is shown in Table 5.

Table 5. Result Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Configuration Register

The 8bit configuration register controls the operation mode, update rate and PGA. The format of configuration register is shown in Table 6. The default setting is 8C_H.

Table 6. Configuration Register

Bit	7	6	5	4	3	2	1	0
Name	ST/DRDY	INP1	INP0	SC	DR1	DR0	PGA1	PGA0
Default	1	0	0	0	1	1	0	0

Bit 7: ST/DRDY

The meaning of the ST/DRDYbit depends on whether it is being written to or read from.

In single conversion mode, writing 1 to the ST/DRDYbit indicates a conversion to start, and writing 0 has no effect. In continuous mode, the MS5112M ignores the value written to ST/DRDY.

In continuous conversion mode, ST/DRDYbit determines whether new conversion data is ready. If ST/DRDYis 1, the data in the result register has already been read. If it is 0, the data in the result register is new, and has not yet been read.

In single conversion mode, ST/DRDYbit determines whether a conversion has completed. If ST/DRDYis 1, the data in the result register is old, and the conversion is still in process. if it is 0, the data in the result register is the new conversion result.

The MS5112M first outputs the value of result register, then the value of configuration register. The state of the ST/DRDYbit applies to the data just read from the result register, rather than the data read from the next read operation.

Bit 6-5: INP

Input signal select bits. The MS5112M can select two differential channels or three single-ended input channels referenced to AIN3 by controlling these two bits, as shown in Table 7,

Table 7. INP Bit

INP1	INP0	VIN+	VIN-
0 ¹	0 ¹	AIN0	AIN1
0	1	AIN2	AIN3
1	0	AIN0	AIN3
1	1	AIN1	AIN3

Note 1: Default setting.

Bit 4: SC

Conversion mode select bit. When SC is 1, the MS5112M is in single conversion mode; when SC is 0, it is in continuous conversion mode. The default value is 0.

Bit 3-2: DR

Update rate select bits, as shown in Table 8.

Table 8. DR Bit

DR1	DR0	Update Rate	Resolution
0	0	240SPS	12Bit
0	1	60SPS	14Bit
1	0	30SPS	15Bit
1 ¹	1 ¹	15SPS	16Bit

Note 1: Default setting.

Bit 1-0: PGA

Gain setting select bits, as shown in Table 9.

Table 9. PGA Bit

PGA1	PGA0	Gain
0 ¹	0 ¹	1
0	1	2
1	0	4
1	1	8

Note 1: Default setting.

Reading from the MS5112M

Read the values in the result register and the configuration register. First address the MS5112M, then read three bytes from the device. The first two bytes are the result register's contents, and the third byte is the configuration register's contents.

It is not required to read the configuration register. It is permissible to read fewer than three bytes during a read operation. Reading more than three bytes from the MS5112M has no effect. All bytes from the fourth byte will be FF_H.

The timing diagram of typical read operation for the MS5112M is shown in Figure 2.

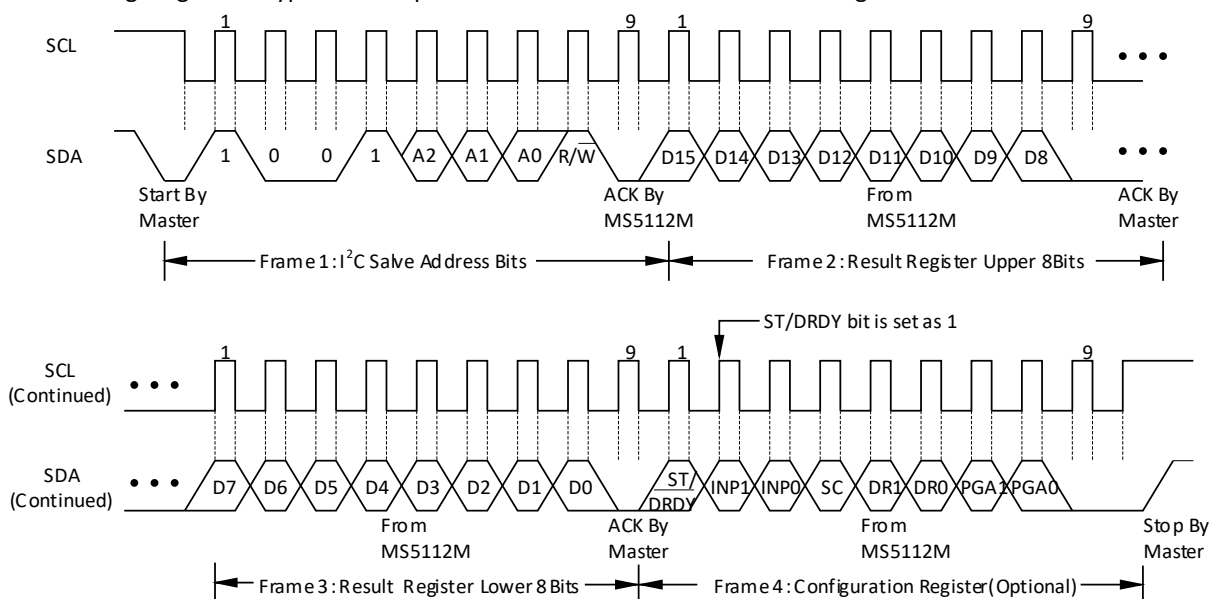


Figure 2. Timing Diagram of the MS5112M Read Operation

Writing to the MS5112M

Write to the configuration register. First address the MS5112M, then write to one byte. This byte will be written to the configuration register.

Writing more than one byte to the MS5112M has no effect. The MS5112M will ignore any byte after the first byte. The timing diagram of typical write operation for the MS5112M is shown in Figure 3.

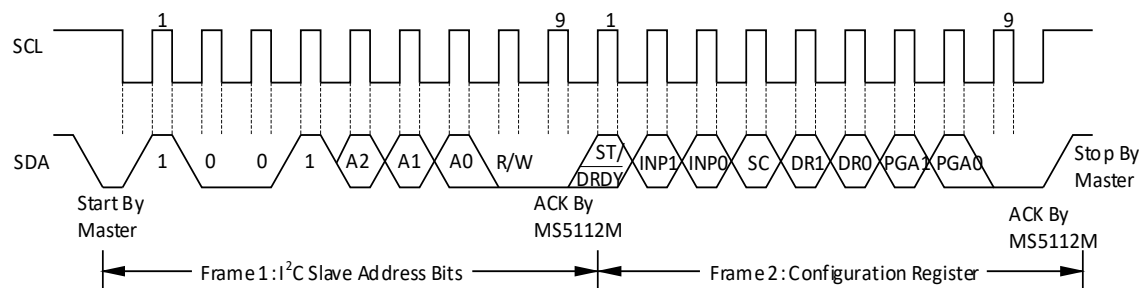


Figure 3. Timing Diagram of the MS5112M Write Operation

TYPICAL APPLICATION DIAGRAM

Basic Connection

For many applications, the basic connection diagram of the MS5112M is shown in Figure 4.

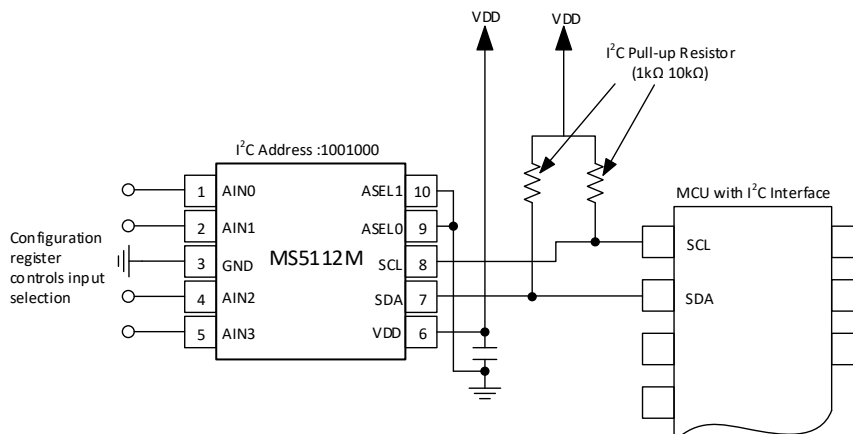


Figure 4. Typical Basic Connection of the MS5112M

Connecting Multiple Devices

Multiple MS5112Ms can be connected to a I²C bus. The MS5112M is available in different eight I²C addresses by ASEL1 and ASEL0 pins. An example showing three MS5112Ms connected on a same bus is shown in Figure 5. Up to eight MS5112Ms (controlled by differential states of ASEL1 and ASEL0 pins) can be connected to one I²C bus.

Note that I²C bus only needs one set of pull-up resistors.

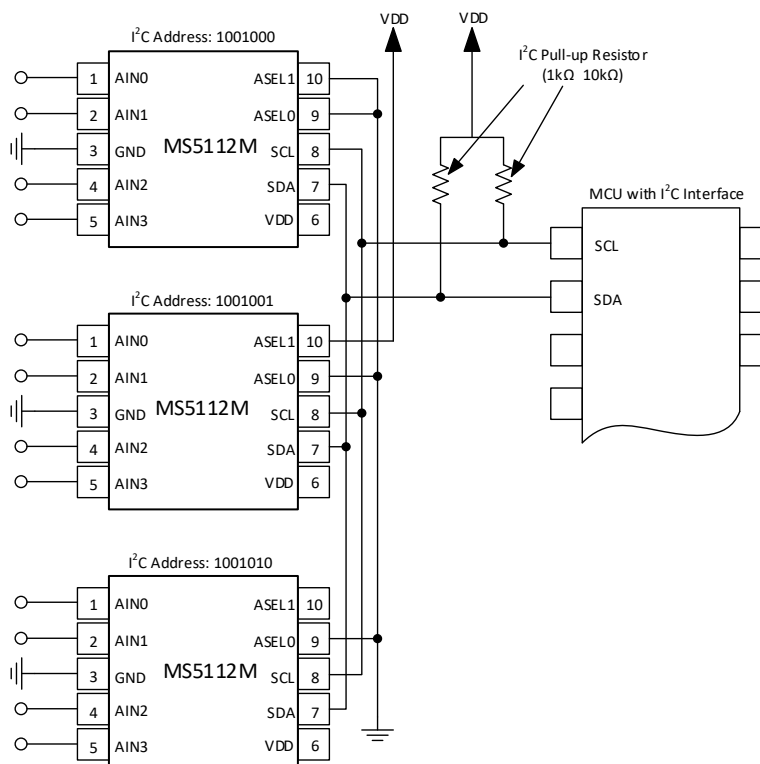


Figure 5. Connecting Multiple MS5112Ms

Low-Side Current Monitor

Figure 6 shows a circuit for low-side current monitor. The circuit reads the voltage across a shunt resistor, the voltage on which can be amplified by the MS8552, and the result is read by the MS5112M.

It is suggested that the MS5112M operate at a gain of 8. The gain of the MS8552 can be reduced. For a gain of 8, the op amp should provide output voltage of no greater than 0.256V. Therefore, the shunt resistor provides a maximum voltage drop of 64mV at full-scale current.

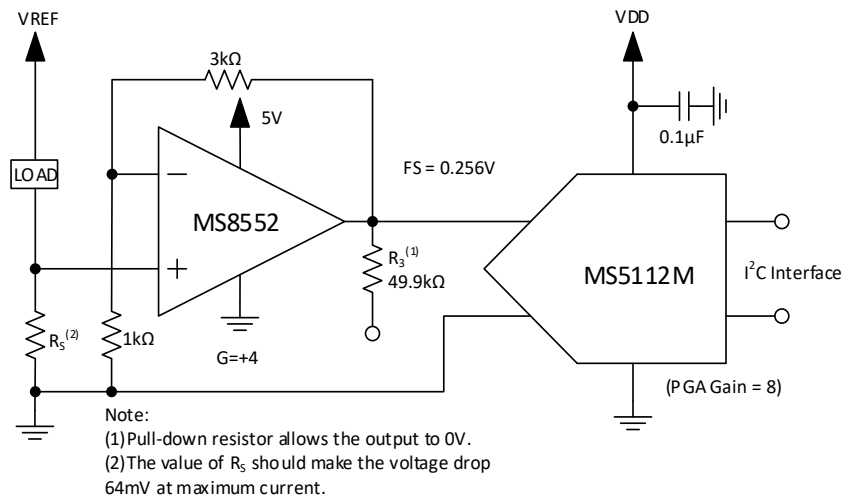
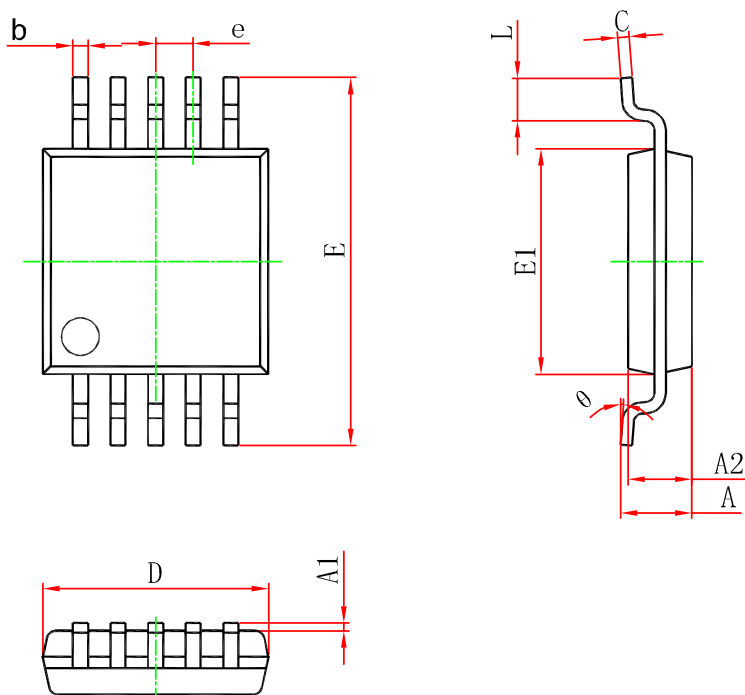


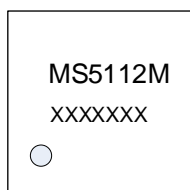
Figure 6. Low-side Current Measurement

PACKAGE OUTLINE DIMENSIONS

MSOP10



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	-	1.100	-	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.330	0.007	0.013
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50BSC		0.020BSC	
E	4.750	5.050	0.187	0.199
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

MARKING and PACKAGING SPECIFICATION**1. Marking Drawing Description**

Product Name: MS5112M

Product Code: XXXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5112M	MSOP10	3000	1	3000	8	24000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.
Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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