Low-Voltage, Multi-Channel Lens Driver IC (Built-in Iris Control)

FEATURES

- Voltage Drive Mode, 256 Microstep Drive Circuit: 5V Operating Voltage, ±0.4A Driving Current for Each H-bridge
- Four-line Serial Bus Communication Control Motor
- PID Iris Control for Hall Position Detection
- Four-Channel, High-Precision Stepper Motor Driver
- Two-Channel DC Motor Driver for IRCUT, also Combine for Fifth Channel Stepper Driver
- Four-Channel LED Driver
- QFN88 (10x10) Package

APPLICATIONS

- Camera
- Monitoring Camera

PRODUCT DESCRIPTION

The MS41968 is 5V low-voltage, multi-channel lens driver IC, which integrates iris driver for Hall mode, four-channel stepper motor driver, two-channel DC motor driver and four-channel LED driver. Ultra-low noise microstep could be realized by voltage driving method with current microstep and torque ripple correction technology.

The MS41968 integrates logic IO interface power supply VIO and can be applied to different voltage interfaces ranging from 1.2V to 3.6V.

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS41968	QFN88	MS41968

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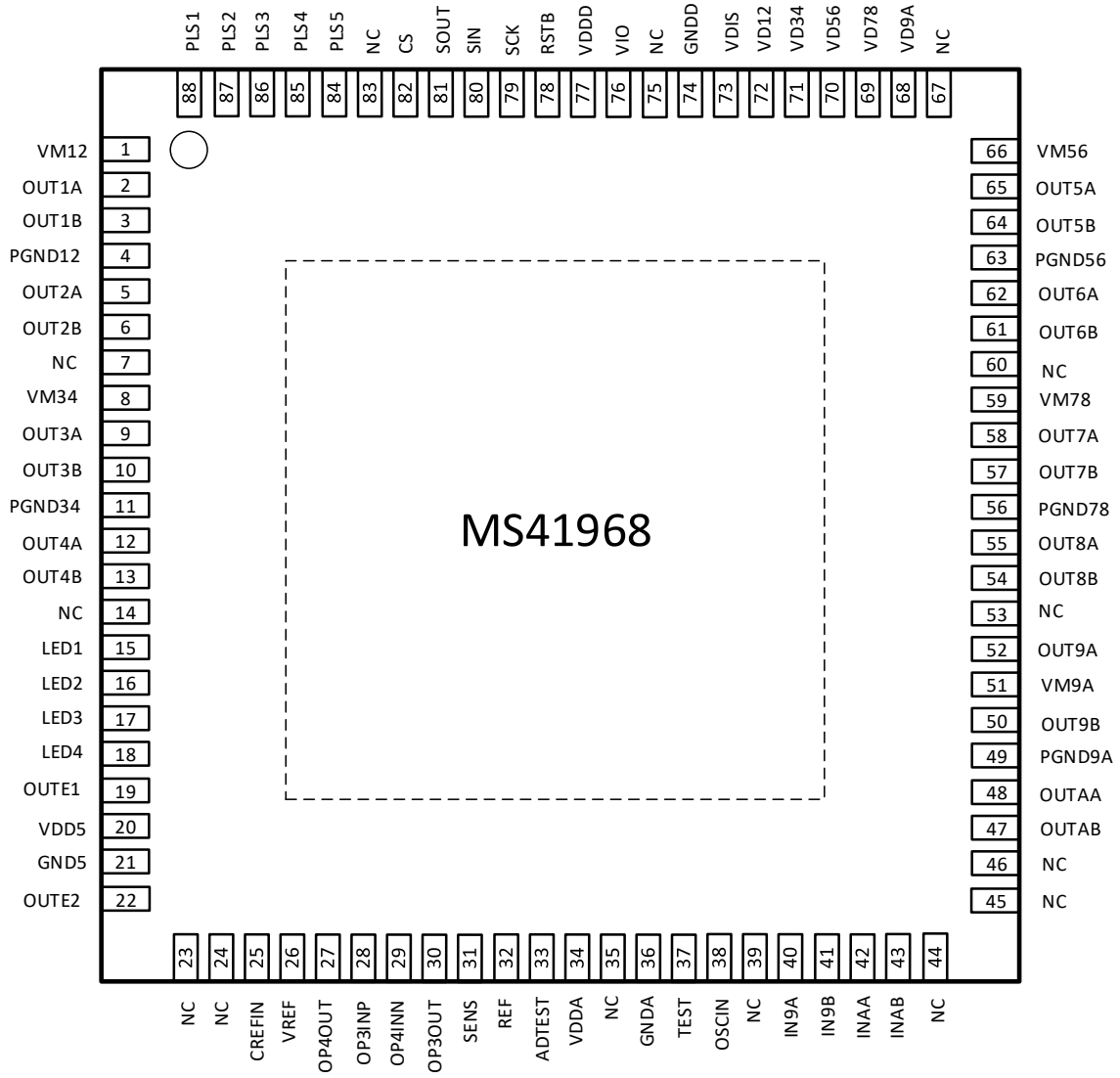
PIN CONFIGURATION



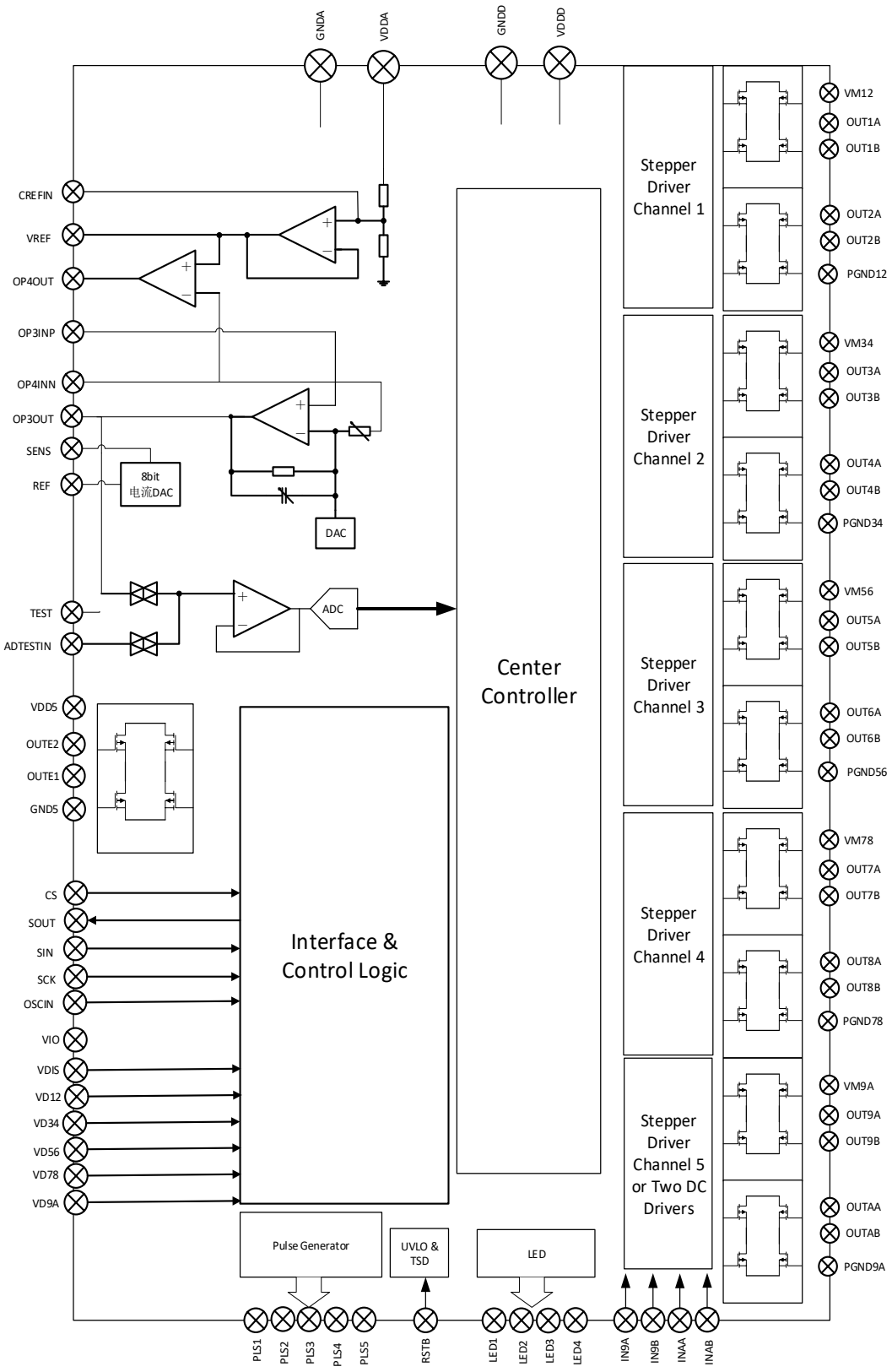
PIN DESCRIPTION

Pin	Name	Type	Description
1	VM12	-	Stepper H-bridge 1, 2 Power Supply
2	OUT1A	O	H-bridge 1, Output A
3	OUT1B	O	H-bridge 1, Output B
4	PGND12	-	Stepper 1, 2 Channel Ground
5	OUT2A	O	H-bridge 2, Output A
6	OUT2B	O	H-bridge 2, Output B
8	VM34	-	Stepper H-bridge 3, 4 Power Supply
9	OUT3A	O	H-bridge 3, Output A
10	OUT3B	O	H-bridge 3, Output B
11	PGND34	-	Stepper 3, 4 Channel Ground
12	OUT4A	O	H-bridge 4, Output A
13	OUT4B	O	H-bridge 4, Output B
15	LED1	O	LED1 Open-drain Output
16	LED2	O	LED2 Open-drain Output
17	LED3	O	LED3 Open-drain Output
18	LED4	O	LED4 Open-drain Output
19	OUTE1	O	Iris H-bridge, Output 1
20	VDD5	-	Iris Power Supply
21	GND5	-	Iris Power Ground
22	OUTE2	O	Iris H-bridge, Output 2
25	CREFIN	I	Regulation Capacitor Pin
26	VREF	O	Hall Reference Voltage
27	OP4OUT	O	Bias Amplifier Output
28	OP3INP	I	Hall Gain Amplifier input
29	OP4INN	I	Bias Amplifier Input
30	OP3OUT	O	Hall Gain Amplifier Output
31	SENS	O	Hall Bias Output
32	REF	-	Hall Current Bias Setting
33	ADTEST	I	ADC Test Input
34	VDDA	-	5V Analog Power Supply

Pin	Name	Type	Description
36	GNDA	-	Analog Ground
37	TEST	I	Test Mode Input
38	OSCIN	I	Operating Clock Input. The pin is grounded when internal clock ins used
40	IN9A	I	H-bridge 9, DC Motor Input A
41	IN9B	I	H-bridge 9, DC Motor Input B
42	INAA	I	H-bridge 10, DC Motor Input A
43	INAB	I	H-bridge 10, DC Motor Input B
47	OUTAB	O	H-bridge 10, Output B
48	OUTAA	O	H-bridge 10, Output A
49	PGND9A	-	Stepper 9, 10 Channel Ground
50	OUT9B	O	H-bridge 9, Output B
51	VM9A	-	H-bridge 9, 10 Power Supply
52	OUT9A	O	H-bridge 9, Output A
54	OUT8B	O	H-bridge 8, Output B
55	OUT8A	O	H-bridge 8, Output A
56	PGND78	-	Stepper 7, 8 Channel Ground
57	OUT7B	O	H-bridge 7, Output B
58	OUT7A	O	H-bridge 7, Output A
59	VM78	-	H-bridge 7, 8 Power Supply
61	OUT6B	O	H-bridge 6, Output B
62	OUT6A	O	H-bridge 6, Output A
63	PGND56	-	Stepper 5, 6 Channel Ground
64	OUT5B	O	H-bridge 5, Output B
65	OUT5A	O	H-bridge 5, Output A
66	VM56	-	H-bridge 5, 6 Power Supply
68	VD9A	I	Stepper Synchronous Signal Input 5
69	VD78	I	Stepper Synchronous Signal Input 4
70	VD56	I	Stepper Synchronous Signal Input 3
71	VD34	I	Stepper Synchronous Signal Input 2
72	VD12	I	Stepper Synchronous Signal Input 1
73	VDIS	I	Iris Synchronous Signal Input

Pin	Name	Type	Description
74	GNDD	-	Digital Ground
76	VIO	-	Interface Power Supply
77	VDDD	-	Digital Power Supply
78	RSTB	I	Reset Signal Input
79	SCK	I	SPI Clock
80	SIN	I	SPI Data
81	SOUT	O	SPI Output
82	CS	I	SPI Chip Select
84	PLS5	O	Motor State Pulse 5 Output
85	PLS4	O	Motor State Pulse 4 Output
86	PLS3	O	Motor State Pulse 3 Output
87	PLS2	O	Motor State Pulse 2 Output
88	PLS1	O	Motor State Pulse 1 Output
7, 14, 23, 24, 35, 39, 44, 45, 46, 53, 60, 67, 75, 83	NC	-	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Ratings

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Ratings	Unit
Power Supply, Control Part [1]	-0.3 ~ +4.0	V
	-0.3 ~ +4.0	
Interface Power Supply [1]	-0.3 ~ +6.0	V
Motor Control Power Supply 1 [1]	-0.3 ~ +6.0	V
Motor Control Power Supply 2 [1]	-0.3 ~ +6.0	V
Power Dissipation [2]	141.1	mW
Operating Temperature [3]	-40 ~ +105	°C
Storage Temperature [3]	-65 ~ +150	°C
Motor Driver 1 (Focus, Zoom), H-bridge Driving Current	±0.4	A/ch
Motor Driver (Iris), H-bridge Driving Current	±0.4	A/ch
Instantaneous H-bridge Driving Current	±0.65	A/ch
Input Voltage, Digital Part [4]	-0.3 ~ (VIO + 0.3)	V
ESD	±3k	V

Note:

1. Absolute maximum ratings are used in the range of power dissipation.

2. Power dissipation refers to the value of encapsulated monomer at Ta= 85°C. In practice, it is expected to refer to the technical data and PD-Ta characteristic diagram on the basis of power supply, load, ambient temperature conditions, and then carry out the heat dissipation design which does not exceed the power dissipation value.

3. Except power dissipation, ambient temperature, and storage temperature parameters, all parameters are at Ta = 25°C.

4. (VIO+0.3) voltage shall not exceed 5.5V.

Operating Power Supply

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	VDDD VDDA	2.7	3.3	5	V
	VIO	1.2		5.5	
	VMxx	3.0	5.0	5.5	
	VDD5	3.0	5.0	5.5	

Terminal Tolerance Current and Voltage Ranges

Note:

1. Terminal tolerance current and voltage ranges, refer to the parameters cannot exceed the absolute maximum ratings in any conditions.

2. Rated voltage value refers to each terminal voltage with respect to GND . GND is the voltage of GNDD, MGNDx.

3. In applications, VDDA and VDDD need to be connected together and they can connect with 2.7V~5V power supply. In addition, it should be ensured that VMxx voltage is more than or equal to VDDA voltage.

4. Outside input voltage and current are strictly prohibited except the described terminals below.

5. For the current, "+" means the current flowing to IC, and "-" means the current flowing out from IC.

Pin	Name	Range	Unit
24	OP3INP	-0.3 ~ (VDDA + 0.3)	V
29	ADTESTIN	-0.3 ~ (VDDA + 0.3)	V
32	TEST	-0.3 ~ (VIO + 0.3)	V
33	OSCIN	-0.3 ~ (VIO + 0.3)	V
71	CS	-0.3 ~ (VIO + 0.3)	V
68	SCK	-0.3 ~ (VIO + 0.3)	V
69	SIN	-0.3 ~ (VIO + 0.3)	V
63	VD_IS	-0.3 ~ (VIO + 0.3)	V
58~62	VDxx	-0.3 ~ (VIO + 0.3)	V
67	RSTB	-0.3 ~ (VIO + 0.3)	V
25	OP4INN	-0.3 ~ (VDDA + 0.3)	V
	OUTxx	±0.15	A
13~16	LEDx	30	mA

Note: (VDDA+0.3) voltage should not exceed 5.5V. (VIO+0.3) voltage should not exceed 5.5V.

ELECTRICAL CHARACTERISTICS

VDD5=VMx=5V, VDDD=VDDA=3.3V, VIO=3.3V. Unless other noted,Ta=25°C±2°C。

Current Consumption

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VMxx Power Supply Current when Reset	Imdisable	27MHz Input, RSTB=L		0		μA
VMxx Power Supply Current when Enable	Imenable	27MHz Input, RSTB=H		0.13		mA
VDD5 Power Supply Current when Reset	Ivdd5reset	27MHz Input, RSTB=L		0		μA
VDD5 Power Supply Current when Enable	Ivdd5enable	27MHz Input, RSTB=H		0.12		mA
VDDD Power Supply Current when Reset	Ivdddreset	27MHz Input, RSTB=L		55		μA
VDDD Power Supply Current when Enable	Ivdddenable	27MHz Input, RSTB=H		6.9		mA
VDDA Power Supply Current when Reset	Ivddareset	27MHz Input, RSTB=L		0		μA
VDDA Power Supply Current when Enable	Ivddaenable	27MHz Input, RSTB=H		0.32		mA
VIO Power Supply Current when Reset	Iioreset	27MHz Input, RSTB=L		52		μA
VIO Power Supply Current when Enable	Iioenable	27MHz Input, RSTB=H		54		μA
Total Quiescent Current when Reset		27MHz Input, RSTB=L		0.3		mA
Total Quiescent Current when Enable		27MHz Input, RSTB=H		8		mA
Total Operating Current when Reset		27MHz Input, RSTB=L, FZ = Enable		0.37		mA
Total Operating Current when Enable		27MHz Input, RSTB=H, FZ = Enable		13.4		mA

Digital Input and Output

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Voltage	$V_{in(H)}$	RSTB		0.52×VIO		V
Low-level Input Voltage	$V_{in(L)}$	RSTB		0.42×VIO		V
SOUT High-level Output Voltage	$V_{out(H)}$: SDATA	[SOUT] 1mA Current Source		VIO		V
SOUT Low-level Output Voltage	$V_{out(L)}$: SDATA	[SOUT] 1mA Current Sink		0		V
PLS1~5 High-level Output Voltage	$V_{out(H)}$: MUX			VIO		V
PLS1~5 Low-level Output Voltage	$V_{out(L)}$: MUX			0		V
Input Pull-down Impedance	$R_{pullret}$	RSTB		102		kΩ

Motor Driver Part 1 (Focal, Zoom, Step Channel OUT1x~OUT8x)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
H-bridge ON Impedance	R_{onFZ}	IM = 100mA		1.1		Ω
H-bridge Leakage Current	I_{leakFZ}			0	1	μA

Motor Driver Part 2 (Step DC Multiplexing Channel, OUT9x, OUTAx)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
H-bridge ON Impedance	R_{onFZ}	IM = 100mA		1.1		Ω
H-bridge Leakage Current	I_{leakFZ}			0	1	μA

Motor Driver Part 3 (Iris, OUTE1, OUTE2)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
H-bridge ON Impedance	R_{onFZ}	IM = 50mA		1.2		Ω
H-bridge Leakage Current	I_{leakFZ}			0	1	μA

LED Driver

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output ON Impedance	R_{onLED}	IM = 20mA, 5V cell		1.73		Ω
Output Leakage Current	$I_{leakLED}$			0	1	μA

OPAMP3 (Hall Sensor Output Amplifier)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage	V_{IN}		0.5×VDDA-0.5	0.5×VDDA	0.5×VDDA+0.5	V
Input Offset Voltage	V_{OF}		-15	1.5	15	mV
Output Voltage (Low)	V_{OL}	ILOAD = - 100μA		0.1		V
Output Voltage (High)	V_{OH}	ILOAD = 100μA	VDDA-0.2	VDDA-0.1		V
Gain	V_{OG}	Gain Setting Value: 0h	20.5	21.3	22.8	V/V

OPAMP4 (For Eliminating Common-mode Voltage of Hall Sensor)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage	VIN		0.5×VDDA-0.2		0.5×VDDA-0.2	V
Input Offset Voltage	VOF		-10	1	10	mV
Output Voltage (Low)	VOL	ILOAD = - 10μA		0.1		V
Output Voltage (High)	VOH	ILOAD = 3mA	VDDA-0.5	VDDA-0.2		V

Refer Output Voltage

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Voltage 1	VREF	ILOAD = 0 A， CVREF = 100pF	0.5×VDDA-0.1	0.5×VDDA	0.5×VDDA+0.1	V
Output Voltage 2	VREFL	ILOAD = ±100μA, CVREF = 100pF	0.5×VDDA-0.1	0.5×VDDA	0.5×VDDA+0.1	V

Hall Bias Control (SENS Terminal Output)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Minimum Output Current	IBL	REF = 10kΩ, SENS = 0.7V Setting Value: 00h		0	0.1	mA
Output Current Accuracy 1	IB40H	REF = 10kΩ, SENS = 0.7V Setting Value: 40h		0.98		mA
Output Current Accuracy 2	IBBFH	REF = 10kΩ, SENS = 0.7V Setting Value: BEh		2.92		mA

Digital Input/Output

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Threshold Voltage	$V_{in(H)}$	SCK,SIN,CS,VD_IS,VD_FZ,TEST		0.41×VIO		V V
Low-level Input Threshold Voltage	$V_{in(L)}$	SCK,SIN,CS,VD_IS,VD_FZ,TEST		0.3×VIO		V V
RSTB Signal Pulse	T_{rst}		100			μs
Input Maximum Hysteresis Error	V_{hysin}	SCK,SIN,CS,VD_IS,VD_FZ,TEST		0.11×VIO		V
Image Synchronous Signal Width	VD_w		80			μs
CS Signal Wait Signal 1	$T_{(VD-CS)}$		400			ns
CS Signal Wait Signal 2	$T_{(CS-DT1)}$		5			μs

Pulse Generator

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Wait Time for Pulse 1 to Arrive	PL1wait	OSCIN = 27MHz		20.1		μs
Pulse 1 Pulse Width	PL1width	OSCIN = 27MHz		1.2		μs
Wait Time for Pulse 2 to Arrive	PL2wait	OSCIN = 27MHz		20.1		μs

Iris Control

Parameter	Symbol	Condition	Min	Typ	Max	Unit
AD Reference Frequency	$IRIS_{Sample}$	OSCIN = 27MHz		500		kHz

Thermal Shutdown

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Temperature of Thermal Shutdown	Ttsd			150		°C
Maximum Hysteresis Error of Thermal Shutdown	ΔTtsd			35		°C

Power Supply Monitoring Circuit

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VDDD VDDA Reset	Vrston			2.4		V
VDDD VDDA Reset Maximum Hysteresis Error	Vrsthys			0.2		V
VIO Reset				1.1		V
VIO Reset Maximum Hysteresis Error				0.1		V
VMxx Reset				2.3		V
VMxx Reset Maximum Hysteresis Error				0.1		V
VDD5 Reset				2.3		V
VDD5 Reset Maximum Hysteresis Error				0.1		V

8bit DAC for Hall Offset Adjustment

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Adjustment Range (High)	DAOTHof			VDDA		V
Adjustment Range (Low)	DAOTLof			0		V

10bit ADC

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Range (High)	$V_{in(H)}$				VDDA-0.2	V
Input Range (Low)	$V_{in(L)}$		0.2			V
Differential Nolinearity Error	DNL10A			1.0		LSB
Integral Nolinearity Error	INL10A			2.0		LSB

FUNCTION DESCRIPTION

1. Serial Interface

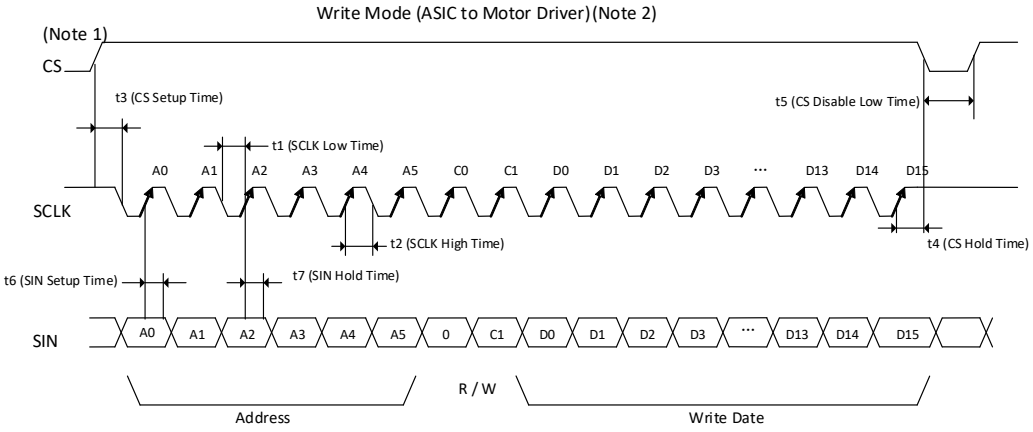


Figure 1. Write Data

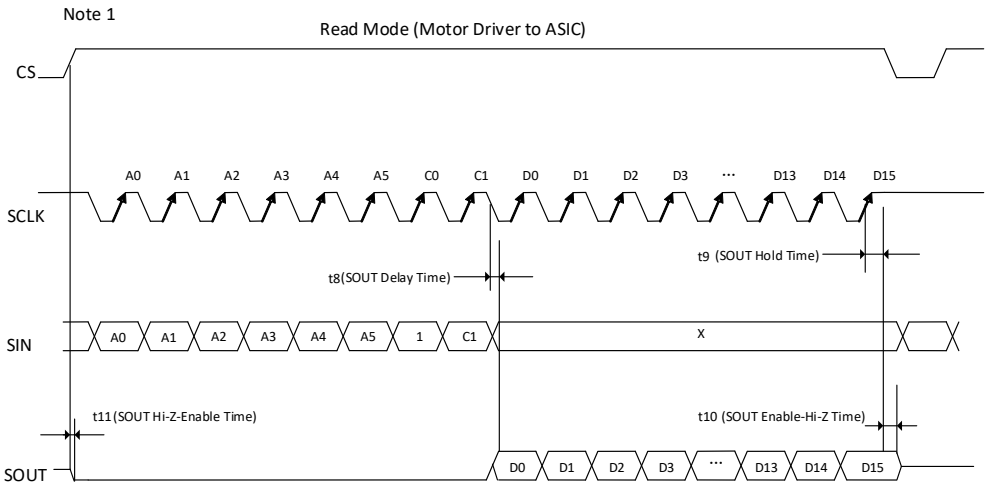


Figure 2. Read Data

Note:

1. In read/write mode, each CS cycle starts from 0 by default.

2. In write mode, system clock must be input from OSCIN terminal.

Electrical Parameters (Design Reference)

VDD5=VMxx =5V, VDDD=VDDA=3.3V, VIO=3.3V. Unless other noted, Ta = 25°C±2°C。

1.1 Serial Port Input

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Serial Clock	Sclock		1		5	MHz
SCK Low Time	t1		100			ns
SCK High Time	t2		100			ns
CS Setup Time	t3		60			ns
CS Hold Time	t4		60			ns
CS Disable Low time	t5		100			ns
SIN Setup Time	t6		50			ns
SIN Hold Time	t7		50			ns
SOUT Delay Time	t8				60	ns
SOUT Hold Time	t9		60			ns
SOUT Enable-Hi-Z Time	t10				60	ns
SOUT Hi-Z-Enable Time	t11				60	ns
SOUT Capacitor Load	Csc				40	pF

1. The data conversion starts at the rising edge of CS and stops at the falling edge of CS.
2. The data stream unit of a conversion is 24 bits.
3. When the address and data are input from the SIN pin, the clock signal SCK remains consistent under the condition that CS = 1.
4. The data is driven into IC at the rising edge of the SCK signal. At the same time, when the data is output, it is read out from the SOUT pin (the data is output at the rising edge of SCK).
5. SOUT outputs high-impedance state at CS = 0, and outputs "0" at CS = 1 unless there is a data read.
6. The control of the entire serial interface is reset at CS = 0.

1.2 Data Format

0	1	2	3	4	5	6	7
A0	A1	A2	A3	A4	A5	C0	C1

8	9	10	11	12	13	14	15
D0	D1	D2	D3	D4	D5	D6	D7

16	17	18	19	20	21	22	23
D8	D9	D10	D11	D12	D13	D14	D15

C0: register read and write options: 0: write mode, 1: read mode

C1: no use

A5~A0: register address

D15~D0: data written to register

1.3 Register Distribution

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00H							IRS_TGT<9:0>									
01H	DGAIN<6:0>							ASOUND_LPF_FC<2:0>			AS_FLT_OFF	DEC_AVE	OVER_LPF_FC_2ND<1:0>		OVER_LPF_FC_1ST<1:0>	
02H	PID_POLE<3:0>				PID_ZERO<3:0>				IRIS_ROUND<3:0>				IRIS_CALC_NR<3:0>			
03H			DT_ADJ_IRIS<1:0>		PWM_IRIS<2:0>			PWM_LPF_FC<2:0>			PWM_FLT_OFF	LMT_ENB	ARW<3:0>			
04H	HALL_OFFSET_DAC<7:0>								HALL_BAIS_DAC<7:0>							
05H				AAF_FC	HALL_GAIN<3:0>						PID_INV	TGT_FLT_OFF	TGT_LPF_FC<3:0>			
06H							START1<9:0>									
07H	P1EN				WIDTH1<11:0>											
08H							START2<9:0>									
09H	P2EN										WIDTH2<5:0>					
0AH						DUTY_TEST	TGT_IN_TEST<9:0>									
0BH	PID_CLIP<3:0>				ADC_TEST	PDWNB	MODESEL_FZ	MODESEL_IRIS	TESTEN1			ASWMODE<1:0>			OCPIris_dly<1:0>	
0CH							IRSAD<9:0>(Read Only)									
0DH																
0EH				AVE_SPEED<4:0>					TGT_UPDATE<7:0>							
0FH						Reserved<10:0>										
20H	DC_EN	DC_Ex_EN							DT1<7:0>							
21H																
22H	MICROAB<1:0>		PHMODAB<5:0>						DT2A							
23H	PPWB<7:0>								PPWA<7:0>							
24H	LEDA	ENDISAB	BREAKAB	CWCCWAB	PSUMAB<11:0>											
25H	INTCTAB<15:0>															
26H	TESTEN2_1	FZTEST_1<4:0>					OCP1_dly<1:0>			PWMRESAB<1:0>		PWMMODEAB<4:0>				
27H									DT2B							
28H	PPWD<7:0>								PPWC<7:0>							
29H	LEDB	ENDISCD	BREAKCD	CWCCWCD	PSUMCD<11:0>											
2AH	INTCTCD<15:0>															
2BH	TESTEN2_2	FZTEST_2<4:0>					OCP2_dly<1:0>			PWMRESCD<1:0>		PWMMODECD<4:0>				
2CH	MICROEF<1:0>		PHMODAB<5:0>						DT2C							
2DH	PPWF<7:0>								PPWE<7:0>							
2EH	LEDC	ENDISEF	BREAKEF	CWCCWEF	PSUMEF<11:0>											
2FH	INTCTEF<15:0>															
30H	TESTEN2_3	FZTEST_3<4:0>					OCP3_dly<1:0>			PWMRESEF<1:0>		PWMMODEEF<4:0>				
31H									DT2D							
32H	PPWH<7:0>								PPWG<7:0>							
33H	LEDD	ENDISGH	BREAKGH	CWCCWGH	PSUMGH<11:0>											
34H	INTCTGH<15:0>															
35H	TESTEN2_4	FZTEST_4<4:0>					OCP4_dly<1:0>			PWMRESGH<1:0>		PWMMODEGH<4:0>				
36H	MICROIJ<1:0>		PHMODIJ<5:0>						DT2E							
37H	PPWJ<7:0>								PPWI<7:0>							
38H		ENDISIJ	BREAKIJ	CWCCWIJ	PSUMIJ<11:0>											
39H	INTCTIJ<15:0>															
3AH	TESTEN2_5	FZTEST_5<4:0>					OCP5_dly<1:0>			PWMRESIJ<1:0>		PWMMODEIJ<4:0>				
3BH					DC_CTL_A<1:0>		DCA_PWM_Freq<1:0>			DCA_PWM_Duty<6:0>						
3CH					DC_CTL_B<1:0>		DCB_PWM_Freq<1:0>			DCB_PWM_Duty<6:0>						
3DH																
3EH									TSD_Clr		OCPIris_Clr	OCP5_Clr	OCP4_Clr	OCP3_Clr	OCP2_Clr	OCP1_Clr

1.4 Register List

Iris Module

Address	Register Name/Bit Width	Description	Page
00h	IRIS_TGT[9:0]	Iris Target Value	23
01h	OVER_LPF_FC_1ST[1:0]	ADC Feedback Filter (1) Cut-Off Frequency	23
	OVER_LPF_FC_2ND[1:0]	ADC Feedback Filter (2) Cut-Off Frequency	24
	DEC_AVE	Moving Average of Iris Target Value	24
	AS_FLT_OFF	Low-pass Filter before PID Controller Enable/Disable	24
	ASOUND_LPF_FC[2:0]	Cut-off Frequency of Low-pass Filter before PID Controller	25
	DGAIN[6:0]	PID Controller Digital Gain	25
02h	IRIS_CALC_NR[3:0]	Upper Limit of Error Accumulation of PID Controller Integrator	27
	IRIS_ROUND[3:0]	Upper Limit of Error Accumulation of PID Controller Differentiator	27
	PID_ZERO[3:0]	PID Controller Zero	27
	PID_POLE[3:0]	PID Controller Pole	28
03h	ARW[3:0]	Number of Bits of PID Controller Integrator	28
	LMT_ENB	PID Controller Integrator Stop	29
	PWM_FLT_OFF	Low-pass Filter after PID Controller Enable/Disable	30
	PWM_LPF_FC[2:0]	Cut-off Frequency of Low-pass Filter after PID Controller	30
	PWM_IRIS[2:0]	PWM Frequency of Iris Module Output	30
	DT_ADJ_IRIS[1:0]	Dead Time Setting of Iris Module Output	31
04h	HALL_BIAS_DAC[7:0]	Bias Current of Hall Element	37
	HALL_OFFSET_DAC[7:0]	Offset Adjustment of Hall Element Output Amplifier	37
05h	TGT_LPF_FC[3:0]	Iris Target Value Low-pass Filter Cut-off Frequency	31
	TGT_FLT_OFF	Iris Target Value Low-pass Filter Enable/Disable	31
	PID_INV	PID Controller Polarity	32
	HALL_GAIN[3:0]	Hall Element Output Amplifier Gain	37
	AAF_FC	Cut-off Frequency of Hall Element Output Amplifier	38
06h	START1[9:0]	Pulse 1 Start Position	32
07h	WIDTH1[11:0]	Pulse 1 Pulse Width	32
	P1EN	Pulse 1 Output Enable	32
08h	START2[9:0]	Pulse 2 Start Position	33
09h	WIDTH2[5:0]	Pulse 2 Pulse Width	33
	P2EN	Pulse 2 Output Enable	33
0Ah	TGT_IN_TEST[9:0]	Iris Module Output Duty Direct Specified Value	34
	DUTY_TEST	Iris Module Output Duty Enable	34

Address	Register Name/Bit Width	Description	Page
0Bh	OCPIris_dly[1:0]	Iris Module Overcurrent Judge Threshold	38
	ASWMODE[1:0]	ADTESTIN Pin Connection Selection	38
	TESTEN1	TEST Mode Enable 1	49
	MODESEL_IRIS	VD_IS Polarity Selection	22
	MODESEL_FZ	VD_FZ Polarity Selection	22
	PDWNB	Iris Module Off	38
	ADC_TEST	ADC Test Mode Selection	39
	PID_CLIP[3:0]	Iris Module Output Maximum Duty	40
0Ch	IRSAD[9:0]	ADC Value Output (Read Only)	40
0Eh	TGT_UPDATE[7:0]	IRS_TGT (Iris Target) Update Delay	35
	AVE_SPEED[4:0]	Iris Target Moving Average Speed	35

Stepper Module

Address	Register Name/Bit Width	Description	Page
20h	DT1[7:0]	Start Point Wait Time	44
	DC_EX_EN	Dual-Channel DC External Pin Control Enable	53
	DC_EN	ε Motor Channel Multiplexed as Dual-Channel DC Control Enable	53
22h/*27h/2Ch /*31h/36h	DT2**A** / B / C / D / E[7:0]	**α**/β/γ/δ/ε Channel Motor Start Point Excitation Wait Time	44
	PHMOD**AB** / *CD / EF / *GH / IJ [5:0]	**α**/*β/γ/*δ/ε Channel Motor Phase Correction	45
	MICRO**AB** / *CD / EF / *GH / IJ [1:0]	**α**/*β/γ/*δ/ε Channel Motor Microstep Selection	44
23h/28h/2Dh/ 32h/37h	PPW**A** / C / E / G / I [7:0]	**A**/C/E/G/I Channel Peak Pulse Width	45
	PPW**B** / D / F / H / J [7:0]	**B**/D/F/H/J Channel Peak Pulse Width	45
24h/29h/2Eh/ 33h/38h/	PSUM**AB** / CD / EF / GH / IJ [11:0]	**α**/β/γ/δ/ε Channel Step Number	46
	CCWCW**AB** / CD / EF / GH / IJ	**α**/β/γ/δ/ε Channel Motor Rotation Direction	47
	BRAKE**AB** / CD / EF / GH / IJ	**α**/β/γ/δ/ε Channel Motor Brake	47
	ENDIS**AB** / CD / EF / GH / IJ	**α**/β/γ/δ/ε Channel Motor Enable/Disable	47
	LED**A** / B / C / D / -	LED **A** / B / C / D Output Control	46
25h/2Ah/2Fh/ 34h/39h	INTCT**AB** / CD / EF / GH / IJ [15:0]	**α**/β/γ/δ/ε Channel Motor Step Cycle	47
26h/2Bh/30h/ 35h/3Ah	PWMMODE**AB** / CD / EF / GH / IJ [4:0]	**α**/β/γ/δ/ε Channel Motor Microstep Output PWM Frequency	52
	PWMRES**AB** / CD / EF / GH / IJ [1:0]	**α**/β/γ/δ/ε Channel Motor Microstep Output PWM Resolution	52

Address	Register Name/Bit Width	Description	Page
26h/2Bh/30h/ 35h/3Ah	OCP**1** / 2 / 3 / 4 / 5_dly[1:0]	**α**/β/γ/δ/ε Channel Motor Overcurrent Judge Threshold	51
	FZTEST_**1** / 2 / 3 / 4 / 5 [4:0]	PLS**1** / 2 / 3 / 4 / 5 Pin Output Signal Selection	49
	TESTEN2_**1** / 2 / 3 / 4 / 5	Motor Channel Test Output Enable	49
3Bh/3Ch	DC**A** / B_PWM_Duty[6:0]	DC Motor A / B Channel State Control	53
	DC**A** / B_PWM_Freq[1:0]	DC Motor A / B PWM Channel Frequency Control	53
	DC_CTL_**A** / B[1:0]	DC Motor A / B PMW Channel Duty Control	53
3Eh	OCPx_Clr	Clear Overcurrent Lock State for Corresponding Channel	54
	TSD_Clr	Clear Thermal Shutdown Indication	54

All register bit data is initialized when RSTB = 0.

α channel corresponds to the stepper motor channel consisting of OUT1A, OUT1B, OUT2A and OUT2B.

β channel corresponds to the stepper motor channel consisting of OUT3A, OUT3B, OUT4A and OUT4B.

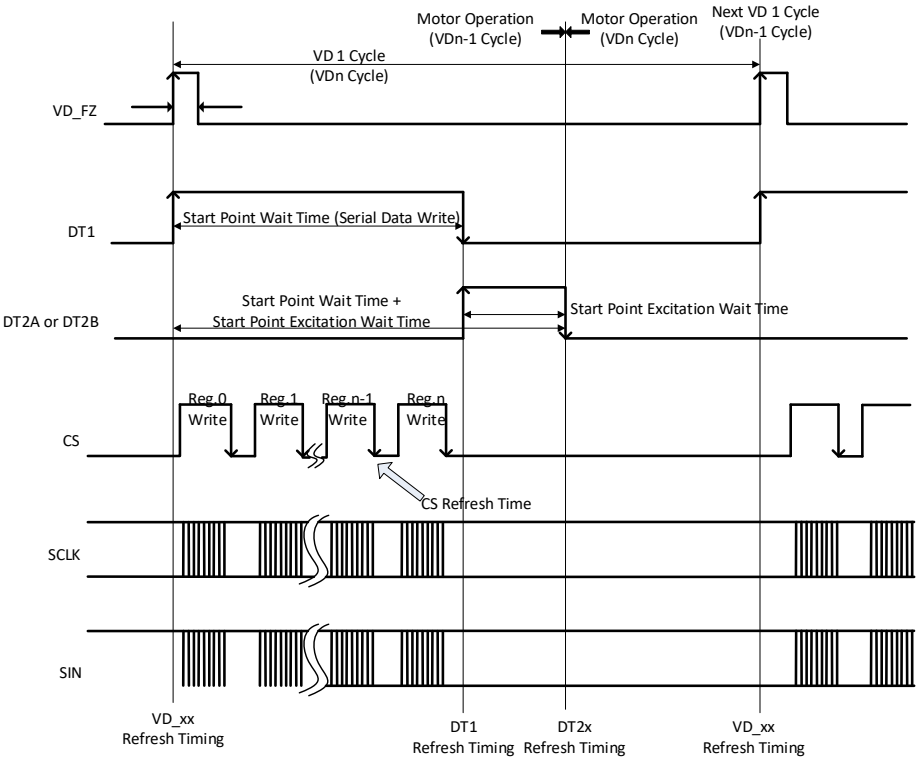
γ channel corresponds to the stepper motor channel consisting of OUT5A, OUT5B, OUT6A and OUT6B.

δ channel corresponds to the stepper motor channel consisting of OUT7A, OUT7B, OUT8A and OUT8B.

ε channel corresponds to the stepper motor channel consisting of OUT9A, OUT9B, OUTAA and OUTAB.

*Note: β channel and δ channel corresponding to 27h, 31h address have no microstep options (fixed to 256 division) and phase correction options. D15~D8 in 27h, 31h address are fixed to 0.

1.5 Register Setup Time



Address	Register Name	Setup Timing
00h	IRIS_TGT[9:0]	VD_IS+Adjusted Value
01h	OVER_LPF_FC_1ST[1:0]	VD_IS
	OVER_LPF_FC_2ND[1:0]	VD_IS
	DEC_AVE	VD_IS
	AS_FLT_OFF	VD_IS
	ASOUND_LPF_FC[2:0]	VD_IS
	DGAIN[6:0]	VD_IS
02h	IRIS_CALC_NR[3:0]	VD_IS
	IRIS_ROUND[3:0]	VD_IS
	PID_ZERO[3:0]	VD_IS
	PID_POLE[3:0]	VD_IS
03h	ARW[3:0]	VD_IS
	LMT_ENB	VD_IS
	PWM_FLT_OFF	VD_IS
	PWM_LPF_FC[2:0]	VD_IS
	PWM_IRIS[2:0]	VD_IS
	DT_ADJ_IRIS[1:0]	VD_IS
04h	HALL_BIAS_DAC[7:0]	VD_IS
	HALL_OFFSET_DAC[7:0]	VD_IS
05h	TGT_LPF_FC[3:0]	VD_IS
	TGT_FLT_OFF	VD_IS
	PID_INV	VD_IS
	HALL_GAIN[3:0]	VD_IS
	AAF_FC	VD_IS
06h	START1[9:0]	VD_IS
07h	WIDTH1[11:0]	VD_IS
	P1EN	VD_IS
08h	START2[9:0]	VD_IS
09h	WIDTH2[5:0]	VD_IS
	P2EN	VD_IS
0Ah	TGT_IN_TEST[9:0]	CS
	DUTY_TEST	CS

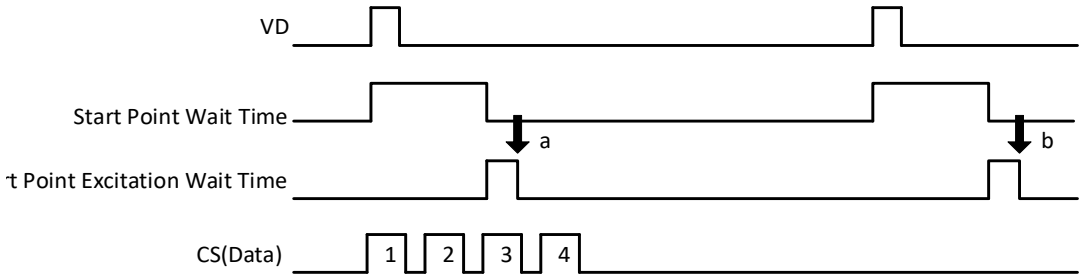
Address	Register Name	Setup Timing
0Bh	OCPIris_dly[1:0]	CS
	ASWMODE[1:0]	CS
	TESTEN1	CS
	MODESEL_IRIS	CS
	MODESEL_FZ	CS
	PDWNB	CS
	ADC_TEST	CS
	PID_CLIP[3:0]	VD_IS
0Ch	IRSAD[9:0]	Read Only
0Eh	TGT_UPDATE[7:0]	CS
	AVE_SPEED[4:0]	VD_IS
20h	DT1[7:0]	VD_FZ
	DC_EX_EN	VD_FZ
	DC_EN	VD_FZ
22h/*27h/2Ch/*31h/36h	DT2**A** / B / C / D / E[7:0]	DT1
	PHMOD**AB** / *CD / EF / *GH / IJ [5:0]	DT2A /B / C / D / E
	MICRO**AB** / *CD / EF / *GH / IJ [1:0]	DT2A /B / C / D / E
23h/28h/2Dh/32h/37h	PPW**A** / C / E / G / I [7:0]	DT1
	PPW**B** / D / F / H / J [7:0]	DT1
24h/29h/2Eh/33h/38h	PSUM**AB** / CD / EF / GH / IJ [11:0]	DT2A /B / C / D / E
	CCWCW**AB** / CD / EF / GH / IJ	DT2A /B / C / D / E
	BRAKE**AB** / CD / EF / GH / IJ	DT2A /B / C / D / E
	ENDIS**AB** / CD / EF / GH / IJ	DT1 or DT2A /B / C / D / E*
	LED**A** / B / C / D / -	CS
25h/2Ah/2Fh/34h/39h	INTCT**AB** / CD / EF / GH / IJ [15:0]	DT2A /B / C / D / E
26h/2Bh/30h/35h/3Ah	PWMMODE**AB** / CD / EF / GH / IJ [4:0]	DT2A /B / C / D / E
	PWMRES**AB** / CD / EF / GH / IJ [1:0]	DT2A /B / C / D / E
	OCP**1** / 2 / 3 / 4 / 5_dly[1:0]	DT2A /B / C / D / E
	FZTEST_**1** / 2 / 3 / 4 / 5 [4:0]	DT1 or DT2A /B / C / D / E*
	TESTEN2_**1** / 2 / 3 / 4 / 5	CS
3Bh/3Ch	DC**A** / B_PWM_Duty[6:0]	CS
	DC**A** / B_PWM_Freq[1:0]	CS
	DC_CTL_**A** / B[1:0]	CS
3Eh	OCPx_Clr	CS
	TSD_Clr	CS

* 0→1: it works on DT1 ; 1→0: it works on DT2x.

*Note: β channel and δ channel corresponding to 27h, 31h address have no microstep options (fixed to 256 division) and phase correction options. D15~D8 in 27h, 31h address are fixed to 0.

In principle, the setup of registers for microstep should be completed during the time period of start point delay (refer to the figure on page 19). Data written outside the start point delay can also be stored in registers. However, if the write operation is executed after the refresh time, the written register will not be valid at the scheduled time. For example, if the updated data 1~4 after the start point excitation delay is written as shown in the following figure, data 1 and 2 are immediately updated at timing a, and data 3 and 4 are updated at timing b. Even if the data is written continuously, the update interval is 1 VD cycle.

For the above reasons, in order to update data timely, the setup of the register data needs to be completed during the time period of start point delay.



2. VD Signal Internal Processing

In this system, the reflection time and rotation time of the stepper motor are respectively based on the rising edges of VD_IS and VD_FZ. The polarities of VD_IS and VD_FZ are set by the following register settings.

Register Details

MODESEL_FZ (VD_FZ Polarity Selection)

MODESEL_IRIS (VD_IS Polarity Selection)

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						MODE SEL_FZ	MODE SEL_IRIS								

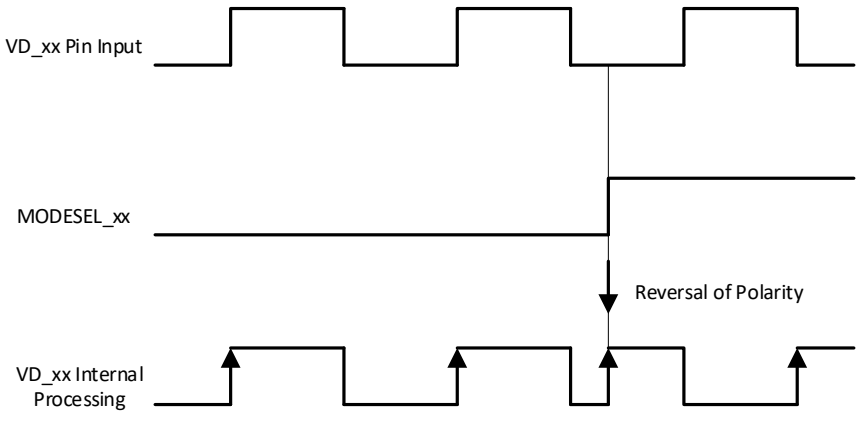
MODEL_FZ and MODESEL_IRIS respectively set the polarities of VD_FZ and VD_IS inputting to IC.

When set to "0", the polarity is based on the rising edge of VD_xx.

When set to "1", the polarity is based on the falling edge of VD_xx.

MODESEL_xx selects the polarity of input VD_xx. Therefore, based on the selection timing of MODESEL_xx, the edge as shown in the following figure is independent of the edge of VD_xx.

Set Value	VD Polarity
0	Non-inverting
1	inverting



Based on the Rising Edge of VD_xx Internal Processing

3. Iris Control

3.1 Features

- PWM Wave Drive → Low Power Dissipation
- Set Each Filter by Register → Low Noise
- Built-in Passive Components around the Gain Amplifier →Damp External Part
- Built-in 8bit DAC Used to Adjust Hall Compensation
- Built-in Current DAC Used to Adjust Hall Bias Current

3.2 Register Details

IRIS_TGT[9:0] (Iris Desired Value)

Address			00h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						IRIS_TGT[9:0]									

IRIS_TGT[9:0] sets the desired ADC input, which is also determined by iris position, that is, the register bit determines the desired position information.

Set Value	AD Input Desired Value
0	VDDA × 0 / 1023
1	VDDA × 1 / 1023
1023	VDDA × 1023 / 1023
n	VDDA × n / 1023

OVER_LPF_FC_1ST[1:0] (ADC Feedback Low-pass Filter (1) Cut-off Frequency)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
														OVER_LPF_FC_1ST[1:0]	

Set the cut-off frequency of LPF(1) in AD feedback module.

Lower cut-off frequency can effectively eliminate the noise generated by the ADC.

In general, set OVER_LPF_FC_1ST[1:0] = 0.

Set Value	Cut-off Frequency
0	2600Hz
1	3600Hz
2	5200Hz
3	8000Hz

OVER_LPF_FC_2ND[1:0] (ADC Feedback Low-pass Filter (2) Cut-off Frequency)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												OVER_LPF_FC_2ND[1:0]			

Set the cut-off frequency of LPF(2) in AD feedback module.

Lower cutoff frequency can effectively eliminate the noise generated by the ADC.

In general, set OVER_LPF_FC_2ND[1:0] = 0.

Set Value	Cut-off Frequency
0	2600Hz
1	3600Hz
2	5200Hz
3	8000Hz

DEC_AVE (Moving Average of Iris Target Value)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											DEC_AVE				

Sets the moving average of the Iris target value.

A large moving average makes the Iris target change more slowly.

In general, set DEC_AVE = 0.

Set Value	Moving Average
0	8
1	4

AS_FLT_OFF (Low-pass Filter before PID Controller Enable/Disable)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										AS_FLT_OFF					

Set whether the filter before PID controller is enabled.

If the algorithm is enabled, the LPF is inserted into the controller.

The LPF removes noise before data enters the PID, and usually set AS_FLT_OFF = 0.

If phase margin is not large enough under the closed-loop frequency condition, in the case of ringing,

AS_FLT_OFF = 1 can be set to improve its phase margin and prevent ringing.

Set Value	Filter before PID
0	Enable
1	Disable

ASOUND_LPF_FC[2:0] (Cut-off Frequency of Low-pass Filter before PID Controller)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							ASOUND_LPF_FC[2:0]								

Set the cut-off frequency of the filter before PID.

Lower cut-off frequency has more effective to remove noise. Normally, set AS_FLT_OFF = 0.

If phase margin is not large enough under the closed-loop frequency condition, in the case of ringing, the cut-off frequency can be increased.

Set Value	Cut-off Frequency
0	900Hz
1	1300Hz
2	1600Hz
3	2000Hz
4	2600Hz
5	3200Hz
6	4000Hz
7	Prohibit

DGAIN[6:0] (PID Controller Gain)

Address			01h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DGAIN[6:0]															

Set the gain of the PID controller.

The setup gain is defined as the gain between AD input at 35Hz and motor input under the conditions of PID zero point=35Hz, pole=900Hz, PWM frequency=31.25kHz. Refer to following table for setup gain.

Set Value	Gain
00h	0
01h~7Fh	{0.125 × {2^(MSB 3 bit - 3'd3)} × [16 + LSB 4 bit]}+3dB

DGAIN[3:0]	DGAIN[6:4]															
	000		001		010		011		100		101		110		111	
	Gain	dB	Gain	dB	增益	dB	Gain	dB	Gain	dB	Gain	dB	Gain	dB	Gain	dB
0h	0	-	0.5	-3.0	1	3.0	2	9.0	4	15.0	8	21.1	16	27.1	32	33.1
1h	0.265625	-8.5	0.53125	-2.5	1.0625	3.5	2.125	9.5	4.25	15.6	8.5	21.6	17	27.6	34	33.6
2h	0.28125	-8.0	0.5625	-2.0	1.125	4.0	2.25	10.0	4.5	16.1	9	22.1	18	28.1	36	34.1
3h	0.296875	-7.5	0.59375	-1.5	1.1875	4.5	2.375	10.5	4.75	16.5	9.5	22.6	19	28.6	38	34.6
4h	0.3125	-7.1	0.625	-1.1	1.25	4.9	2.5	11.0	5	17.0	10	23.0	20	29.0	40	35.0
5h	0.328125	-6.7	0.65625	-0.7	1.3125	5.4	2.625	11.4	5.25	17.4	10.5	23.4	21	29.4	42	35.5
6h	0.34375	-6.3	0.6875	-0.3	1.375	5.8	2.75	11.8	5.5	17.8	11	23.8	22	29.8	44	35.9
7h	0.359375	-5.9	0.71875	0.1	1.4375	6.2	2.875	12.2	5.75	18.2	11.5	24.2	23	30.2	46	36.3
8h	0.375	-5.5	0.75	0.5	1.5	6.5	3	12.5	6	18.6	12	24.6	24	30.6	48	36.6
9h	0.390625	-5.2	0.78125	0.9	1.5625	6.9	3.125	12.9	6.25	18.9	12.5	24.9	25	31.0	50	37.0
AH	0.40625	-4.8	0.8125	1.2	1.625	7.2	3.25	13.2	6.5	19.3	13	25.3	26	31.3	52	37.3
BH	0.421875	-4.5	0.84375	1.5	1.6875	7.5	3.375	13.6	6.75	19.6	13.5	25.6	27	31.6	54	37.6
CH	0.4375	-4.2	0.875	1.8	1.75	7.9	3.5	13.9	7	19.9	14	25.9	28	31.9	56	38.0
DH	0.453125	-3.9	0.90625	2.1	1.8125	8.2	3.625	14.2	7.25	20.2	14.5	26.2	29	32.2	58	38.3
EH	0.46875	-3.6	0.9375	2.4	1.875	8.5	3.75	14.5	7.5	20.5	15	26.5	30	32.5	60	38.6
Fh	0.484375	-3.3	0.96875	2.7	1.9375	8.7	3.875	14.8	7.75	20.8	15.5	26.8	31	32.8	62	38.8

IRIS_CALC_NR[3:0] (Upper Limit of Error Accumulation of PID Controller Integrator)

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												IRIS_CALC_NR[3:0]			

When the register bit is set, that is, the accumulative error generated by the integrator will be reduced. However, the integral algorithm will also be weakened. In general, set IRIS_CALC_NR[3:0] = 0.

Set Value	Upper Limit of Error Accumulation
0	Disable
1~14	$\pm 1/2^{(15-n)}$ LSB
15	± 1 LSB

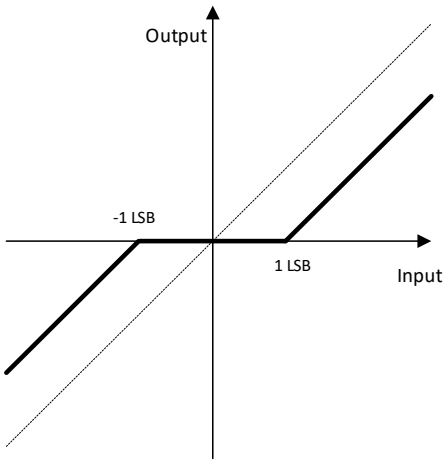
IRIS_ROUND[3:0] (Upper Limit of Error Accumulation of PID Controller Differentiator)

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								IRIS_ROUND[3:0]							

The upper limit of noise response generated by the differentiator is set. When the register is set, the amplitude of the noise generated by the differentiator will be attenuated, and the differential algorithm will be weaken accordingly.

Set Value	Upper limit of Error Accumulation
0	Disable
1~14	$\pm 1/2^{(15-n)}$ LSB
15	± 1 LSB

In the following figure, if the register bit is set to the maximum value, the input signal less than ±1 LSB will be ignored.



PID_ZERO[3:0] (PID Controller Zero)

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				PID_ZERO[3:0]											

Set PID controller zero.

PID_POLE[3:0] (PID Controller Pole)

Address			02h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PID_POLE[3:0]															

Set PID controller pole.

Set Value	Zero
0	10Hz/10Hz
1	15Hz/15Hz
2	20Hz/20Hz
3	25Hz/25Hz
4	30Hz/30Hz
5	35Hz/30Hz
6	35Hz/35Hz
7	40Hz/35Hz
8	40Hz/40Hz
9	45Hz/45Hz
10	50Hz/50Hz
11	55Hz/55Hz
12	60Hz/60Hz
13	65Hz/65Hz
14	70Hz/70Hz
15	75Hz/75Hz

Set Value	Pole
0	710Hz
1	790Hz
2	870Hz
3	950Hz
4	1040Hz
5	1120Hz
6	1200Hz
7	1280Hz
8	1370Hz
9	1450Hz
10	1530Hz
11	1620Hz
12	1700Hz
13	1790Hz
14	1870Hz
15	1960Hz

ARW[3:0] (Number of Bits of PID Controller Integrator)

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												ARW[3:0]			

Set the number of bits of PID controller integrator, which would affect the saturation recovery time of integrator.

Set Value	Number of Bits of PID Controller Integrator
0~3	12bit
4~14	15-(Set Value)bit
15	1bit

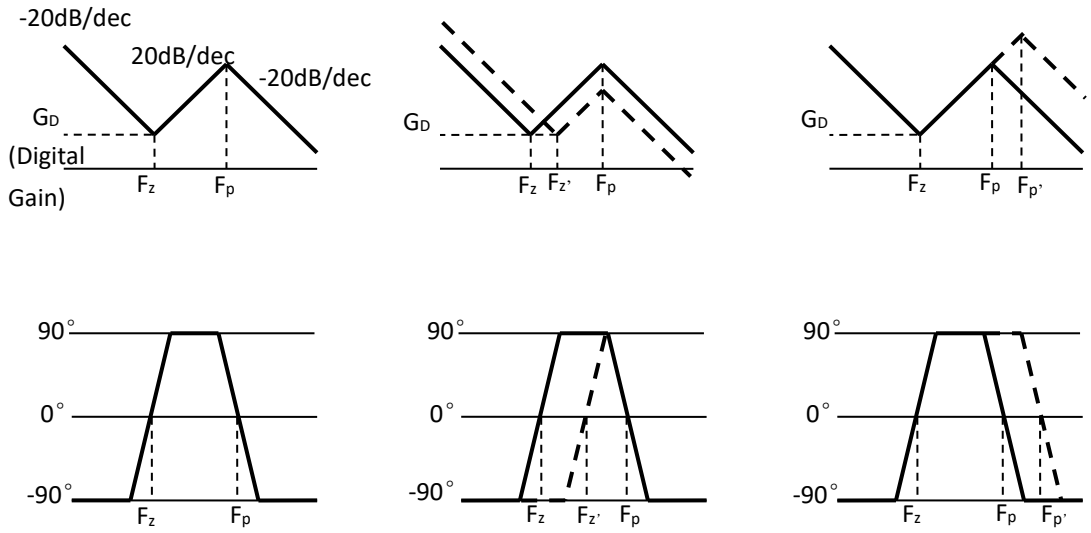
LMT_ENB (PID Controller Integrator Stop)

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											LMT_ENB				

The integrator algorithm stop is enabled or disabled. It has a great influence on the saturation time of PID output.

Set Value	Integrator Stop
0	Disable
1	Enable

The characteristic of PID controller, and the effect of changing PID_ZERO[3:0] and PID_POLE[3:0] are shown below.



G_D:DGAIN[6:0] F_Z:PID_ZERO[3:0] F_P:PID_POLE[3:0]

The position of system pole mainly affects the position of the system amplitude characteristic peak. The position of system zero mainly affects the position of the system amplitude characteristic valley and the degree of depression. The strength of the integrator is determined by the zero position, and the strength of the differentiator is determined by the zero and pole positions together. The smaller the zero position is, the stronger the integral effect will be. The integral effect will reduce the system stability. When the integral effect is strong, the system will be unstable, but the steady-state error can be eliminated. Differential effect by the zero pole joint action, can improve the dynamic characteristics. When differential effect is larger, the overshoot is larger and the adjustment time is shorter. When the differential effect is smaller, the overshoot is also larger and the adjustment time is longer. Only when parameters are set reasonably, the overshoot is smaller and adjustment time is reduced. The increase of gain makes the system sensitive, speed up and steady-state error reduced. When gain is larger, the number of oscillations increases and the overshoot time increases. When the gain is too large, system tends to be unstable. When gain is too small, slow the system down.

In general, the selection of parameters usually adopts experimental trial method, and the overall step is "first proportion, then integration, and finally differentiation". (1) tuning gain control: change the gain control effect from small to large, observe each response, until the response curve with fast response and small overshoot is obtained. (2) setting integral link: reduce the scale coefficient selected in step (1) to the original 50%~80%, adjust the zero again to make the integral effect from small to large, get a more satisfactory response by trial and error, and determine the relevant parameters of the ratio and integral. (3) if the dynamic process is not satisfactory after two steps above, the pole is set from small to large, and the proportion and zero are correspondingly changed to obtain satisfactory control effect and related parameters by repeated trial and error.

PWM_FLT_OFF (Low-pass Filter after PID Controller Enable/Disable)

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										PWM_ FLT_OFF					

Set whether the filter after PID controller is enabled or disabled.

Filter function is to remove noise generated in the filtering process, so PWM_FLT_OFF = 1 is generally set.

If phase margin is not large enough under the closed-loop frequency condition, in case of ringing, PWM_FLT_OFF = 1 can be set to improve the phase margin and prevent ringing.

Set Value	Filter after PID Controller
0	Enable
1	Disable

PWM_LPF_FC[2:0] (Cut-off Frequency of Low-pass Filter after PID Controller)

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							PWM_LPF_FC[2:0]								

Set the cut-off frequency of the filter after PID controller.

Lower cut-off frequency filter has stronger filtering effect and can achieve the effect of low noise.

Normally, set PWM_LPF_FC[2:0] = 0.

If phase margin is not large enough under the closed-loop frequency condition, in case of ringing, the cut-off frequency can be increased.

Set Value	Cut-off Frequency
0	900Hz
1	1300Hz
2	1600Hz
3	2000Hz
4	2600Hz
5	3200Hz
6	4000Hz
7	Prohibit

PWM_IRIS[2:0] (PWM Frequency of Iris Module Output)

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				PWM_IRIS[2:0]											

Set PWM frequency of Iris module.

Set Value	PWM Frequency(kHz)
0	26
1	31.25
2	62.5
3	93.75
4	125
5	150
6	187.5
7	210

DT_ADJ_IRIS[1:0] (Dead Time Setting of Iris Module Output)

Address			03h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		DT_ADJ_ IRIS[1:0]													

Set the total amount of dead time correction.

Set Value	Total amount of Dead Time Correction
0	Standard Correction
1	Standard Correction-1
2	Standard Correction-2
3	Not Correction

TGT_LPF_FC[3:0] (Iris Target Value Low-pass Filter Cut-off Frequency)

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
												TGT_LPF_FC[3:0]			

The cut-off frequency of low-pass filter is set before the Iris position information enters the PID system.

Lower cut-off frequency will cause the target value to change slowly, but will eliminate the audio error.

In general, the cut-off frequency should be lower than VD frequency, so that no step change appears. But there may be some delay.

Set Value	Cut-off Frequency
0	325Hz
1	650Hz
2	1300Hz

Set Value	Cut-off Frequency
7	80Hz
8	100Hz
9	125Hz

Set Value	Cut-off Frequency
3	2600Hz
4	40Hz
5	50Hz
6	63Hz

Set Value	Cut-off Frequency
10	160Hz
11	200Hz
12	250Hz
-	-

TGT_FLT_OFF (Iris Target Value Low-pass Filter Enable/Disable)

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											TGT_ FLT_OFF				

Whether low-pass filter is enabled or disabled before the Iris position information enters the PID system.

Set Value	Iris Target Value Filter
0	Enable
1	Disable

PID_INV (PID Controller Polarity)

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										PID_INV					

Set the PID controller polarity.

Set Value	PID Controller Polarity
0	Non-inverting
1	Inverting

START1[9:0] (Pulse 1 Start Position)

Address			06h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						START1[9:0]									

WIDTH1[11:0] (Pulse 1 Pulse Width)

Address			07h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				WIDTH1[11:0]											

P1EN (Pulse 1 Output)

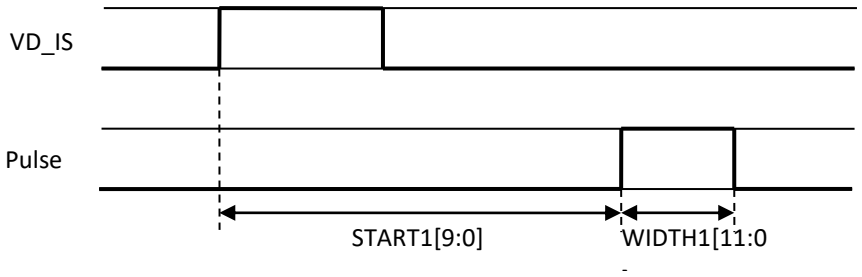
Address			07h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
P1EN															

START[9:0], WIDTH[11:0] and P1EN set pulse output for flashlight (pulse 1).

START1[9:0] sets the start time of pulse 1. Starting from the rising edge of the video field synchronous signal (VD_IS), until the set time is reached.

WIDTH1[11:0] sets the pulse width of pulse 1. Start counting synchronously at the end of the start time until the set time is reached. P1EN controls the output of pulse 1.

When any of START1[9:0], WIDTH1[11:0] and P1EN is "0", the pulse is not output.



Set Value	Cut-off Frequency
0	0
1	20.1μs
n	n×(68/3.375) μs
1023	20.56 ms

Set Value	Cut-off Frequency
0	0
1	1.19μs
n	n×(4/3.375) μs
4095	4.87 ms

START2[9:0] (Pulse 2 Start Position)

Address			08h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						START2[9:0]									

WIDTH2[5:0] (Pulse 2 Pulse Width)

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										WIDTH2[5:0]					

P2EN (Pulse 2 Output)

Address			09h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
P2EN															

START2[9:0], WIDTH2[5:0] and P2EN set the pulse output (pulse 2) for the Iris to completely shut off.

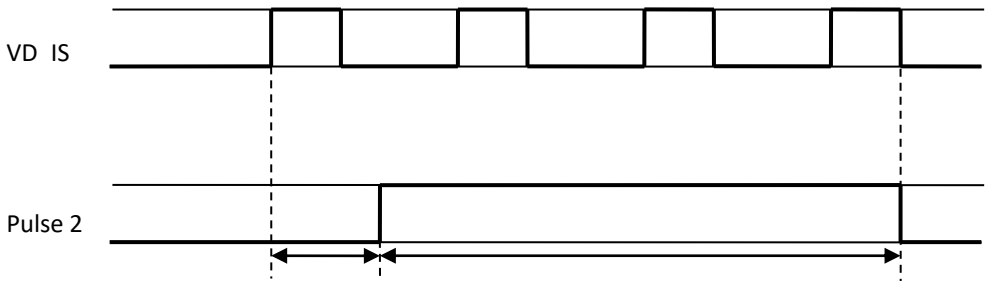
Note: no pulse 2 is allowed in PID operation.

START2[9:0] sets the start time of pulse 2. Starting from the rising edge of the video field synchronous signal (VD_IS), until the set time is reached.

WIDTH2[5:0] sets the pulse width of pulse 2. This setting is executed after the start time count has finished, and rising edge appears. After counting the number of rising edges of VD_IS, the falling edge of VD_IS ends. After the specified number of times of rising edge of VD_IS is counted, the output of pulse 2 ends at the falling edge of VD_IS.

P2EN controls the output of pulse 2.

When any of START2[9:0], WIDTH2[5:0] and P2EN is "0", the pulse is not output. Meanwhile, START2 and WIDTH2 are not updated while counting.



Set Value	Cut-off Frequency
0	0
1	20.1μs
n	n × (68/3.375) μs
1023	20.56 ms

Set Value	Cut-off Frequency
0	0
1	VD_IS 1 Count
63	VD_IS 63 Count
n	VD_IS n Count

TGT_IN_TEST[9:0] (Iris Module Output Duty Direct Specified Value)

Address			0Ah			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						TGT_IN_TEST[9:0]									

The duty cycle of the iris module output driver signal can be directly controlled. DUTY_TEST must be "1" to enable the algorithm.

TGT_IN_TEST[9] sets the rotation direction of the iris output module. TGT_IN_TEST[8:0] sets the driver duty cycle for the iris output module.

Method of Calculating Duty Cycle

The driver signal duty cycle is related to the set value of PWM_IRIS[2:0].

a is calculated by a = {TGT_IN_TEST[8:1],2 'b00,TGT_IN_TEST[0]}(binary 11bit).

B is related to PWM_IRIS[2:0] as shown in the table above.

The duty cycle is obtained by calculating a/b. If a/b is >, 1, the duty cycle is 100%.

Example: when TGT_IN_TEST[8:0] = 80h, PWM_IRIS[2:0] = 2,

a = {40h, 2 'b00', 1 'b0} = 200h ; a/b = 200h/862 =0.59

TGT_IN_TEST[9]	Drive Direction
0	Current Direction OUTE2→OUTE1
1	Current Direction OUTE1→OUTE2

PWM_IRIS[2:0]	b
0	2046
1	1726
2	862
3	574
4	430
5	350
6	286
7	254

TGT_IN_TEST[8:0]	Drive Signal Duty Cycle
000h	0%
1FFh	100%
N	a/b

DUTY_TEST (Iris Module Output Duty Enable)

Address			0Ah			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					DUTY_TEST										

Duty cycle of iris drive can be directly controlled. This algorithm is enabled when DUTY_TEST is set to "1".

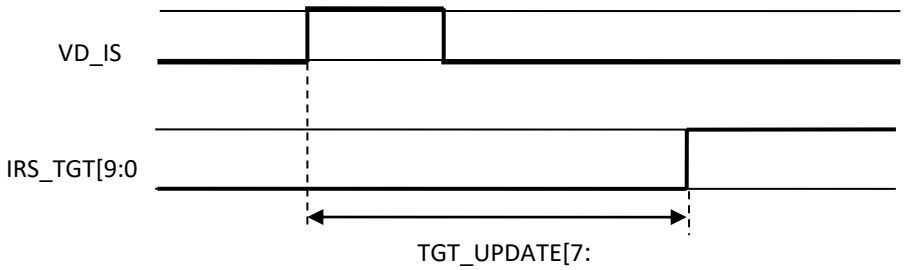
Set Value	Algorithm Enable
0	Disable
1	Enable

TGT_UPDATE[7:0] (IRS_TGT Update Delay)

Address			0Eh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TGT_UPDATE[7:0]							

TGT_UPDATE[7:0] adjusts the update time of IRS_TGT[9:0].

IRS_TGT[9:0] is updated after the rising edge of VD_IS as shown in the figure below.



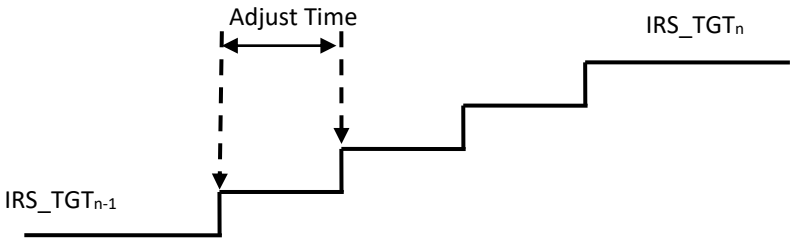
Set Value	Update Delay
0	0
1	80μs
n	n × (270/3.375)μs
255	20.4ms

AVE_SPEED[4:0] (Iris Target Moving Average Speed)

Address			0Eh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			AVE_SPEED[4:0]												

AVE_SPEED[4:0] sets the moving average shift time for iris target.

Set Value	Update Delay
0	2μs
1	152μs
n	(n×512 + 1)/3.375μs
31	4.703 ms

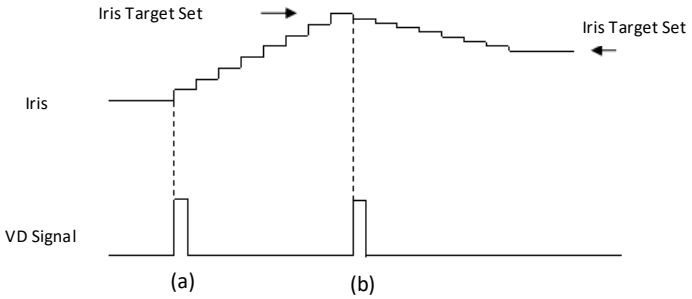


Examples:

Set AVE_SPEED[4:0] so that the update speed of data is same as the period of VD signal.

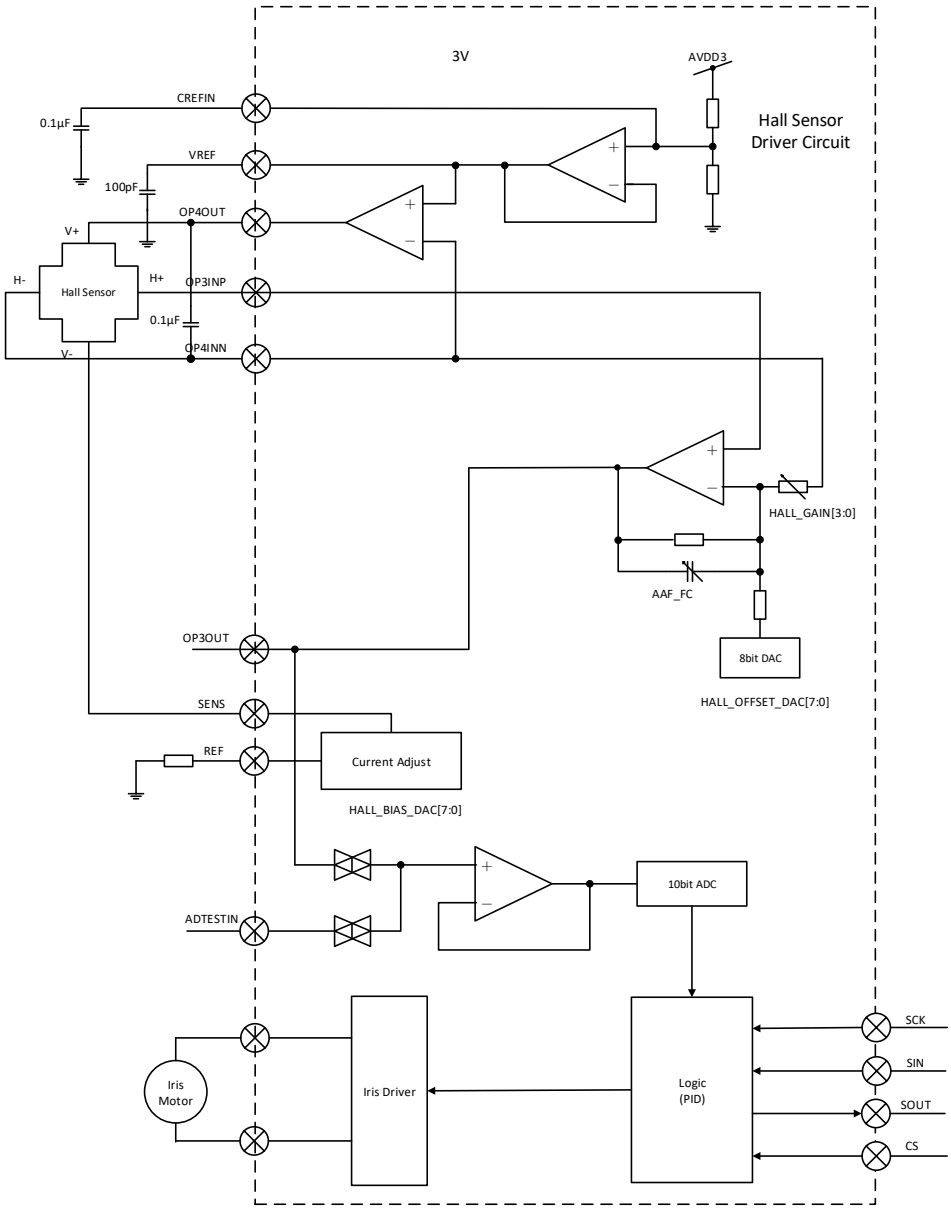
If VD = 60Hz, the time of each step is 1/ (60Hz) / 8 = 2.08ms in the case of 8 steps adjustment.

Refer to the table, the time of each step can be set to 2.12ms according to the value of AVE_SPEED[4:0], so the iris is changed every 17.0ms.



3.3 Iris Control Hall Sensor

Block Diagram



HALL_BIAS_DAC[7:0 (Bias Current of Hall Element)

Address			04h			Initial Value		0							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								HALL_BIAS_DAC[7:0]							

Set drive current of hall signal. The value depends on the external resistance of the REF port.

The drive current of SENS port can be calculated by the following equation:

ISENS = REF Port Voltage / RREF×(Set Value / 8)

REF Port Voltage= 1.22V (Typical Value).

HALL_OFFSET_DAC[7:0] (Offset Adjustment of Hall Element Output Amplifier)

Address			04h			Initial Value		0							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HALL_OFFSET_DAC[7:0]															

Compensation value setting for hall output amplifier.

Set Value	Total Amount of Compensation
0~255	VDDA / 256 ×(Set Value -128)

The bias current and bias adjustment methods are as follows:

1) Bias current of Hall element is set.

2) Once the offset voltage is set to 0 (Set Value: 80h), output OP3OUT is adjusted (feedback to a 10bit ADC).

a) The adjustment of hall gain (HALL_GAIN[3:0]) makes the output of OP3OUT close to the target range in the range of iris fully open and completely closed.

For example: when the target value VDDD = 3.0v, fully open = 0.2V, fully closed = 2.8V;

Hall gain (HALL_GAIN[3:0]) is adjusted to make the OP3OUT port output range close to 2.8V - 0.2V= 2.6V.

b) Bias current is adjusted so that the output range is close to the target range.

c) Offset voltage is adjusted so that the output of OP3OUT is close to the target value range.

b and c can be executed separately.

HALL_GAIN[3:0] (Hall Element Output Amplifier Gain)

Address			05h			Initial Value		0							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				HALL_GAIN[3:0]											

The gain setting of hall output amplifier is as follows:

Set Value	Gain	Set Value	Gain
0	21.9	8	58.0
1	26.4	9	62.6
2	31.0	10	67.1
3	35.5	11	71.7
4	40.1	12	76.3
5	44.6	13	80.8
6	49.2	14	85.4
7	53.7	15	89.9

AAF_FC (Cut-off Frequency of Hall Element Output Amplifier)

Address			05h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			AAF_FC												

The cut-off frequency of hall amplifier is as follows:

Set Value	Cut-off Frequency (kHz)
0	6.85
1	20.0

OCPIris_dly[1:0] (Iris Module Overcurrent Judge Threshold)

Address			0Bh			Initial Value			2						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
														OCPIris_dly[1:0]	

Set Value	Overcurrent Event Judge (μs)
0	Overcurrnt Detection Off
1	3
2 (Initial Value)	5
3	7

OCP1 / 2 / 3/ 4/ 5_dly configurations are same.

PDWNB (Iris Module Enable)

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					PDWNB										

PDWNB sets the enable of entire Iris control circuit.

Set Value	Iris Control
0	Disable
1	Enable

ASWMODE[1:0] (ADTESTIN Pin Connection Selection)

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											ASWMODE[1:0]				

ASWMODE[1:0] sets the test mode of Iris ADC.

Set Value	Iris ADC Mode
0	Normal mode
1	Normal mode
2	Test mode
3	-

By setting ASWMODE[1:0] = 2, the open-loop frequency response can be tested.

See the next page for more details.

ADC_TEST (ADC Test Mode Selection)

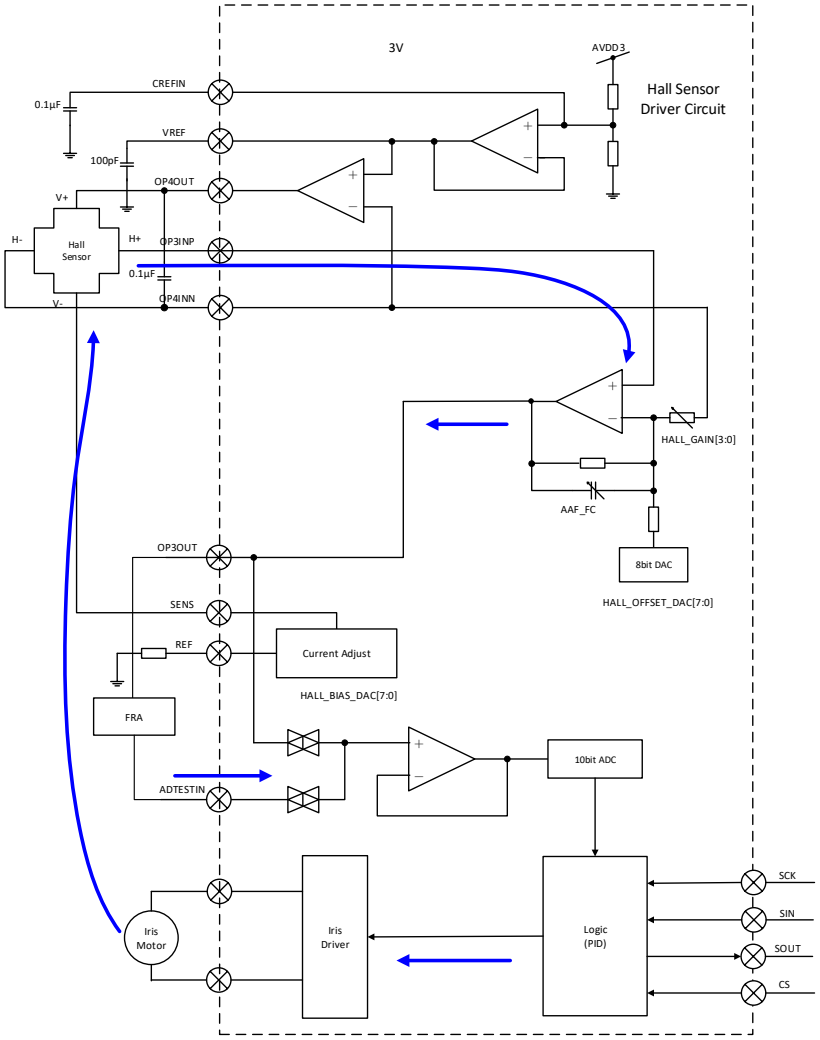
Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				ADC_TEST											

ADC_TEST is used to select ADC functional test.

Do not set ADC_TEST = 1.

Set Value	Algorithm
0	Normal
1	Iris ADC Function Test

Method of Testing Open-Loop Frequency Response



FRA: Frequency Response Analyzer

1) Set ASWMODE[1:0] = 2.

2) Connect FRA between OP3OUT and ADTESTIN.

3) Set PID parameters.

4) Test open-loop frequency response.

PID_CLIP[3:0] (PID Maximum Duty Cycle Setting)

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PID_CLIP[3:0]															

PID_CLIP[3:0] sets the maximum duty cycle for the Iris PWM driver.

Set Value	Maximum Duty Cycle
0	100%
1	93.75%
n	(100 - n × 6.25)%
15	6.25%

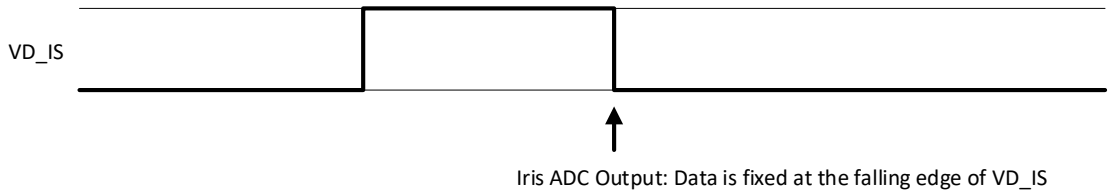
IRSAD[9:0] (ADC Value Output)

Address			0Ch			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						IRSAD[9:0]									

IRSAD[9:0] is a read-only register and used to receive the output of iris ADC.

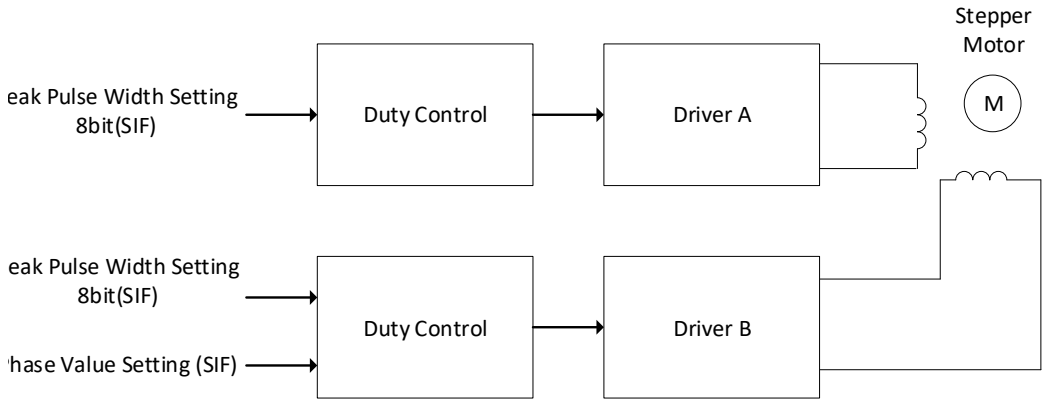
This register can only be used when VD_IS is low.

(IC updates data when VD_IS = "H". If IRSAD[9:0] is used when VD_IS = "H", the read data is not correct.)



4. Stepper Motor Microstep

4.1 Block Diagram



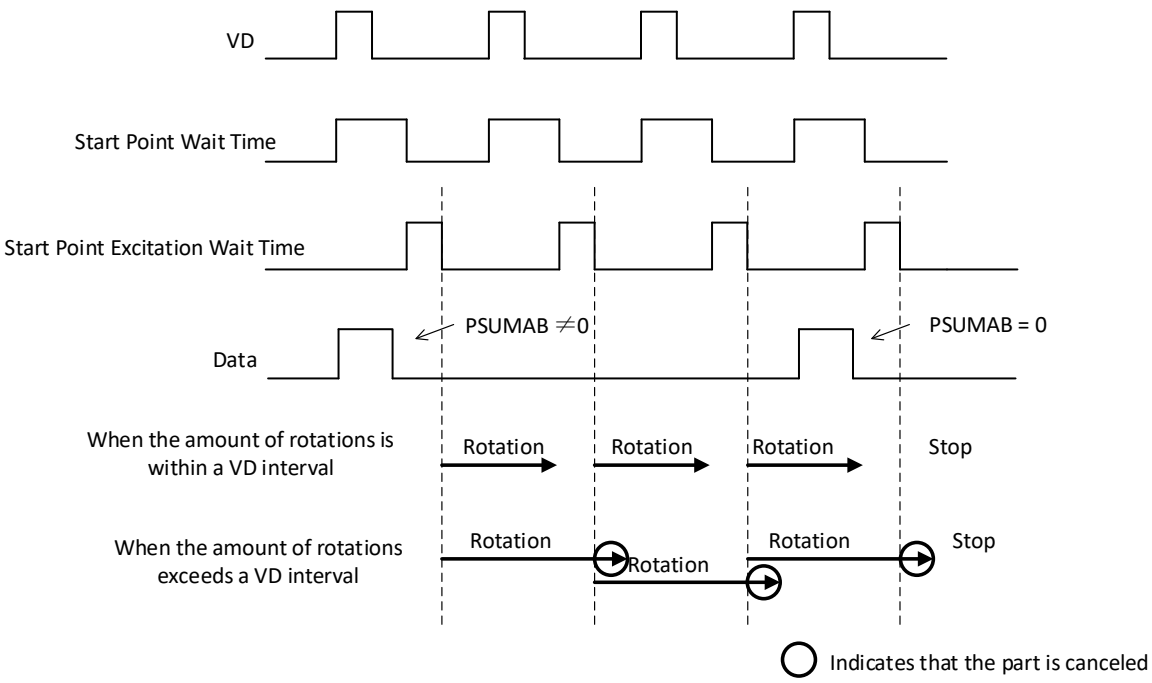
This module is a stepper motor driver for focusing and magnifying. The following settings can be used to perform a series of controls. (The following description is for α motor: drive A/B. Drive C/D, E/F, G/H, I/J performs the same algorithm as α motor.) Drive I/J can be multiplexed as dual-channel DC motor by DC_EN in 20h.

Main setting parameters:

1. MICROAB[1:0]: Microstep can be set to 64, 128 and 256.
2. PHMODAB[5:0]: The phase difference between driver A and driver B is on the basis of 90 degree, and can be adjusted from -22.5 degree to +21.8 degree.
3. DT2A[7:0]: Update data time setting.
4. PPWA[7:0], PPWB[7:0]: Set the load current of driver A/B independently.
5. PSUMAB[11:0]: Stepper Motor Step Number.
6. INTCTAB[15:0]: Motor rotation speed is set. The rotation speed is regardless of microstep mode of sine wave.
7. PWMMODEAB[4:0], PWMRESAB[1:0]: PWM frequency of driver output is set.
8. FZTEST_1[4:0]: Set output selection for PLS1.
9. Overcurrent.
10. Other.

4.2 Setup Timing of the Relevant Settings

The setup timing and related time are shown below.



Because the settings of 27h to 2Bh, 2Ch to 30h, 31h to 35h, 36h to3Ah are same as 22h to 26h, the description for 27h to3Ah can be omitted. If the relevant register is refreshed, one setting load refresh is implemented for each VD cycle. When the same setting is executed with more than 2 VD pulses, it is not necessary to write register data at each VD pulse.

DT1[7:0] (Start Point Wait Time, Address 20h)

Update data time settings. Five step channels share same settings. This must be set after the system hardware reset (39 pin RSTB: low → high), before starting the excitation and driving motor (DT1 ends).

Since this setting is updated every time a VD pulse comes in, it is not necessary to write within the start point wait time.

DT2A[7:0] (Start Point Excitation Wait Time, Address 22h)

Update data time Settings. After reset (39 pin RSTB: low → high), it is necessary to be executed before starting excitation and driving motor (DT1 ends).

MICROAB[1:0] (Sine Wave Division Number, Address 22h)

Sets division number of sine wave. This setting does not change the rotation number and rotation speed.

This is set only when the rotation speed is not up to the demand. After reset (39 pin RSTB: low →high), setting effective.

PHMODAB[5:0] (Phase Correction, Address 22h)

By correcting the phase difference between coils A and B, the driver produces less noise.The appropriate phase correction must be based on the rotation direction and speed of the motor. This setting needs change with the rotation direction (CCWCWAB) or the rotation speed (INTCTABA).

PPWA[7:0], PPWB[7:0] (Peak Pulse Width, Address 23h)

Set the PWM maximum duty cycle. Settings need to be executed before starting excitation and driving motor (DT1 ends).

PSUMAB[11:0] (Stepper Motor Step Number, Address 24h)

The rotation number of the motor is set within 1 VD time interval.

The number of times the motor is set for each VD pulse input. Therefore, setting the number to "0" can stop the rotation of the motor.

When the total number of rotations exceeds the time of 1 VD pulse, the exceeded part will be canceled.

CCWCWAB (Rotation Direction, Address 24h)

Motor rotation direction setting. Just set it before selecting the rotation direction.

BRAKEAB (Motor Brake, Address 24h)

Set the current to 0 when braking. This setting is generally used to stop the motor immediately because it is difficult to obtain the final position of the motor when this setting is performed.

ENDISAB (Motor Enable/Disable, Address 24h)

Set the motor enable. When set to disable, the motor pin outputs high impedance state, and should not be set to disable while the motor is rotating.

LEDA (LED Setting, Address 24h)

LED on/off settings. It is set at the falling edge of CS. it can be considered independent of motor drive, and can achieve independent settings of on/off.

INTCTAB[15:0] (Pulse Cycle, Address 25h)

Pulse cycle setting. The rotation speed depends on this setting.

TESTEN2_1 (Motor Channel Test Output Enable, Address 26h)

PLS1 output enable. It is used with TESTEN1.

FZTEST_1[4:0] (PLS1 Pin Output Signal Selection, Address 26h)

PLS1 pin output signal selection.

OCP1_dly[1:0] (Iris Module Overcurrent Judge Time, Address 26h)

Overcurrent judge time setting. It is same as OCPIris_dly[1:0].

PWMMODEAB[4:0], PWMRESAB[1:0] (Microstep Output PWM Frequency, Address 26h)

Set the PWM frequency of the microstep output. It is necessary to be executed before starting excitation and driving motor (DT1 ends).

4.3 How to adjust the register value when the stepper motor is driven by microstep

In order to control the lens, it is required to set the number and speed of motor rotation at each VD. The registers for rotation times and speed of the relevant settings are:

INTCTxx[15:0]: Set the time of each step (corresponding to rotation speed)

PSUMxx[11:0]: Total rotation steps at each VD

When the motor is continuously driven in a continuous VD period, the continuous rotation time needs to be set to adapt to the VD period.

The following is how to calculate INTCTxx[15:0] and PSUMxx[11:0] when the motor is rotating:

1) Calculate INTCTxx[15:0] (determine the motor rotation speed)

$$INTCTxx[15:0] \times 768 = OSCIN\ Frequency/Rotation\ Frequency$$

2) PSUMxx[11:0] was calculated by INCTxx[15:0]. Can't just look at the value of PSUMxx[11:0].

When the following equation holds, the continuous rotation time and VD time are the same, and the motor achieves smooth rotation.

$$INTCTxx[15:0] \times PSUMxx[11:0] \times 24 = OSCIN\ Frequency/VD\ Frequency$$

3) INTCTxx[15:0] is recalculated from the above formula after the setting of PSUMxx[11:0] is completed.

For example, OSCIN Frequency = 27MHz, VD Frequency = 60Hz

Calculate PSUMxx[11:0] and INTCTxx[15:0] to rotate motor at 800pps (1-2 phase)

800pps is equal to 100Hz, so

$$INTCTxx[15:0] = 27MHz / (100Hz \times 768) = 352$$

Corresponding:

$$PSUMxx[11:0] = 1/(60Hz) \times 27MHz/ (352 \times 24) = 53$$

Recalculate INTCTxx[15:0]:

$$INTCTxx[15:0] = 1/(60Hz) \times 27MHz/ (53 \times 24) = 354$$

More details can be found on pages 46 and 47.

If the left side of the equation in 2) is smaller than the right side, the rotation time will be smaller than VD period and will cause discontinuous rotation. On the contrary, the rotation beyond VD period will be canceled.

4.4 Register Details

DT1[7:0] (Start Point Wait Time)

Address			20h			Initial Value			0Ah						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT1[7:0]							

DT1[7:0] sets the delay time of data written to the system (start point wait time) .

The motor can be activated precisely after the start point wait time is flipped from "1" to "0". The start point wait time is calculated from the rising edge of the video synchronous signal (VD_FZ).

Because the start delay time is mainly used to wait for the serial data to be written. The register value should be set to greater than "0". If it is "0", the corresponding data cannot be updated.

Refer to page 19 for the relationship between VD_FZ and start point wait time.

DT1	Start Point Wait Time
0	Prohibit
1	18.96μs
255	4.83ms
n	n × 512/27MHz

MICROAB[1:0] (α Motor Sine Wave Division Number)

Address			22h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MICROAB[1:0]															

MICROAB[]1:0] sets sine wave division number of α motor.

The wave for 64 divisions is shown in page 48.

MICROAB[1:0]	Division Number
00	256
01	256
10	128
11	64

DT2A[7:0] (α Motor Start Point Excitation Wait Time)

Address			22h			Initial Value			03h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2A[7:0]							

DT2A[7:0] sets the wait delay time before α motor starts to rotate.

The motor starts to rotate after the start point excitation wait time is flipped from "1" to "0". The start point excitation wait time starts to calculate at the end of start point wait time.

This signal is a separate delay for channel AB. The register value should be set to greater than "0". If it is "0", the corresponding data cannot be updated.

Refer to page 19 for the relationship between VD_FZ and start point excitation wait time.

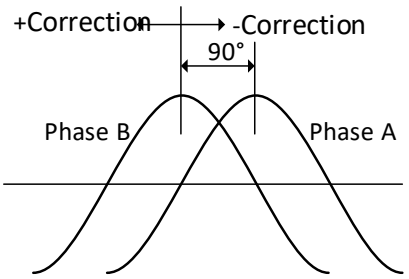
DT1	Start Point Excitation Wait Time
0	Prohibit
1	18.96μs
255	4.83ms
n	n × 512/27MHz

PHMODAB[5:0] (α Motor Phase Correction)

Address			22h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODAB[5:0]													

The current phase difference of α motor is set by PHMODAB[5:0]. The default value is 90° and set 1 unit to 0.7° . Meanwhile, the data can be subject to positive and negative deviation.

PHMODAB	Phase Correction Number
000000	± 0°
000001	+ 0.7°
011111	+ 21.80°
100000	- 22.50°
111111	- 0.7°
Damping Unit	360° /512 = 0.70°



Phase difference between the stepper motor coils is generally 90 degree. However, due to different motors or process deviations, the phase difference will also be shifted by 90 degree. Therefore, even if the phase difference of the drive waveform current is 90 degree, but the motor itself is not 90 degree difference, it will produce torque ripple, and the noise still exists.

The main purpose of this setting is to reduce the torque ripple caused by motor changes.

PPWA[7:0] (Driver A Peak Pulse Width)

PPWB[7:0] (Driver B Peak Pulse Width)

Address			23h			Initial Value			0,0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWB[7:0]								PPWA[7:0]							

Maximum duty cycle of the PWM wave is set by PPWA[7:0] to PPWD[7:0], which determines the position of the peak output current from driver A to D.

The maximum duty cycle is calculated by the following equation:

Maximum Duty Cycle = PPWx/ (PWMMODE × 8)

When PPWx = 0, the coil current is 0.

For example,

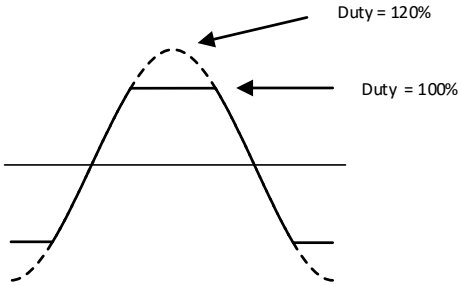
when PPWA[7:0] = 200 and PWMMODE[4:0] = 28, the maximum duty cycle is 200 / (28 × 8) = 0.89.

According to the values of PWMMODE and PPWx, the maximum duty cycle may exceed 100%.

Of course, the duty cycle in PWM cannot exceed 100%, and the peak point of sine wave will be truncated as shown in the following figure.

For example, when PWMMODE = 10, PPWx = 96, maximum duty cycle = 90/ (10 × 8) = 120%.

The waveform of the target current is shown as follows:



PSUMAB[11:0] (α Motor Step Number)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				PSUMAB[11:0]											

PSUMAB[11:0] sets the total step number of α motor.

If need to stop the motor, set PSUMXX[11:0]=0.

Register Value	Total Step Number		
	64 Microstep Mode	128 Microstep Mode	256 Microstep Mode
0	0	0	0
1	2	4	8
255	510	1020	2040
n	2n	4n	8n

As long as the maximum duty cycle of PWM wave is not set as "0", when PSUMxx[11:0]=0, the motor can be kept in the state of release.

An example to see the meaning of setting:

When PSUMAB[11:0]=8 is set, run 16 steps in 64 microstep mode, i.e. 16/64=1/4 sine wave cycle. Similarly, in 128 and 256 microstep modes, it is also a quarter of sine wave cycle.

LED Driver

LEDA (LED A Setting)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LEDA															

LEDA sets output enable of LED A.

Set Value	LED Output
0	Off
1	On

CCWCWAB (α Motor Rotation Direction)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			CCWCWAB												

CCWCWAB sets the rotation direction of α motor.

Direction definition:

Set Value	Motor Rotation Direction
0	Forward
1	Reverse

BRAKEAB (α Motor Brake)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		BRAKEAB													

BRAKEAB and BRAKECD set the brake mode of α motor and β motor.

Set Value	A Motor Brake
0	Normal State
1	Brake State

Both of upper-side PMOSs of H bridge turn on in brake mode. The brake mode cannot be used during normal operation and can only be used during emergency shutdown. It is recommended to be used under abnormal condition.

ENDISAB (α Motor Enable/Disable)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	ENDISAB														

ENDISAB sets the output control of α motor.

When ENDISxx=0, output high impedance state. However, the internal excitation position counter at ENDISxx = 0 still keeps counting. Therefore, when want to stop the motor under normal condition, set PSUMxx[11:0] = 0 instead of ENDISxx = 0.

Set Value	Motor Output State
0	Output Off (Hi-Z)
1	Output On

INTCTAB[15:0] (α Motor Step Cycle)

Address			25h			Initial Value			80h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTAB[15:0]															

INTCTAB[15:0] sets a step cycle of α motor.

Register Value	Total Step Number		
	64 Microstep Mode	128 Microstep Mode	256 Microstep Mode
0	0	0	0
1	444ns	222ns	111ns
n	12n/27MHz	6n/27MHz	3n/27MHz

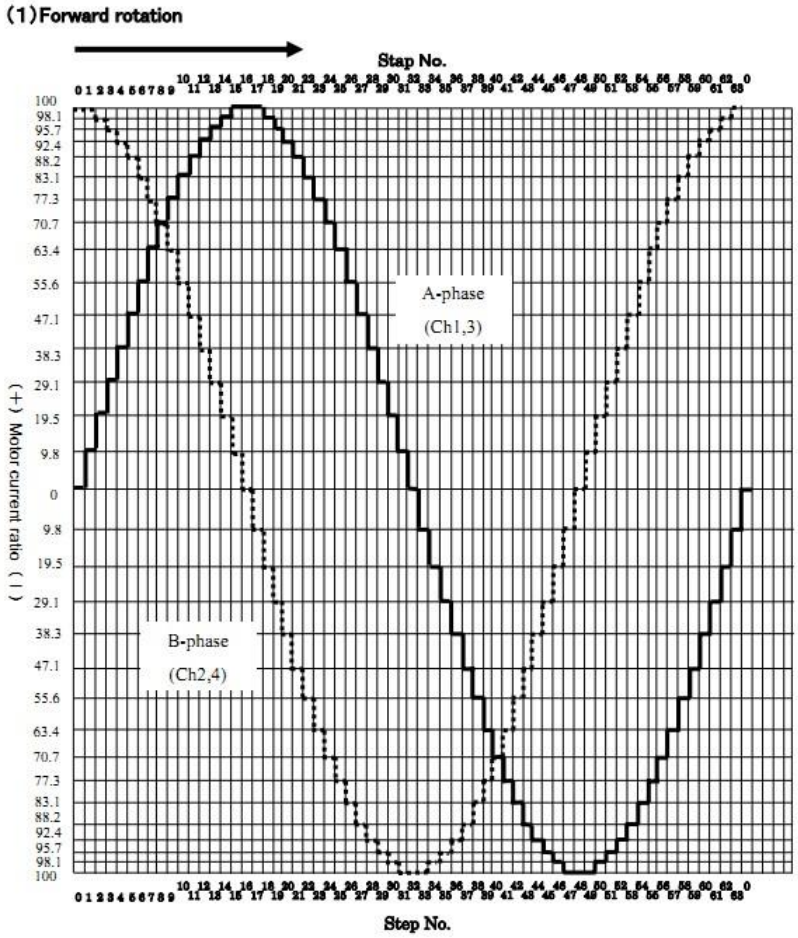
When INTCTAB[15:0]=0, as long as PWM maximum duty cycle is not 0, the motor will remain in the release state.

Examples: When INTCTAB[15:0]=400, each step cycle in 64 microstep:

$$12\times400/27MHz=0.178ms$$

Therefore, the period of each sine wave is 11.4ms (87.9Hz). Similarly, this is the same for 128 microstep and 256 microstep.

Stepper Motor Driver (64 Microstep Current Curve)



5. Test Signal

TESTEN1 (Test Setting 1)

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN1							

TESTEN2 (Test Setting 2)

Address			26h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TESTEN2															

FZTEST[4:0] (Test Signal Output Setting)

Address			26h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	FZTEST[4:0]														

FZTEST_X[4:0] selects the test signal of PLSX output.

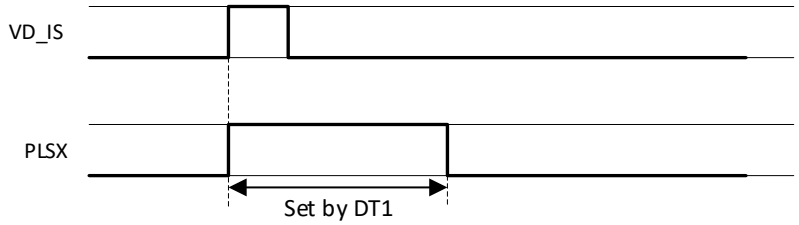
TESTEN1 and TESTEN2 need to be set to "1" to allow the test signal output.

The following table is the output setting signal when specified setting.

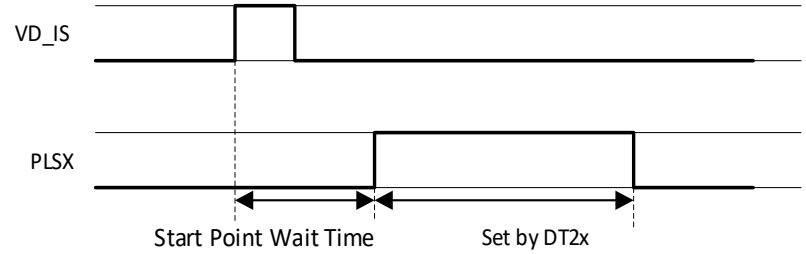
Set Value	Step Cycle	Description
	PLS1	
0	/	Default State
1	Start Point Wait Time	"H" Bridge Output during Start Point Wait Time
2	Start Point Excitation Wait Time A	"H" Bridge Output during Start Point Excitation Wait Time
3	ENDISAB	ENDISxx Setting
4	CCWCWAB	CCWCWxx Setting
5	Monitor Output Pulse A	"H"/"L"changes at the speed of 64 microstep when motor rotates
6	PWM Cycle Monitoring	Motor Output PWM Periodic Signal
7	Complete Pulse Output of Channel A	"H" bridge output when motor rotates
9	ADC System Clock	Monitor Operation State of ADC (Only Output by PLS_1 and PLS_2)

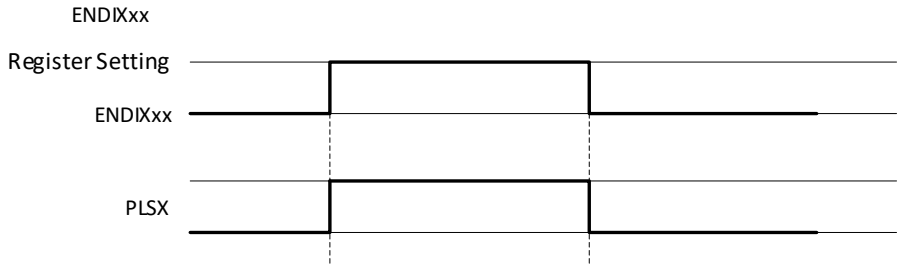
The relevant waveform is described as follows:

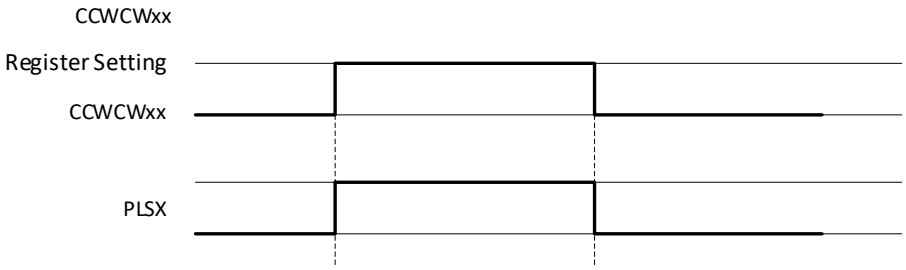
Start Point Wait Time

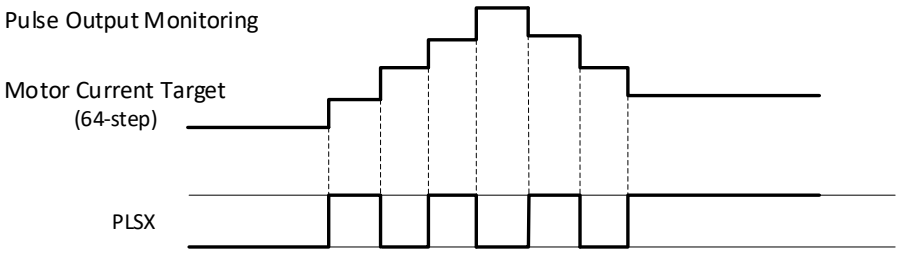


Start Point Excitation Wait Time



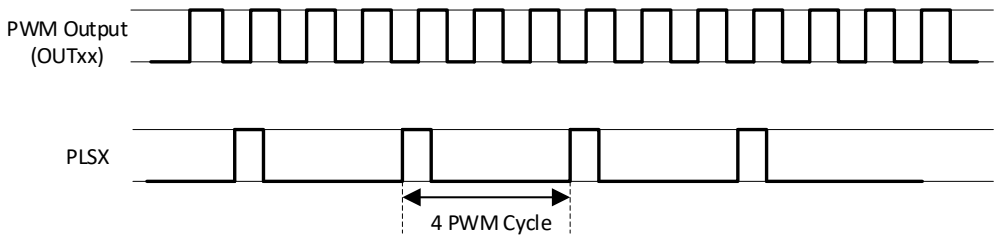




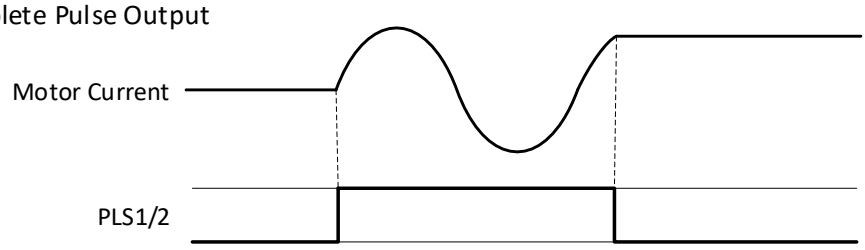


For 128-step and 256-step, change every 2 and 4 steps respectively

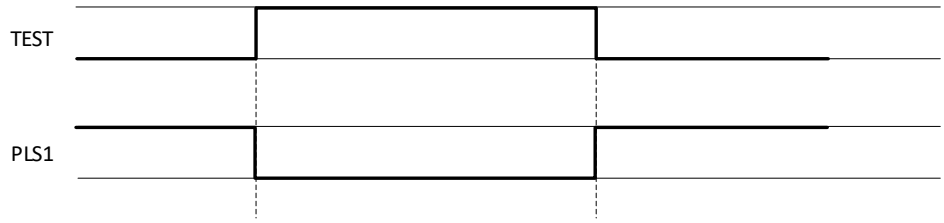
PWM Cycle Monitoring



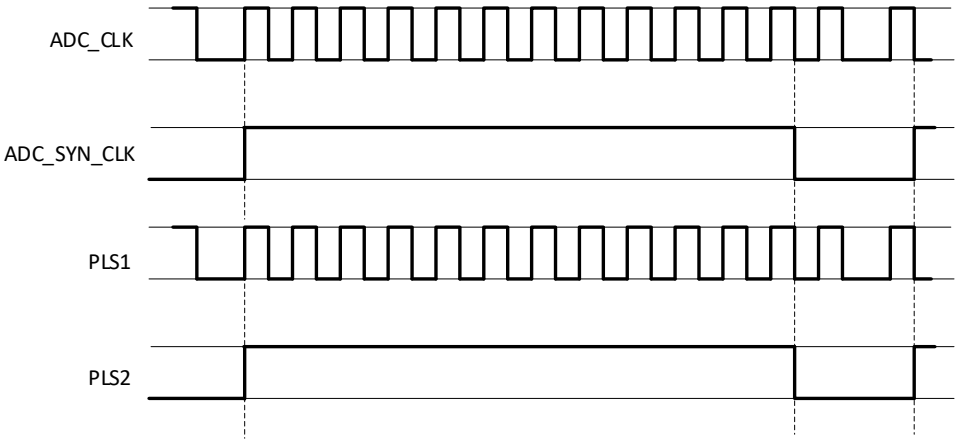
Complete Pulse Output



TEST



ADC Monitoring



OCP1_dly[1:0] (Iris Module Overcurrent Judge Threshold)

Address			26h			Initial Value			2						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						OCP1_dly[1:0]									

Set Value	Overcurrent Judge Time (μs)
0	Off
1	3
2 (Initial Value)	5
3	7

PWMMODEAB[4:0] (Microstep Output PWM Frequency)

Address			26h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											PWMMODE[4:0]				

PWMRESAB[1:0] (Microstep Output PWM Resolution)

Address			26h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									PWMRES[1:0]						

PWMMODEAB[4:0] sets the microstep output PWM frequency by setting the frequency division of system clock OSCIN.

PWMMODEAB[4:0] can be set in the range of 1 to 31. The PWM frequency is the same when PWMMODEAB = 0 and PWMMODEAB= 1.

PWMRESAB[1:0] sets the resolution of frequency division determined by PWMMODEAB[4:0].

The PWM frequency is calculated by the following formula:

$$\text{PWM Frequency} = \text{OSCIN Frequency} / ((\text{PWMMODEAB} \times 2^3) \times 2^{\text{PWMRESAB}})$$

When OSCIN=27MHz, the PWM frequency is shown in the following table.

PWMMODEAB	PWMRESAB			PWMMODEAB	PWMRESAB		
	0	1	2		0	1	2
1	3375.0	1687.5	843.8	17	198.5	99.3	49.6
2	1687.5	843.8	421.9	18	187.5	93.8	46.9
3	1125.0	526.5	281.3	19	177.6	88.8	44.4
4	843.8	421.9	210.9	20	168.8	84.4	42.2
5	675.0	337.5	168.8	21	160.7	80.4	40.2
6	526.5	281.3	140.6	22	153.4	76.7	38.4
7	482.1	241.1	120.5	23	146.7	73.4	36.7
8	421.9	210.9	105.5	24	140.6	70.3	35.2
9	375.0	187.5	93.8	25	135.0	67.5	33.8
10	337.5	168.8	84.4	26	129.8	64.9	32.5
11	306.8	153.4	76.7	27	125.0	62.5	31.3
12	281.3	140.6	70.3	28	120.5	60.3	30.1
13	259.6	129.8	64.9	29	116.4	58.2	29.1
14	241.1	120.5	60.3	30	112.5	56.3	28.1
15	225.0	112.5	56.3	31	108.9	54.4	27.2
16	210.9	105.5	52.7				

(kHz)

DC_EN I/J 9Driver Multiplexed as DC Channel Enable)

Address			20h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DC_EN															

After DC_EN is enabled, 3Bh and 3Ch can control DC channel A and B respectively. Because setting items are same, only explain A channel as follows.

DC_CTL_A (Drive State Control for DC Motor A)

Address			3Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				DC_CTL_A[1:0]											

By DC_EX_EN, address 20h, external pin INxA, INxB control are switched. This setting is effective for dual-channel DC motor.

DC_EX_EN (DC Motor Drive State External Control Enable)

Address			20h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	DC_EX_EN														

D11/INxA	D10/INxB	Drive State
0	0	Hi-Z (Initial Value)
0	1	Forward
1	0	Reverse
1	1	Brake

DCA_PWM_Freq[1:0] (PWM Frequency Control for DC Motor A)

Address			3Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						DCA_PWM_ Freq[1:0]									

D1	D0	Chopping Frequency
0	0	OSCIN / 128
0	1	OSCIN / 256
1	0	OSCIN / 512
1	1	OSCIN / 1024

Note: OSCIN is the clock frequency provided for main logic.

DCA_PWM_Duty[6:0] (Duty Control for DC Motor A)

Address			3Bh			Initial Value			40h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									DCA_PWM_Duty[6:0]						

D6	D5	D4	D3	D2	D1	D0	PWM Duty
0	0	0	0	0	0	0	1/128 ×100%
0	0	0	0	0	0	1	2/128 ×100%
~							~
1	1	1	1	1	1	1	128/128 ×100%

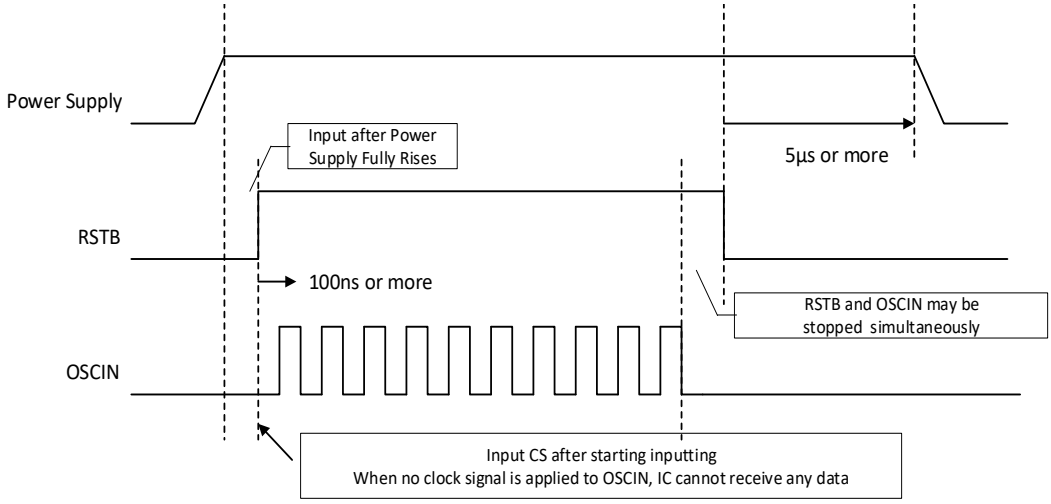
Error Indication Register

Address			3Eh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TSD_ Clr		OCPIr is_Clr	OCP5 _Clr	OCP4 _Clr	OCP3 _Clr	OCP2 _Clr	OCP1 _Clr

Latch/clear for error indication signal. When in abnormal operation (for example, motor stops midway), read 0x3E and determine abnormal type. After abnormal state is removed, write 1 to corresponding position and clear the latch and recover operation.

Start/Stop Timing

The start/stop timing of power signal, RSTB and OSCIN are shown in the following figure:



Input Capacitance of Input Pin

The capacitance of input pin is 10pF or less.

OSCIN and VD Signal Timing

Once VD signal (VD_FX or VD_IS input) is synchronized with OSCIN,VD signal and OSCIN signal have no constraint on input timing.

Power-down Mode

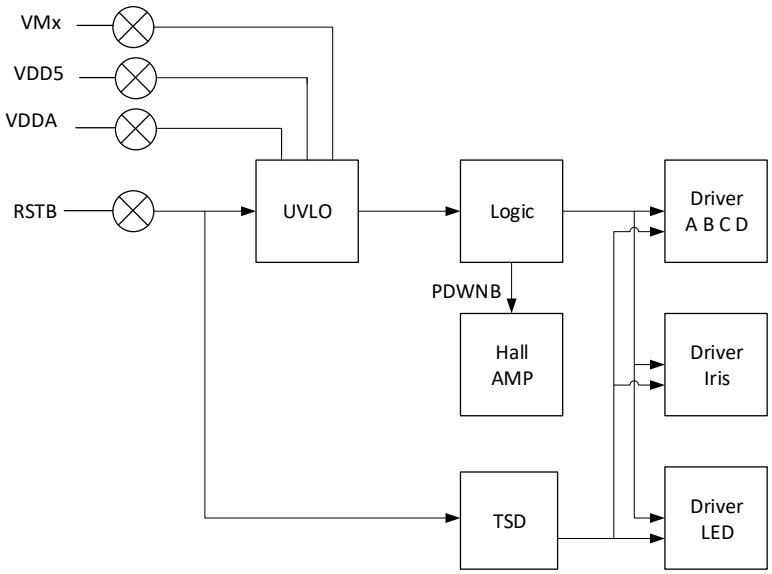
When PDWNB=0, power-down mode is set. In power-down mode, the circuit in the iris analog part stops working (the motor driver is not affected). When only the motor driver is in use, setting PDWNB to "0" can reduce power dissipation.

In power-down mode, the operation of related pin is as follows:

Pin	Operation
Related Input Pin	Grounding
Related Output Pin	Float
CREFIN	Float
REF	Float

6. Reset/Protection Circuit

The following figure shows the relationship between RSTB, UVLO, TSD and other circuits.

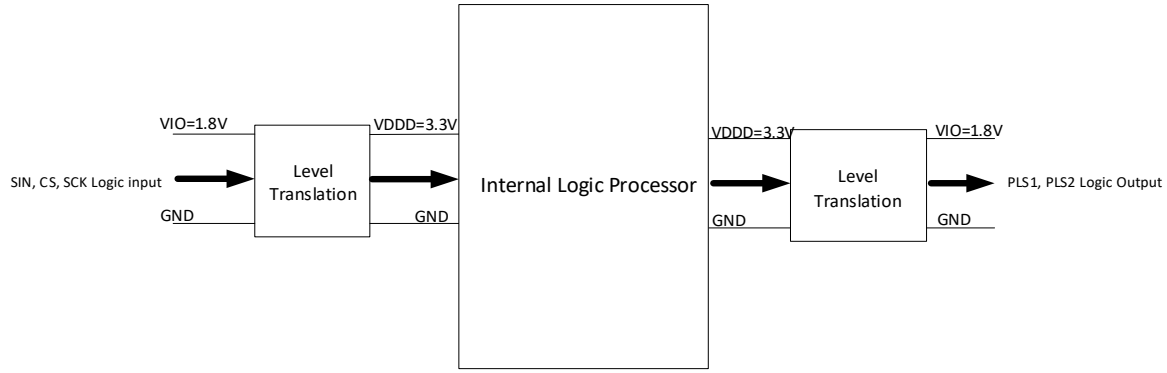


The corresponding specifications are shown in the following table:

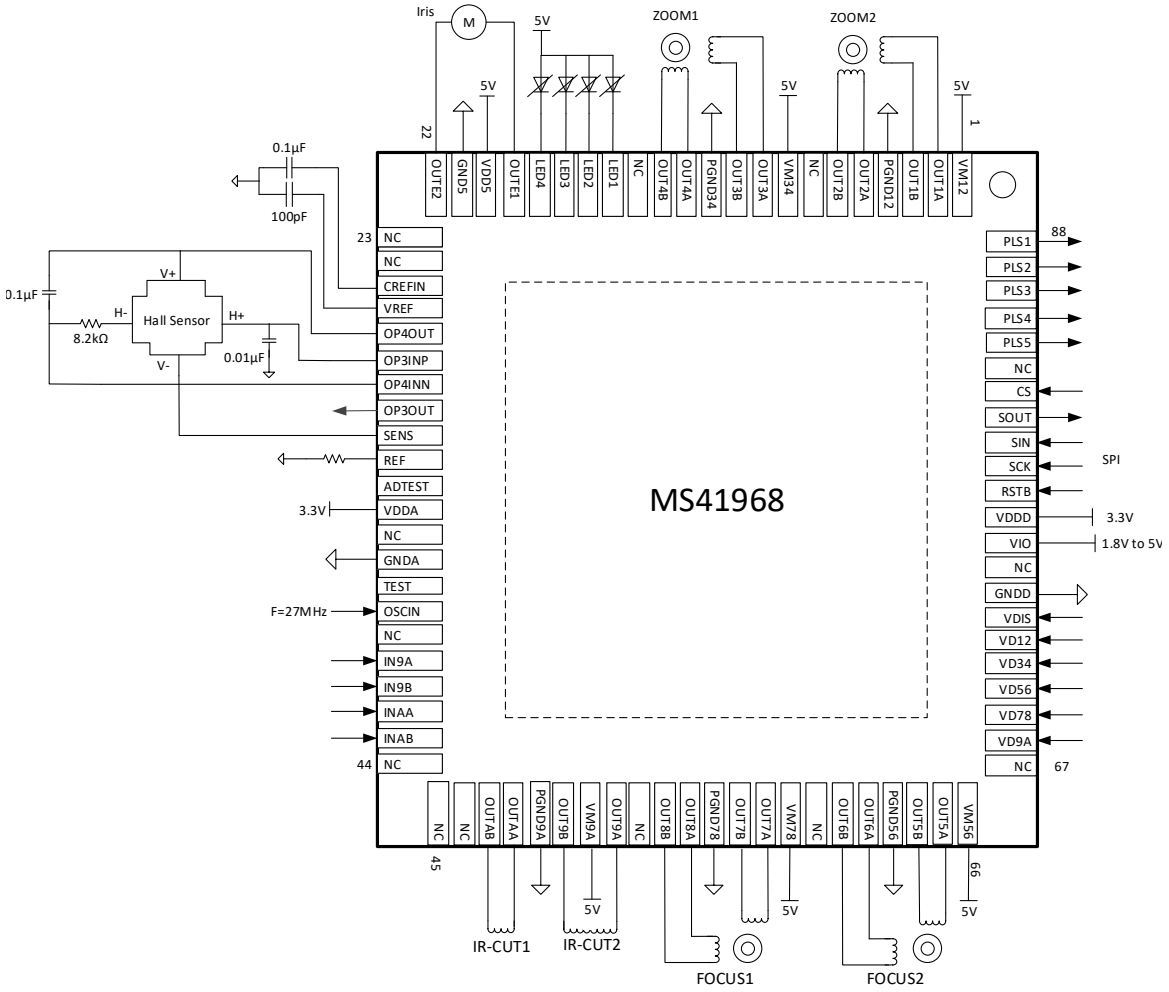
	Normally	Hall Amplifier	Focus/Zoom Output	Iris Output	LED
Pin RSTB	Disable	Logic Reset - > Disable	Logic Reset -> Output Off		
Thermal Shutdown (TSD)	×	×	Output Off		
Undervoltage Lockout (UVLO)	×	Logic Reset - > Disable	Logic Reset -> Output Off		

7. Input and Output Level Translation

In order to meet the logic signal of front-end processor, the MS41968 also integrates level translation circuit. Set the voltage on VIO (Pin12) to be equal to interface voltage and achieve level match.



TYPICAL APPLICATION DIAGRAM

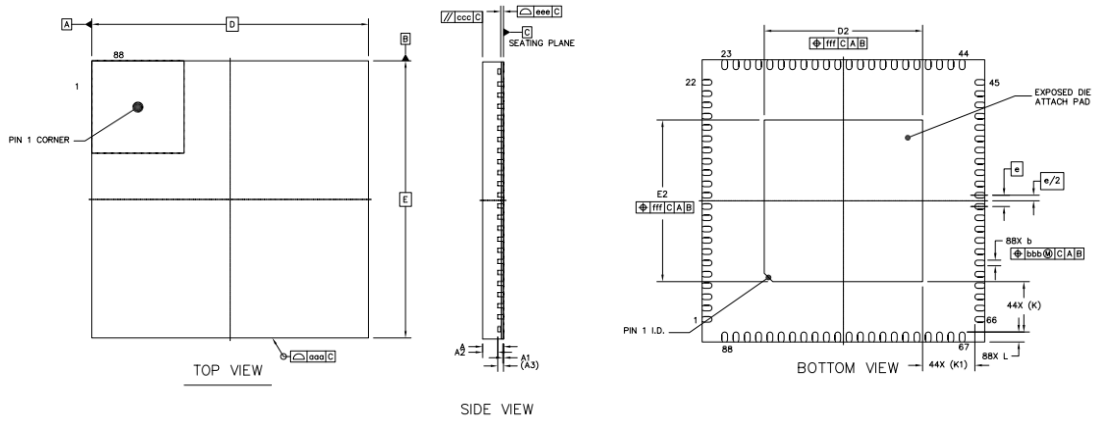


Note: VIO provides power supply for digital input pin. Input logic voltage should not exceed VIO.

VDDA and VDDD need to be connected together to connect with 2.7V to 5V power supply. In addition, it needs to ensure that VMxx voltage is more than or equal to VDDA voltage.

PACKAGE OUTLINE DIMENSIONS

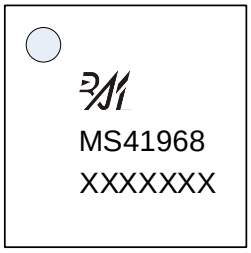
QFN88



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3		0.203 REF	
b	0.15	0.2	0.25
D		10 BSC	
E		10 BSC	
e		0.4 BSC	
D2	5.5	5.6	5.7
E2	5.63	5.73	5.83
L	0.25	0.35	0.45
K		1.785 REF	
K1		1.85 REF	
aaa		0.1	
ccc		0.1	
eee		0.08	
bbb		0.07	
fff		0.1	

MARKING and PACKAGING SPECIFICATION

1. Marking Drawing Description



Product Name: MS41968

Product Code: XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Tray	Tray/Box	Piece/Box	Box/Carton	Piece/Carton
MS41968	QFN88	168	10	1680	4	6720

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS41968	QFN88	2000	1	2000	8	16000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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