SYNC separator IC with AFC

Description

The MS7218 contains a video synchronization separation circuit, a vertical video synchronization separation circuit,a horizontal oscillation circuit, and a phase comparator. It separates and outputs the horizontal and vertical synchro-nization signals (HD and VD), and the composite synchronization signal (Sync-out) from input video or composite synchronization signals. The phase difference between HD and VD is guaranteed for both the rising and falling edges of VD.

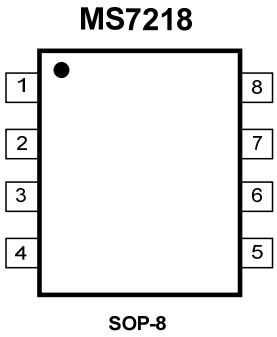


Fig. 1

Features

- Built in AFC circuit.
- HD and VD phase difference guaranteed.
- Wide supply voltage range (3V to 7V).
- Horizontal free-run frequency does not require adjustment.
- Low external parts count.
- SOP 8-pin package.

Applications

- TVs
- VCR
- camcorders

Product class

product	package	Print name
MS7218	SOP8	MS7218

Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	VCC	8.0	V
Power dissipation	Pd	350	mW
Operating temperature	Topr	–40 — 85	℃
Storage temperature	Tstg	–55 —125	℃

Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VCC	2.85	—	7.5	V

Electrical characteristics

parameter	symbol	min	tye	max	unit	conditions
Quiescent current	IQ	3.0	5.8	8.6	mA	pin 8 open
Minimum SYNC separation level	Vsyn-min	—	0.08	0.15	VP-P	pin 1 terminated with 75Ω resistor
Pulse voltage low	Vp-L	—	0.1	0.3	V	pins 2, 7
Pulse voltage high	Vp-H	4.7	5.0	—	V	pins 2, 7
(Horizontal) free-running frequency	fH.O	13.5	15.7	17.9	KHz	No input signal
Capture range	ΔfCAP	2.3	2.7	—	KHz	——
Lock-in phase	THPH	0.6	1.6	2.6	us	pin 2 falling edge to pin 1 falling edge
HD, VD phase deviation 1	THVD1	19.0	24.0	29.0	us	pin 7 falling edge to pin 2 rising edge
HD, VD phase deviation 2	THVD2	19.0	24.0	29.0	us	pin 7 rising edge to pin 2 rising edge
HD pulse width	THD	9.0	10.0	11.0	us	pin 2 pulse width
VD pulse width	TVD	249	254	259	us	Pin 7 pulse width
VIN, VD phase difference	TINVD	41.0	48.0	55.0	us	pin 1 falling edge to pin 7 falling edge

Block diagram

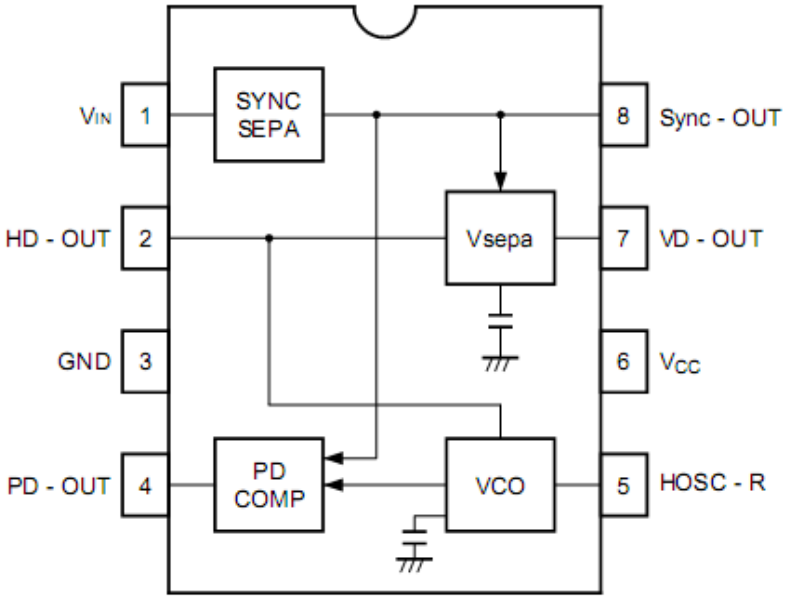


Fig. 2 bolck diagram

Pin No.	Pin name	Function
1	VIN	Video input
2	HD - OUT	HD output
3	GND	GND
4	PD - OUT	Phase comparator output
5	HOSC - R	Horizontal oscillator resistor
6	VCC	Power supply
7	VD - OUT	VD output
8	Sync - OUT	Synchronization signal output

Electrical characteristic curves

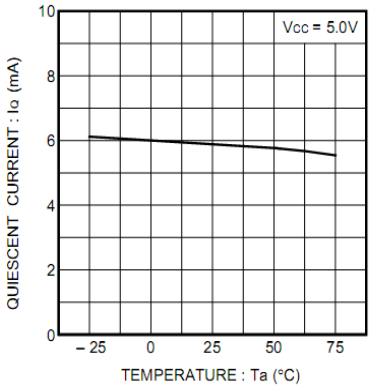


Fig. 3 Quiescent current vs. temperature

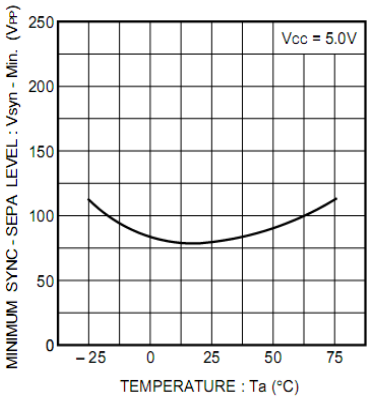


Fig. 4 Minimum synchronization separation level vs. temperature

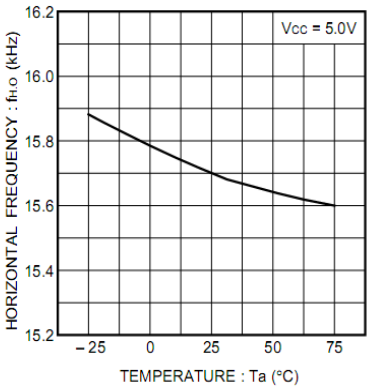


Fig. 5 Horizontal free-running frequency vs. temperature

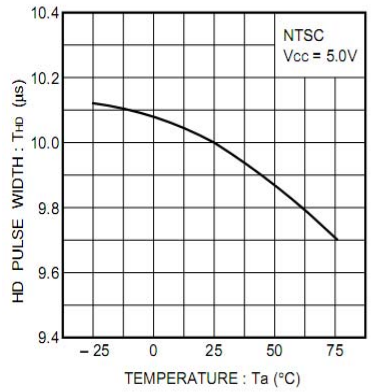


Fig. 6 HD pulse width vs. temperature

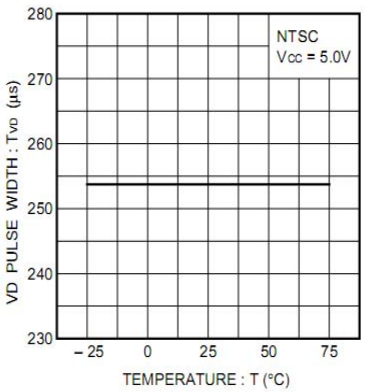


Fig. 7 VD pulse width vs. temperature

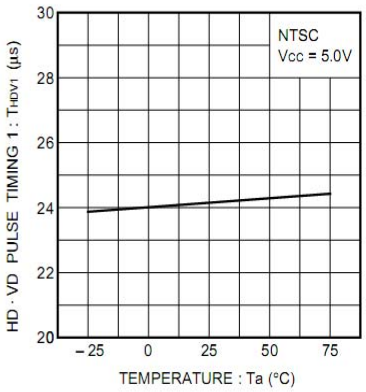


Fig. 8 HD, VD phase difference 1 vs. temperature

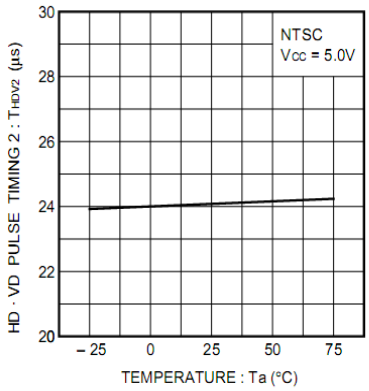
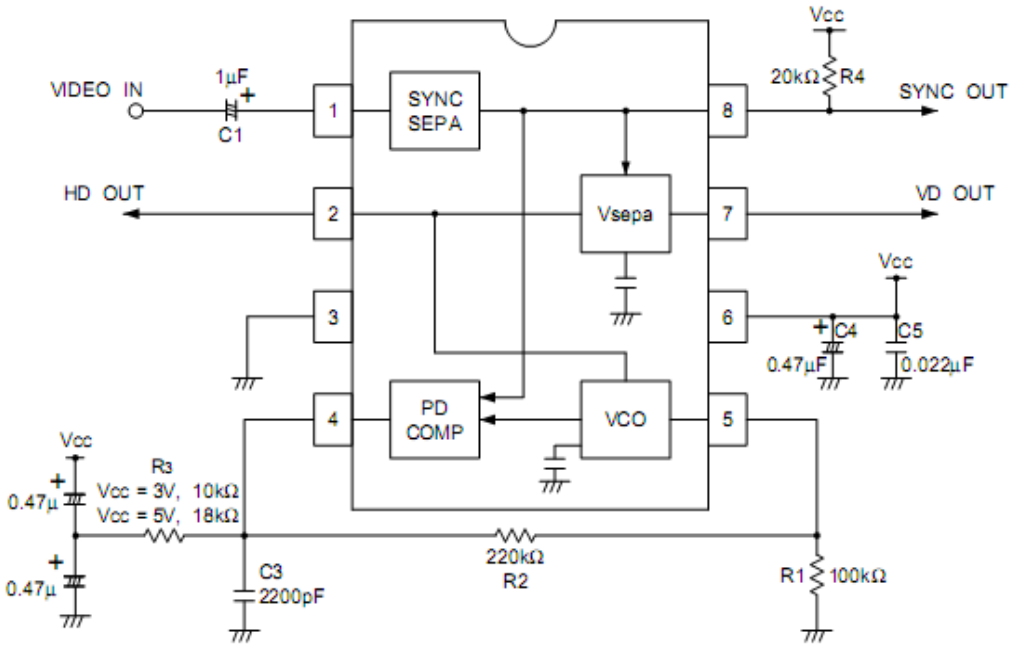
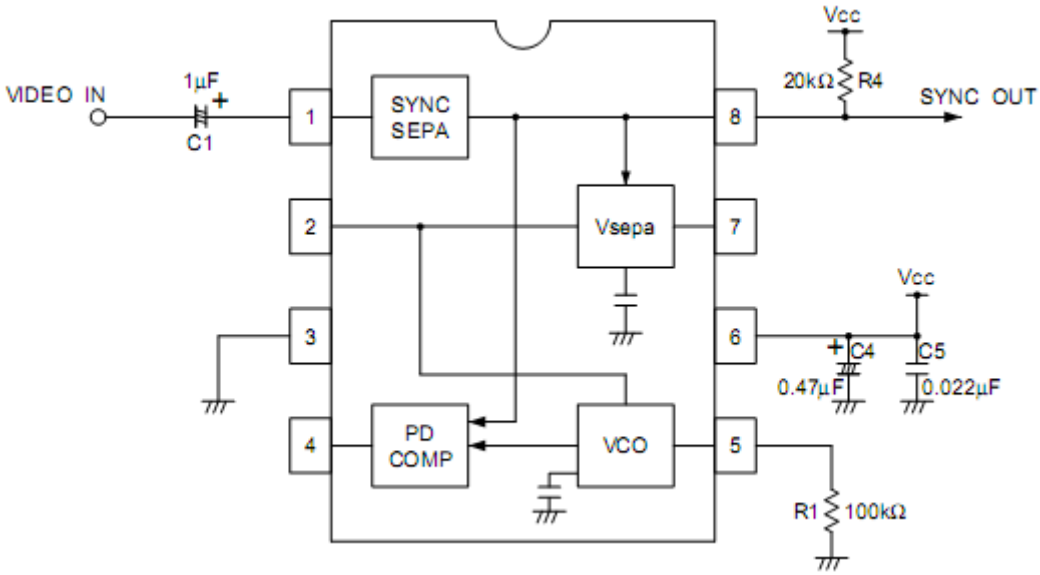


Fig. 9 HD, VD phase difference 2 vs. temperature

Application



When SYNC SEPA output only is used. HD and VD unused



Circuit operation

(1) Synchronization separation circuit

Detects the charging current to a externally-connected capacitor, and performs synchronization separation.

(2) Horizontal oscillation circuit

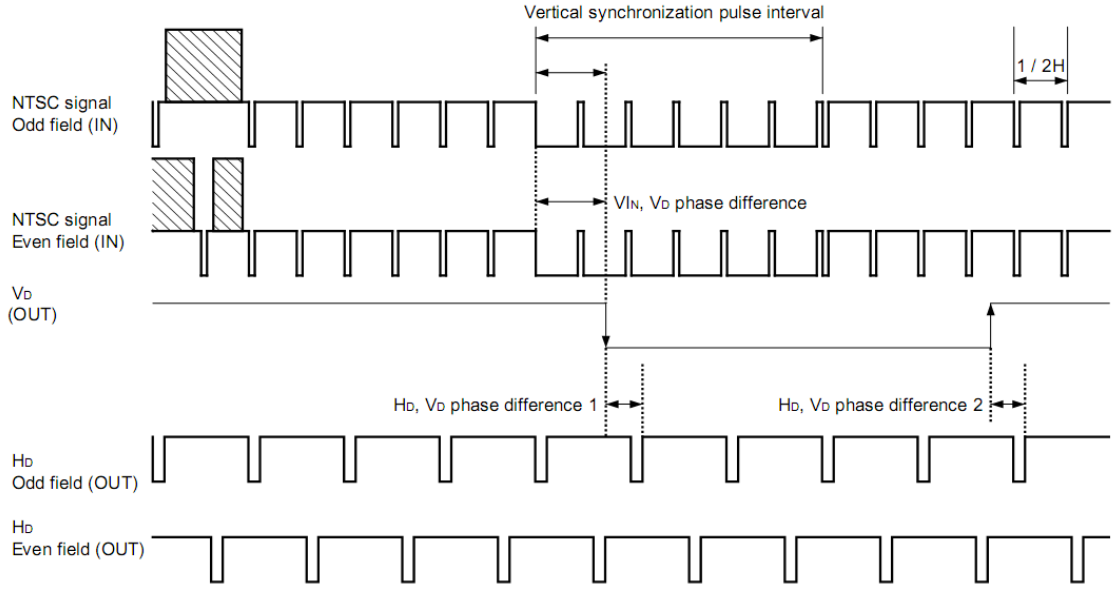
When a video signal is input, it is synchronized with Hsync by the PLL. The horizontal free-running frequency is determined by external resistor R1.

$$f_{H \cdot O} = \frac{1.57E6}{R_1} \quad [kHz]$$

(3) Vertical synchronization separation circuit

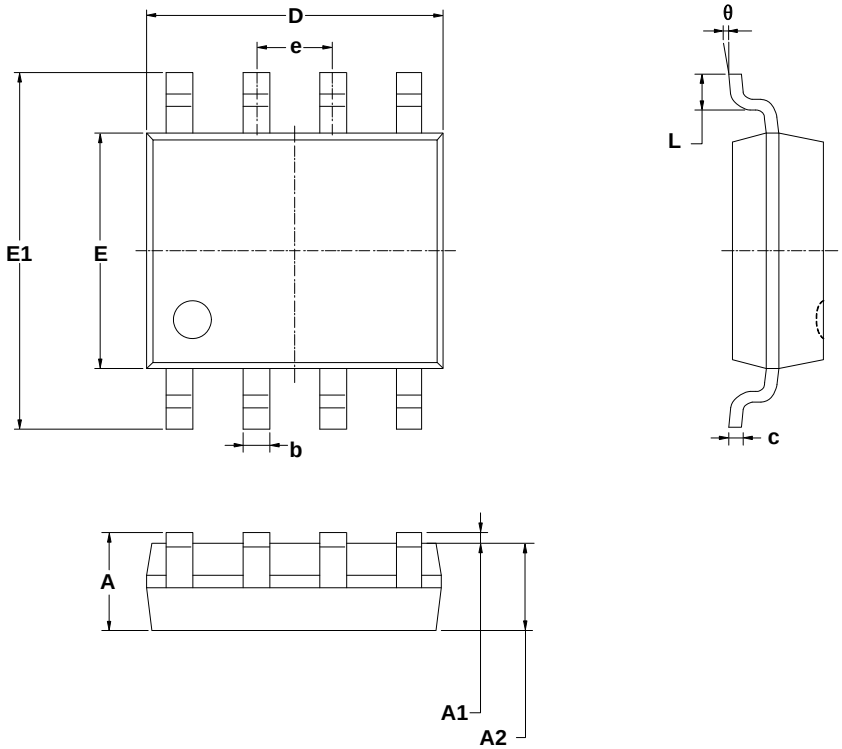
When a video signal is input, synchronization signal separation is done over the vertical synchronization pulse interval.

(4) VIN, HD, and VD timing charts



Package

SOP8



Symbol	dimensions (Units: mm)		dimensions (Units: inch)	
	min	max	min	max
A	1.350	1.750	0.053	0.069
A1	0.100	0.025	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0 °	8 °	0 °	8 °